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A Stacked Symmetrical Non-Isolated High Step-Up Voltage Gain Converter with High Efficiency and Low Voltage Stress on Components

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Abstract: This paper introduces a cascaded symmetrical non-isolated high step-up voltage gain converter with high efficiency and low voltage stress on components combining a non-isolated buck-boost converter and voltage doubler structure. In the proposed converter, the input source is connected in series to the output load; hence, a part of the source energy is directly delivered from source to load, not through the switching branch, improving efficiency. Furthermore, the appropriately stacked voltage doubler stage not only amplifies the high step-up voltage gain ratio but also considerably diminishes the voltage stress on all semiconductor devices and capacitors. As a result, the costless low internal resistance and low voltage components can be employed for higher efficiency, higher power density, and lower cost. To demonstrate the practicality of the proposed topology, the operating principle is outlined, and the steady-state characteristics are thoroughly analyzed. Furthermore, a 360 W prototype converter has been fabricated to confirm the efficiency of the proposed converter.

Keywords: stacked symmetrical non-isolated converter; high efficiency; inverting buck-boost; low voltage stress; voltage doubler

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1. Introduction

Following the zero-carbon emission commitment of countries, renewable energy increasingly plays an important role in progressively dropping dependence on fossil fuels. Technically, renewable energy sources like fuel cells and solar cells generate direct current (DC) at low voltages, typically ranging between 25 V and 45 V [1,2]. Hence, employing a high voltage gain DC-DC converter to elevate the renewable source's low voltage is crucial for supplying an appropriate DC link voltage to the subsequent DC-AC inverter, which uses 380 VDC for single-phase AC systems or 800 VDC for three-phase AC systems [3,4].

The simple solution that could be used is the isolated DC-DC converter topologies; however, it would not be a good option for small power systems in which volume and cost are critical factors. Traditional non-isolated DC-DC converters, like the non-isolated boost converter, are viable options for such applications. Nonetheless, its gain is capped due to the inductor's parasitic components, and as the duty cycle nears one, the inductor's current ripple and the power device's hard-switch current increase, leading to substantial conduction and switching losses [1,2]. Furthermore, parasitic elements also introduce additional impedance and energy storage characteristics that can affect the overall performance and reliability of the system. Trace inductance, for example, can lead to undesired voltage spikes and ringing in the circuit due to the inductive energy stored during rapid changes in current. This can result in increased voltage stresses on components, potentially causing voltage breakdown or negatively impacting the lifespan of the devices. On the other hand, parasitic capacitances can affect the current stresses by introducing additional charge/discharge

paths. This can lead to increased switching losses, higher power dissipation, and potential issues with signal integrity [5].

Over the past decade, numerous advanced boosting methods have been devised to surpass the constraints of traditional topologies. In [6], a new DC-DC converter with reduced inductor current was introduced to achieve a larger ratio of duty cycle to voltage gain and an inductor with a smaller current and reduced inductance. As a result, a smaller peak current is obtained. In general, the topologies can be categorized into multi-stage/interleaved boost converters, coupled-inductor-based topologies, switched capacitors, voltage doublers, and voltage lift techniques, each with distinct benefits and limitations [1,2].

The multi-stage [7–9], or interleaved boost converter [10–12], could be the first consideration. Reference [10] shows various configurations employing an interleaved boost converter with a clamped capacitor structure. Reference [11] detailed multiple interleaved boost converters integrated with voltage doubler cells. While these converters achieve high voltage gain, they are disadvantageous due to complex controls, component stress, larger volume, and hard-switching that lead to reduced efficiency [12].

Coupled inductor-based techniques, as in [13–24], seem to be a good choice. The voltage step-up gain is most dependent on the winding ratio. However, due to the voltage spike on the switch caused by leakage inductance, the external snubber is required, making the system complex and expensive. A further limitation of the coupled inductor-based topology is the excessive voltage stress on components, particularly those positioned after the coupled inductor's second winding.

Non-magnetic coupling topologies, including the converters utilizing the switched capacitors (SCs) [25–34] and the voltage multiplier (VMs) [35–39], are also popular methods to achieve a high step-up ratio. Yet, converters utilizing SCs typically underperform regarding switch and capacitor voltage stresses due to the involvement of various voltages and the fact that most switches are not ground-referenced, complicating implementation. Another significant problem with SCs is the pulsating current caused by the charging and discharging of the capacitors. To address this issue, certain converters integrate SCs with additional magnetic components. The converter described in [28] merges two SCs with an energy storage (ES) cell. The pulsating current is mitigated, and the voltage stress on the switches is decreased. Unfortunately, the efficiency of this topology is low due to hard switching. Moreover, three large inductors need to be used, and the output capacitor is still stressed by the output voltage. As a result, the size and cost of this converter increase significantly. The converter mentioned in [29] improves efficiency, yet the voltage stress on components remains high, and control complexity increases due to the use of three main switches. While the converter in [30] achieves high voltage gain with a low-duty cycle, the high voltage stress on components and the notably low efficiency due to the absence of soft-switching techniques are significant drawbacks.

Similar to SC topology, converters with VMs benefit from the simplicity and ease of cascading for higher voltage gain, yet they primarily suffer from high stress on components and low efficiency [35–38]. The converter in [38] is structured to attain high gain with reduced component stress by symmetrically cascading voltage multipliers (VMs). However, its efficiency is not enhanced due to the persistence of hard-switching. Additionally, the voltage lift (VL) technique [40–44] is considered a promising approach for achieving high voltage gain. Luo introduced several lifting methods in [40], and various topologies based on these techniques have been proposed in [41–48]. However, this technique requires multiple inductors, which increases the circuit's volume. Additionally, the stress on components remains high, particularly for those near the output side. To address the aforementioned issues, a proposed solution is a converter that achieves high efficiency and low voltage stress on all components.

The proposed converter is devised by attaching the positive and negative voltage doublers (VDs), as depicted in Figure 1a,b, to the upper and lower parts of the modified inverting buck-boost converter (m-IBB) shown in Figure 1a. The m-IBB converter's output is

serially linked with the capacitors of the voltage doublers, facilitating a substantial step-up in voltage gain. Moreover, this configuration reduces the voltage stress on all semiconductor devices and capacitors. A notable advantage is the enhanced power conversion efficiency since a part of input power is directly transferred to the load, not through switching devices. For even greater voltage gain, the design allows for simple expansion by adding more VDs at both the top and bottom of the m-IBB converter's output. It should be noted that while having different grounds between input and output is a primary drawback, it does not significantly affect the complexity of the control design. This is because only one half-bridge MOSFET needs to be controlled, which can be easily addressed with a simple half-bridge gate driver with a bootstrap configuration.

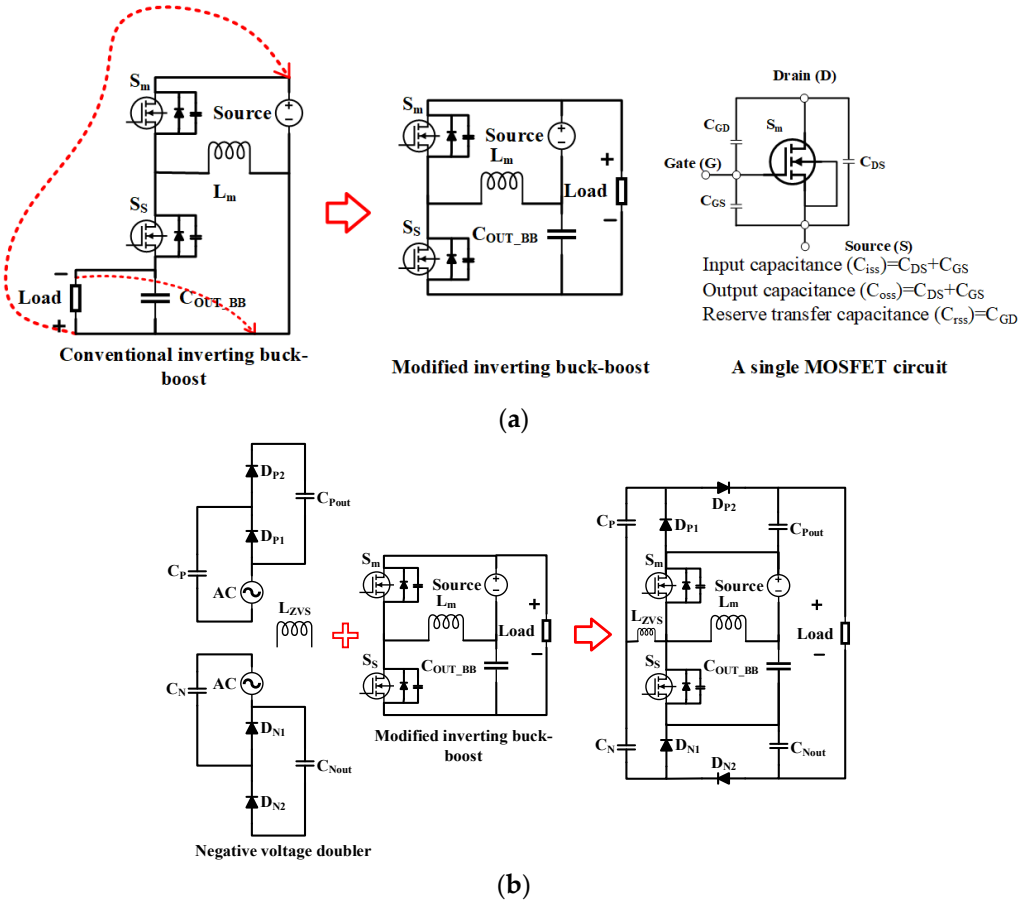

Figure 1. The revolution of the proposed topology; (**a**) The modified inverting buck-boost; (**b**) Integrating the voltage doublers.

This paper consists of five sections. Section 2 outlines the operating principles of the proposed converter. Section 3 details the design process for the proposed converter with two stages of the VDs. A comparative analysis of the proposed topology with other topologies is provided in Section 4. Section 5 discusses the experimental results to highlight the advantages of the proposed converter, culminating in a conclusion in Section 6.

2. Structure and Operating Principles

2.1. Structure

As shown in Figure 2, the proposed converter is constituted by four main parts: The modified synchronous inverting buck-boost is in the center as a source for N stages positive and negative voltage doublers (VDs) connected in series at both sides forming the symmetrical configuration. The Zero-Voltage Switching (ZVS) inductor in the common path of the positive and negative VDs is the main factor in achieving soft switching for all

MOSFETs and diodes and eliminating the pulsating current caused by the source capacitor C_P and C_N of VDs. By connecting the output of m-IBB in series with its input, a higher step-up voltage gain can be achieved. Moreover, a part of power can be transferred directly from input to output, reducing losses and, hence, achieving higher efficiency. Furthermore, to attain an even higher voltage gain, the proposed converter can be readily extended by adding additional VDs in a cascading manner at both the top and bottom of the m-IBB output, all while maintaining the same voltage stress on components.

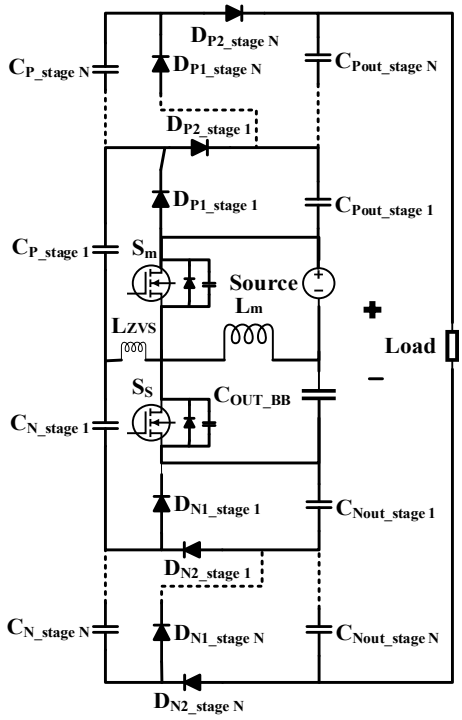

Figure 2. The proposed topology N stages of the voltage doubler.

2.2. Working Principle

To simplify the working of the converter, the detailed analysis of the operation principle of the proposed converter is applied for only one stage of positive and negative VDs, and the voltage gain and voltage applied to components for N-stage VDs can be easily extended from a one-stage structure.

The operating principle of the proposed converter is examined in continuous conduction Mode (CCM), with the component operation waveforms depicted in Figure 3. One switching period of the proposed converter is segmented into six Modes, delineated by the status of the main switches of the m-IBB. The equivalent circuits for each Mode are illustrated in Figure 4. To elucidate the operating principle of the proposed converter, the following assumptions must be established:

- All components are ideal, with parasitic components disregarded;
- The circuit operates in a steady state with continuous inductor current;
- All capacitors C_P and C_N have the same value;
- All output capacitors C_{Pout}, C_{Nout}, and C_{OUT_BB} have the same value of C_{out} and are sufficiently large to keep their voltages constant during the switch-off period.

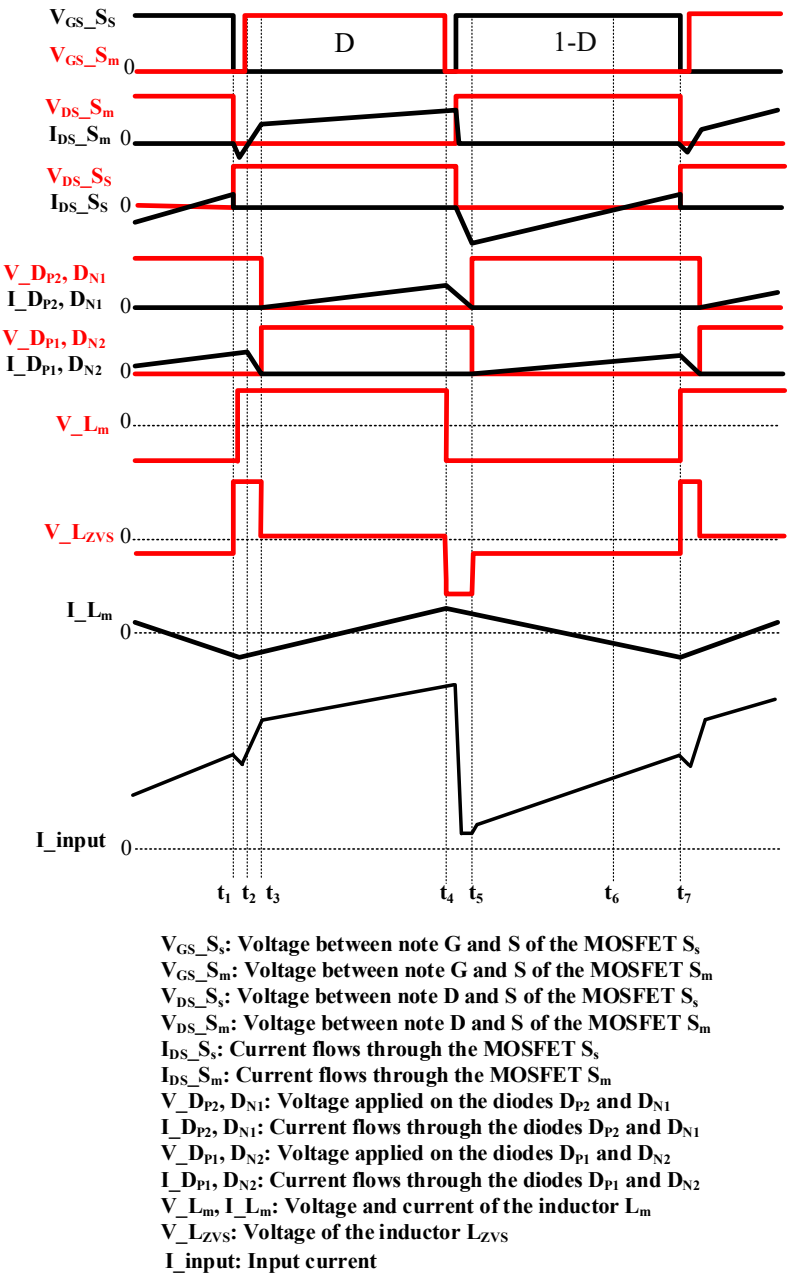

Figure 3. Operating waveform.

The switching period is T_s; switches close for a duration of DT_s and open for $(1-D)T_s$.

(1) Mode 1 (t_1–t_2): ZVS Turn-On Condition for Main Switch S_m

Before that, the main switch S_m is off, and diodes D_{P1} and D_{N1} are reverse-biased. D_{P1} and D_{N2} are forward-biased. The synchronous switch S_S is conducted through the main channel, not the body diode.

This Mode is started when S_S switches off, the parasitic capacitor of S_S is charged raising the voltage applied to this switch resulting in the discharge of the parasitic capacitor of the main switch S_m and reducing the voltage V_{DS} applied to drain-source of S_m. Since the parasitic capacitor of S_m becomes fully discharged, the V_{DS} of S_m will reach zero. Right the time the parasitic capacitor of S_m discharged totally, the ZVS inductor L_{ZVS} starts discharging and then changes its voltage polarity, leading to the forward bias of the body diode of S_m, then creating a ZVS turn-on for this main switch. At the end of this Mode, S_m switches on with ZVS condition.

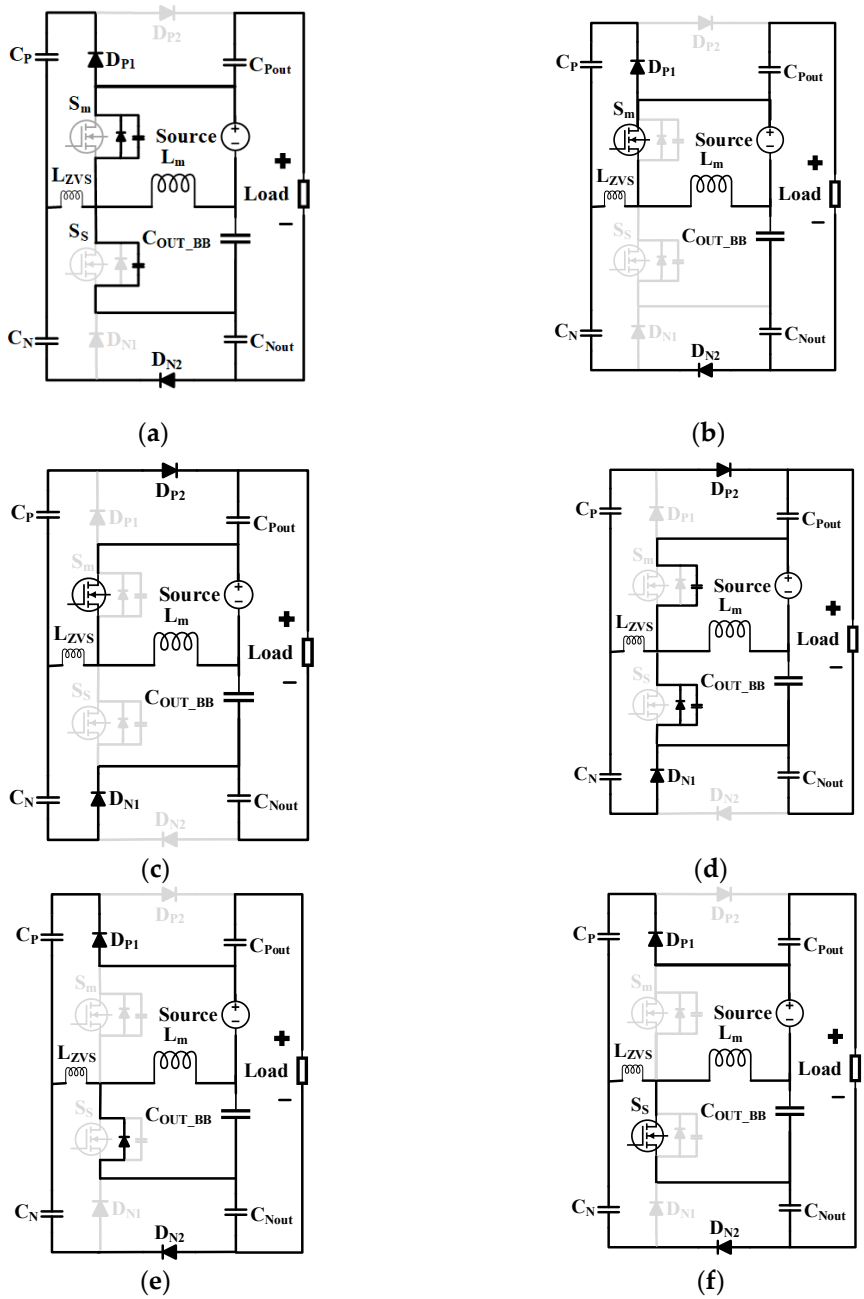

Figure 4. Operation Mode: (**a**) Mode 1; (**b**) Mode 2; (**c**) Mode 3; (**d**) Mode 4; (**e**) Mode 5; (**f**) Mode 6.

(2) Mode 2 (t_2–t_3): ZCS (Zero-Current Switching) Turn-Off Condition for Diode D_{P2} and D_{P1}

S_m is fully on, and the current flows through its main channel. Due to the discharging of ZVS inductor L_{ZVS}, the current flows through diode D_{P1} and D_{N2} decreases and reaches zero at the end of this Mode, forming a ZCS turn-off condition for these diodes.

$$V_{C_P} = V_{L_m} + V_{C_{oss\_Sm}} + V_{L_{ZVS}} + V_{Source} \tag{1}$$

$$V_{C_P} + V_{L_{ZVS}} + V_{L_m} = V_{C_{OUT\_BB}} + V_{C_{Nout}} + V_{C_{oss\_S_S}} \tag{2}$$

$$V_O = V_{C_{Pout}} + V_{C_{OUT\_BB}} + V_{C_{Nout}} + V_{Source} \tag{3}$$

(3) Mode 3 (t_3–t_4): Main Energy Transfer Mode

At the start of this Mode, S_m is on, S_S is off. The main inductor L_m and ZVS inductor L_{ZVS} are storing energy. Diodes D_{P2} and D_{N1} are conducted, D_{P1} and D_{N2} are off, capacitors C_N and C_{Pout} are charged, C_P and C_{OUT_BB} are charged.

The output voltage V_o and voltage applied on components in this Mode can be expressed as follows.

$$V_{L_m} = V_{Source} \tag{4}$$

$$V_{C_P} = V_{C_{Pout}} + V_{L_{ZVS}} \tag{5}$$

$$V_{L_m} = V_{C_N} - V_{C_{OUT\_BB}} + V_{L_{ZVS}} \tag{6}$$

$$V_O = V_{C_{Pout}} + V_{C_{OUT\_BB}} + V_{C_{Nout}} + V_{Source} \tag{7}$$

Since the current I_{Lzvs} is the combination of the current that flows through C_{Pout} and C_{OUT_BB}. Given that all the output capacitors are connected in series, and each has the same value as initially assumed, the current I_{Lzvs} flowing through the ZVS inductor L_{zvs} can be determined as expressed in Equation (8).

$$I_{L_{ZVS}} = \frac{2C_{Pout}\Delta V_o}{(t_4 - t_3)T_s} \tag{8}$$

Then, the voltage of ZVS inductor L_{zvs} can be calculated as in (9).

$$V_{L_{ZVS}} = \frac{L_{ZVS}di_{L_{ZVS}}}{dt} = \frac{L_{ZVS}2C_{Pout}\Delta V_o}{((t_4 - t_3)T_s)^2} \tag{9}$$

(4) Mode 4 (t_4–t_5): ZCS Turn Off Condition for Diodes D_{P1} And D_{N2}

At the start, S_m switches off, and S_S switches on. The diodes D_{P1} and D_{N2} are reverse-biased, and D_{P2} and D_{P1} are forward-biased. S_S is conducted via its body diode, the parasitic capacitor of S_S is discharged, and that of S_m is charged. The main and ZVS inductors discharge, resulting in the decrement of the current through diodes D_{P2} and D_{P1} and creating ZCS turn-off for these diodes when the ZVS inductor L_{ZVS} is fully discharged.

The voltage equations in this Mode are given in (3).

$$V_{C_P} = V_{C_{Pout}} + V_{C_{OSS\_S_m}} + V_{L_{ZVS}} \tag{10}$$

$$V_{Source} = V_{L_m} + V_{C_{OSS\_S_m}} \tag{11}$$

$$V_{C_N} = V_{C_{OSS\_S_S}} + V_{L_{ZVS}} \tag{12}$$

$$V_{C_{OSS\_S_S}} = V_{L_m} + V_{C_{OUT\_BB}} \tag{13}$$

$$V_O = V_{C_{Pout}} + V_{C_{OUT\_BB}} + V_{C_{Nout}} + V_{Source} \tag{14}$$

(5) Mode 5 (t_5–t_6): Main Energy Transfer Mode

In this Mode, the energy accumulated in the inductor is released to the output capacitor C_{OUT_BB}, while the blocking capacitor C_N of the negative VD discharges to the output capacitor C_{Nout}. Following its complete discharge in Mode 3, the secondary side ZVS inductor L_{ZVS} is recharged. Simultaneously, the blocking capacitor C_P of the positive VD is charged in preparation for the next discharging cycle.

(6) Mode 6 (t_6–t_7): Main Energy Transfer Mode

At $t = t_6$, as the voltage across capacitor C_{OUT_BB} rises above that of the main inductor, the body diode of S_S becomes reverse-biased, causing the current to flow through S_S rather than its body diode. By $t = t_7$, the end of this Mode, one switching period concludes, setting the stage for the next cycle.

The output voltage and voltage applied on components in Modes 5 and 6 can be expressed as follows:

$$V_{L_m} = -V_{C_{OUT\_BB}} \tag{15}$$

$$V_{L_m} = V_{Source} - V_{C_P} - V_{L_{ZVS}} \tag{16}$$

$$V_{C_N} = V_{C_{Nout}} + V_{L_{ZVS}} \tag{17}$$

$$V_O = V_{C_{Pout}} + V_{C_{OUT\_BB}} + V_{C_{Nout}} + V_{Source} \tag{18}$$

The same as in Mode 3, the current I_{LZVS} flowing through the ZVS inductor L_{ZVS} can be calculated as in (19).

$$I_{L_{ZVS}} = \frac{2C_{Pout}\Delta V_o}{(t_7 - t_5)T_s} \tag{19}$$

Then, the voltage of inductors L_{ZVS} can be extracted as in (20)

$$V_{L_{ZVS}} = \frac{L_{ZVS}di_{L_{ZVS}}}{dt} = \frac{2L_{ZVS}C_{Pout}\Delta V_o}{((t_7 - t_5)T_s)^2} \tag{20}$$

2.3. Steady-Stage Analysis of the Proposed Converter

2.3.1. Voltage Gain Expression

In the steady state, since Mode 1 occurs briefly, we can disregard these two Modes for steady-state analysis. Consequently, the period from t_2 to t_4 is DT_S, and the period from t_5 to t_7 is $(1 - D)T_S$. Applying the voltage-second principle of the inductor L_m, the average voltage across the inductor L_m in the switching period is zero, and the following equations can be obtained from (4)–(9) and (15)–(20).

$$\overline{V}_{L_m} = DV_{Source} - (1 - D)V_{C_{OUT\_BB}} = 0 \tag{21}$$

$$\overline{V}_{L_m} = DV_{Source} - (1 - D)(V_{Source} - V_{C_P} - V_{L_{ZVS}}) = 0 \tag{22}$$

$$\overline{V}_{L_m} = D(V_{C_N} - V_{C_{OUT\_BB}} + V_{L_{ZVS}}) - (1 - D)V_{C_{OUT\_BB}} = 0 \tag{23}$$

$$V_O = V_{C_{Pout}} + V_{C_{Nout}} + V_{C_{OUT\_BB}} + V_{Source} \tag{24}$$

Then, the voltage of each capacitor can be obtained:

$$V_{C_{OUT\_BB}} = \frac{DV_{Source}}{1 - D} \tag{25}$$

$$V_{C_N} = \frac{V_{Source}}{1 - D} - \frac{2L_{ZVS}C_{Nout}\Delta V_o}{(DT_s)^2} \tag{26}$$

$$V_{C_P} = \frac{V_{Source}}{1 - D} - \frac{2L_{ZVS}C_{Pout}\Delta V_o}{((1 - D)T_s)^2} \tag{27}$$

$$V_{C_{Pout}} = \frac{V_{Source}}{1 - D} - \frac{2L_{ZVS}C_{Pout}\Delta V_o}{((1 - D)T_s)^2} - \frac{2L_{ZVS}C_{Pout}\Delta V_o}{(DT_s)^2} \tag{28}$$

$$V_{C_{Nout}} = \frac{V_{Source}}{1 - D} - \frac{2L_{ZVS}C_{Nout}\Delta V_o}{((1 - D)T_s)^2} - \frac{2L_{ZVS}C_{Nout}\Delta V_o}{(DT_s)^2} \tag{29}$$

The voltage gain equation can be expressed as in (30).

$$V_o = \frac{3V_{Source}}{1 - D} - \frac{4L_{ZVS}C\Delta V_o}{((1 - D)T_S)^2} - \frac{4L_{ZVS}C\Delta V_o}{(DT_S)^2} \tag{30}$$

Furthermore, the ultra-high voltage gain can be easily achieved with the proposed converter by cascading more VD stages. It is important to ensure that the number of positive voltage doubler stages cascaded equals the number of negative voltage doubler stages, maintaining a symmetrical configuration. Assume that there are N stages of positive VDs and N stage negative VDs cascaded more. Theoretically, the cascaded voltage doubler stages function as a conventional voltage doubler, with the voltage output of each stage

being twice that of its source. Then, the voltage output of N VD stages can be expressed as in (31).

$$V_{O_{TOT}} = \frac{(3+2N)V_{Source}}{1-D} - \frac{4L_{ZVS}C\Delta V_{O_{TOT}}}{((1-D)T_S)^2} - \frac{4L_{ZVS}C\Delta V_{O_{TOT}}}{(DT_S)^2} \quad (31)$$

2.3.2. Voltage Stress on Components

In the proposed converter, it should be noted that the voltage across the switch and diodes are clamped by the capacitors. Consequently, low voltage stress can be attained for all semiconductor devices and passive components. Equation (25)–(29) demonstrates the voltage stress on all capacitors, while the stress on semiconductor devices is detailed in (32)–(34).

$$V_{S_m} = V_{S_S} = \frac{V_{Source}}{1-D} \quad (32)$$

$$V_{D_{P1}} = V_{D_{P2}} = V_{C_P} = \frac{V_{Source}}{1-D} - \frac{2L_{ZVS}C\Delta V_o}{((1-D)T_s)^2} - \frac{2L_{ZVS}C\Delta V_o}{(DT_s)^2} \quad (33)$$

$$V_{D_{N1}} = V_{D_{N2}} = V_{C_N} = \frac{V_{Source}}{1-D} - \frac{2L_{ZVS}C\Delta V_o}{((1-D)T_s)^2} - \frac{2L_{ZVS}C\Delta V_o}{(DT_s)^2} \quad (34)$$

From (25)–(29) and (32)–(34), it is evident that the voltage stress on components is significantly lower than the output voltage and does not depend on it. This characteristic is a crucial advantage for high-gain step-up applications. For N-stage VDs cascaded, essentially, all the diodes and capacitors of the positive voltage doubler stages experience uniform voltage stress. In (33), the general voltage stress equation for diodes and capacitors of positive voltage doubler stages can be expressed.

Likewise, all the diodes and capacitors of the negative voltage doubler stages endure identical voltage stress, which can be detailed in (34).

2.3.3. ZVS Condition

From Mode 1, we know that, because of the discharging of inductor L_{ZVS}, the voltage V_{DS} of switch S_m becomes zero while it is turning on. Then, the ZVS condition can be expressed as in (35).

$$V_{L_{ZVS}} - V_{C_P} \geq 0 \quad (35)$$

Then, (35) can be expressed as follows.

$$\frac{L_{ZVS}\Delta I_{L_{ZVS}(t_7-t_5)}}{T_a} \geq V_{C_P} \quad (36)$$

where T_a is the time to inductor L_{ZVS} is fully discharged, and equal to the time of Mode 1 and Mode 2 (t_3–t_1).

From (19) and (36), the value of inductor L_{ZVS} can be calculated as in (37).

$$L_{ZVS} \geq \frac{V_{C_P}T_a}{\Delta I_{L_{ZVS\_(t_7-t_5)}}} = \frac{V_{C_P}T_a}{\frac{2C_1\Delta V_o}{(1-D)T_s}} \quad (37)$$

It should be noted that, the current $\Delta I_{L_{ZVS\_(t_7-t_5)}}$ represents the current circulating in the path including L_{ZVS}, C_P, D_{P1} and S_m, as depicted in Figure 4a during Mode 1 and it causes some conduction loss during MOSFET switching. Therefore, its value should be kept small to minimize its contribution to the total losses of the converter. In this study, we opted for a design value of 0.5 A.

3. Design of the Proposed Converter

3.1. The ZVS Inductor Lzvs, Duty Cycle D, and Dead Time T_D of Switches

Initially, it is necessary to determine a boundary for the duty cycle D, after which the boundary voltage of capacitor C_P can be calculated. According to (30), the minimum duty

cycle can be derived from the maximum output voltage when there is no effect of the ZVS inductor, as indicated in (38).

$$D_{\min} = 1 - \frac{3V_{source}}{V_O} \tag{38}$$

Next, we will calculate the value of inductors L_{ZVS}. From the (27), we see that when there is no inductor L_{ZVS}, the maximum voltage of capacitor C_P is as follows. Then, we can calculate the maximum voltage of capacitor C_P when duty cycle D is minimum, as shown in (39).

$$V_{C_P\_\max} = \frac{V_{Source}}{1 - D} \tag{39}$$

From (38) and (39), we can calculate the boundary value of inductor L_{ZVS} with an assumption of discharging time T_r. Then, we can choose the value of inductor L_{ZVS} based on this boundary. After choosing the value for inductor L_{ZVS}, we need to calculate the right value for the duty cycle from (30). The dead time T_d between the two switches must be smaller than the discharging time T_r of the inductor L_{ZVS} to maintain ZVS condition. In addition, the deadtime T_d must be greater than total time taken for the rise and fall of the drain-source voltage of the MOSFETs to ensure the ZVS condition is maintained and to prevent the creation of a short circuit when the high-side MOSFET and low-side MOSFET of the half-bridge conduct simultaneously. This consideration can be determined from the data sheet of the MOSFETs and should be taken into account in the gate driver design.

3.2. Capacitor C_P and C_D

In Mode 1, when the switch S_m is activated but diode D_{P1} continues to conduct, the ZVS inductor L_{ZVS} resonates with the capacitor C_P. To achieve the ZVS condition for S_m, the resonant frequency must be significantly lower than the switching frequency. Additionally, as previously assumed, the capacitors C_P and C_N are of equal value, which can be determined using (40).

$$C_N = C_P >> \frac{1}{(2\pi f_S)^2 L_{ZVS}} \tag{40}$$

3.3. Main Inductor Design

The main inductors L_m are configured to ensure the proposed converter operates in CCM. Consequently, the values for inductor L_m can be calculated accordingly as in (41)

$$L_m \geq \frac{V_{Source} D}{\Delta I_{L_m} f_{SW}} \tag{41}$$

where ΔI_{L_m} is the current ripple of the main inductor L_m, f_{SW} is the switching frequency.

3.4. Output Capacitor Design

The output capacitors can be determined based on the maximum output ripple voltage as (42).

$$C_{out} \geq \frac{I_O D}{f_{SW} \times \Delta V_O} \tag{42}$$

where I_O is the output current

C_{out_Eq} is the equivalent output capacitor, and can be calculated as (43).

$$C_{out\_Eq} = \frac{C_{Pout} C_{OUT\_BB} C_{Nout}}{C_{Pout} C_{OUT\_BB} + C_{OUT\_BB} C_{Nout} + C_{Pout} C_{Nout}} \tag{43}$$

Beginning from Section 2, we assumed that all the output capacitors are of the same value. Therefore, the value of these output capacitors can be calculated accordingly (44)

$$C_{Pout} = C_{Nout} = C_{OUT\_BB} = 3C_{out\_Eq} \geq \frac{3I_O D}{f_{SW} \times \Delta V_O} \tag{44}$$

4. Experiment Results

To verify the superiority of the proposed high step-up topology, a 360 W converter circuit with one stage of VDs is built and tested as in Figure 5 with the specification and used components shown in Tables 1 and 2.

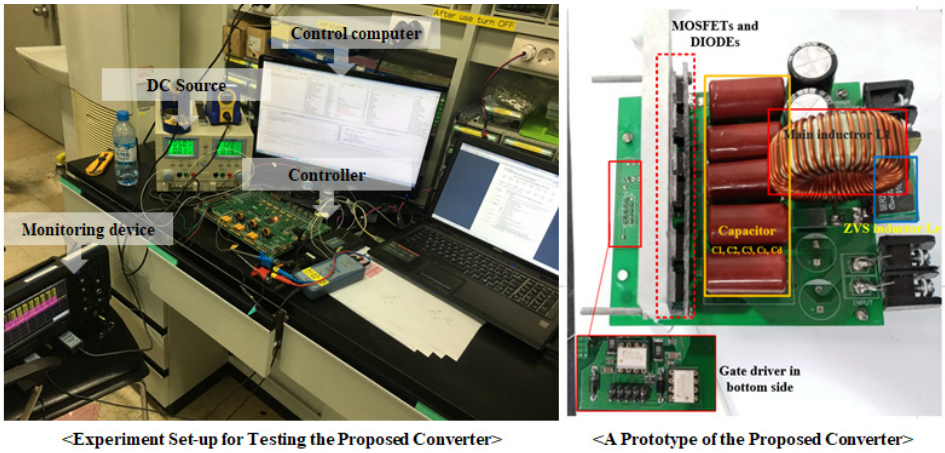

Figure 5. Prototype of the proposed converter.

Table 1. General specification of the proposed converter.

Parameter	Designator	Value
Input voltage	V_{Source}	40 V
Output voltage	V_O	380 V
Power	P_O	360 W
Switching frequency	f_{SW}	100 kHz

Table 2. Specification of component devices.

Devices	Part Number	Specification
Switches (S_m, S_S)	SiR570DP	150 V, 77.4 A
Diodes	STPS10200SF	150 V, 10 A
Capacitors	106MMR250K	10 µF/150 V
Main Inductor (L_m)	CTX100-10-52-R	300 µH
ZVS Inductor (L_{ZVS})	XAL1580-302MED	3 µH

In the experiments, the MCU STM32G431CBT3, a product of STMicroelectronics and sourced from Seoul, South Korea, is used for controlling. The maximum duty cycle of the S_m in full load is 0.73 to boost the input voltage from 40 V to the output voltage of 380 V. The dead time between the two switches is 100 ns.

Figure 6 shows the experimental waveform of all the switches and diodes. As seen in Figure 6a, it is evident that the main MOSFET S_m is turned on with the ZVS condition. Additionally, Figure 6b,c show the voltage and current waveforms for diodes. It is obvious that all the diodes are switched on with ZVS and turned off with ZCS condition. Although there is a small ringing in current through the diode caused by the parasitic components and PCB layout, soft switching is achieved for all switches and diodes.

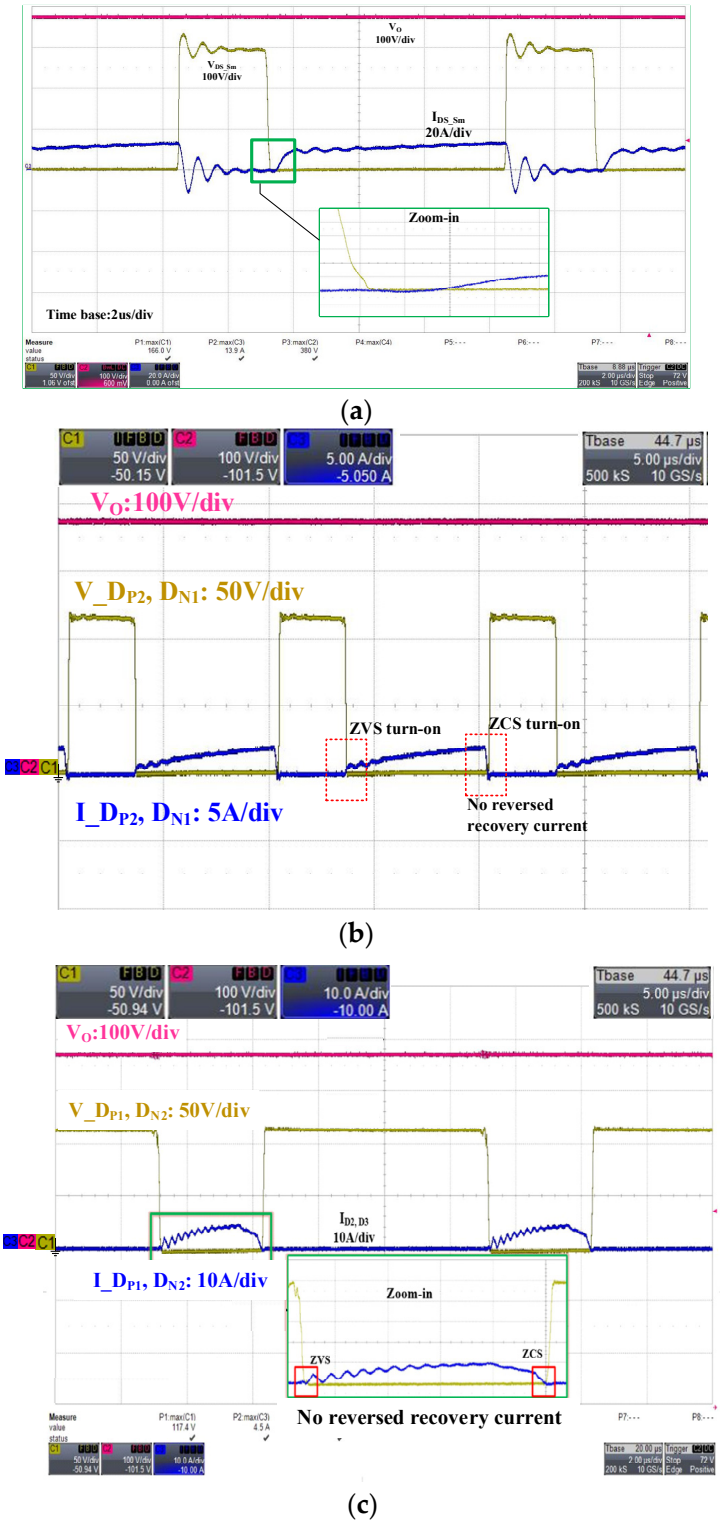

Figure 6. Experimental voltage and current waveforms of the proposed converter: (**a**) Drain-Source voltage and current of the main switch S_m; (**b**) Voltage applied on the diodes D_{P2} and D_{N1} & Current flows through the diodes D_{P2} and D_{N1}; (**c**) Voltage applied on the diodes D_{P1} and D_{N2} & Current flows through the diodes D_{P1} and D_{N2}.

Figure 7 illustrates the voltage across the output capacitors, which, due to the symmetrical configuration, is considerably lower compared to other topologies.

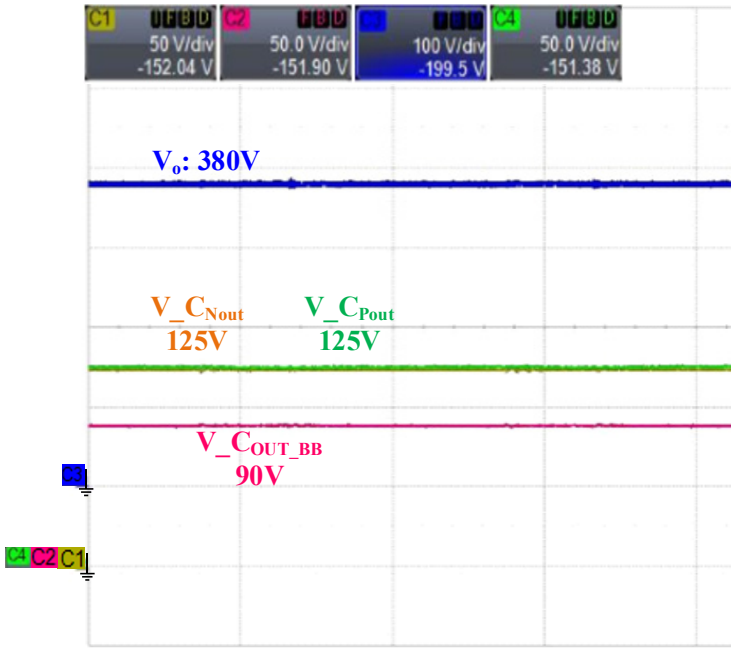

Figure 7. Capacitor voltage waveforms.

Figure 8 presents the waveforms of the main inductor current I_{LZVS} and the voltage waveform of the ZVS inductor V_{LZVS} at full load, closely aligning with the simulation results. It is clear that the ZVS inductor L_{ZVS} fully discharges in a brief period when the switch S_m turns on, fulfilling the requirement for the ZVS condition to occur.

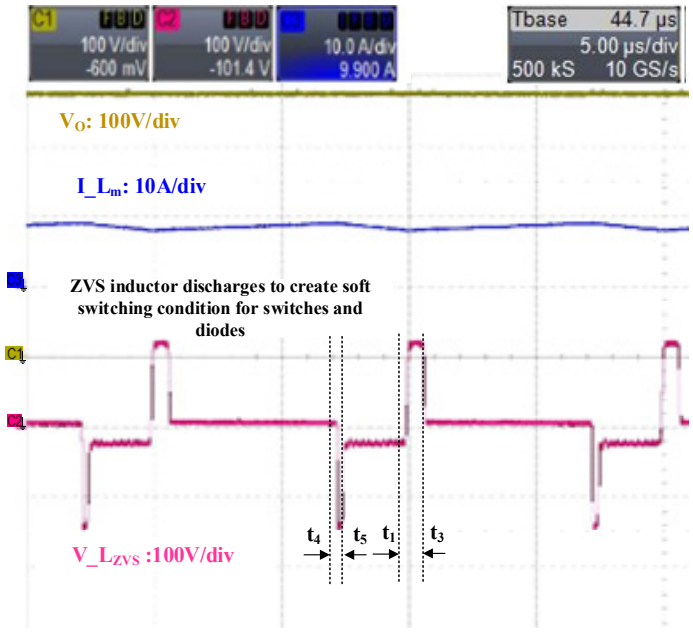

Figure 8. Measured waveforms of main inductor current I_{Lm} and ZVS inductor voltage V_{LZVS}.

Figure 9 displays the efficiency plot for the proposed converter varies to the output power with input parameters of V_{Source} = 40 V, V_O = 380 V, and a switching frequency of 100 kHz. As indicated in Figure 9, the efficiency varies from above 95% at light load to over 97% at heavy load, with a peak efficiency of 97.4% achieved at 295 W.

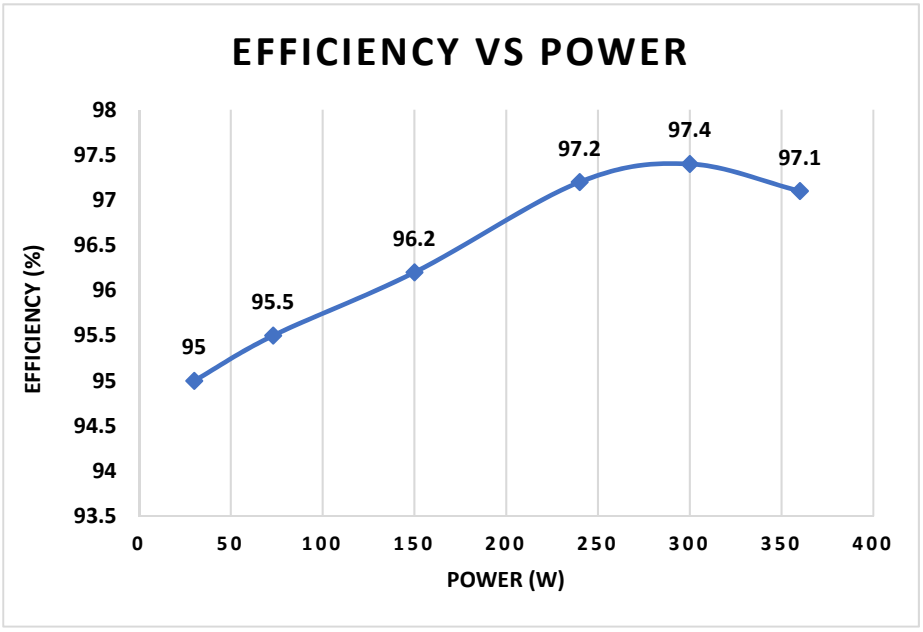

Figure 9. The measured efficiency curve of the proposed converter.

Figure 10 displays the efficiency plot for the proposed converter varying with the input voltage, with input parameters set to output power = 300 W, V_O = 380 V, and a switching frequency of 100 kHz. As indicated in Figure 10, the efficiency ranges from above 94.1% at an input voltage of 24 V to over 97% at an input voltage of 42 V, reaching a peak efficiency of 97.4% at an input voltage of 40 V.

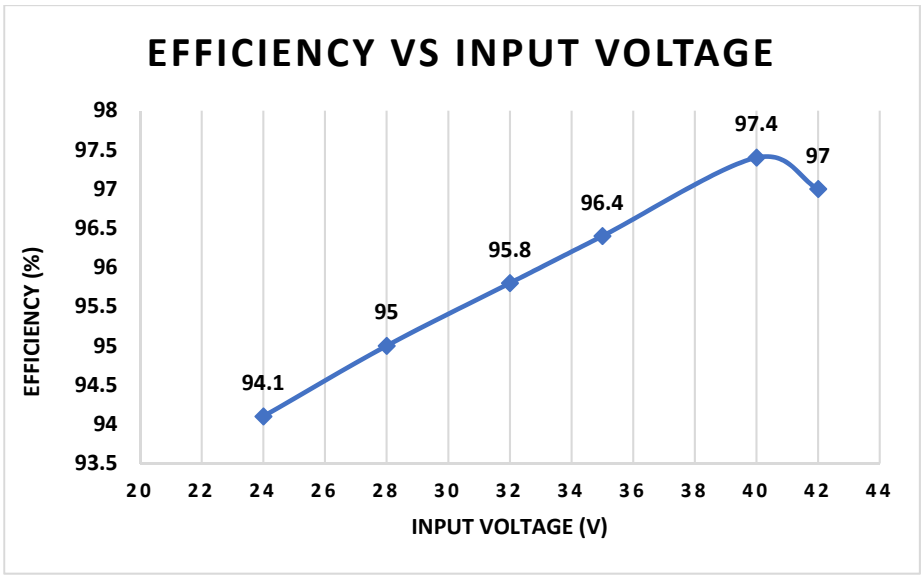

Figure 10. The measured efficiency curve of the proposed converter varies with input voltage.

5. Detailed Comparison and Discussion

From Table 3, we can see that the proposed converter achieves higher efficiency and lower voltage stress on components, especially on the output side components, while maintaining a high step-up gain.

Table 3. Comparison of the proposed converter with other existing topologies.

Topology	Voltage Gain (Vo/Vin)	Voltage Stress on Switches (Vs/Vin)	Maximum Voltage Stress on Diodes (VDmax/Vin)	Maximum Voltage Stress on Output Capacitors (VCo/Vin)	S/D/I/C/T	Efficiency
[9]	$\frac{2D}{(1-D)^2}$	$S1:\frac{1D}{1-D}$, $S2:\frac{1+D}{(1-D)^2}$	$\frac{1+D}{(1-D)^2}$	NI	2/3/2/3/10	93.9%
[12]	$\frac{3}{1-D}$	$S1,\ S2:\frac{1}{1-D}$	$\frac{2}{1-D}$	$\frac{3}{1-D}$	2/2/2/3/9	95.3%
[25] (Figure 2e)	$\frac{2}{1-D}$	$\frac{1}{1-D}$	NI	$\frac{2}{1-D}$	1/3/1/3/8	92.1%
[24] (Figure 4c)	$\frac{2}{1-D}$	NI	$\frac{2}{1-D}$	NI	1/3/1/3/8	95.8%
[28]	$\frac{2+D}{(1-D)^2}$	$S1:\frac{M_{CCM}(-1+\sqrt{1+12M_{CCM}})}{6M_{CCM}+1-\sqrt{1+12M_{CCM}}}$ $S2:\frac{2M_{CCM}^2}{6M_{CCM}+1-\sqrt{1+12M_{CCM}}}$	$\frac{2M_{CCM}^2}{6M_{CCM}+1-\sqrt{1+12M_{CCM}}}$	$Co:\frac{2+D}{(1-D)^2}$ $C2,\ C3:\frac{2M_{CCM}^2}{6M_{CCM}+1-\sqrt{1+12M_{CCM}}}$	2/5/3/6/16	95.22%
[29]	$\frac{3+D_1-D_2}{(1-D_1-D_2)}$	$\frac{M_{CCM}+1}{4}$, $\frac{M_{CCM}-1}{2}$	$\frac{M_{CCM}+1}{2}$	$\frac{3+D_1-D_2}{(1-D_1-D_2)}$	3/3/2/3/10	95.8%
[30]	$\frac{3-3D_1+D^2}{1-3D_1+D^2}$	$\frac{\left(\frac{3-3D_1+D^2}{1-3D_1+D^2}\right)-1}{2}$	$\frac{3-3D_1+D^2}{1-3D_1+D^2}-1$	$\frac{\left(\frac{3-3D_1+D^2}{1-3D_1+D^2}\right)-1}{2}$	2/6/2/4/14	92.8%
[35] (Figure 38 with M = 1)	$\frac{2}{1-D}$	$\frac{1}{1-D}$	$\frac{2}{1-D}$	$\frac{1}{1-D}$	2/12/2/7/23	95.3%
[40] (Figure 1h)	$\frac{3-D}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	1/4/1/4/10	95.44%
[46] (Figure 2c)	$\frac{3-D}{1-D}$	$\frac{\frac{3-D}{1-D}-1}{2}$	$\frac{3-D}{1-D}-1$	NI	2/3/2/3/10	NI
[47] (Figure 11)	$\frac{2D}{1-D}$	NI	NI	$\frac{2D}{1-D}$	1/2/2/3/8	NI
[48] (Figure 2, n = 2)	$\frac{N}{1-D}$	NI	$\frac{1}{1-D}$	$\frac{1}{1-D}$	1/5/1/5/12	90%
[34]	$\frac{3-D}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	NI	1/4/4/1/10	96%
[39] (Figure 3)	$\frac{4}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	NI	3/9/1/7/20	97.35%
Proposed converter	$V_o=\frac{3}{1-D}-\frac{4L_rC_1\Delta V_o}{((1-D)T_S)^2}-\frac{4L_rC_1\Delta V_o}{(DT_S)^2}$	$\frac{1}{1-D}$	$\frac{1}{1-D}-\frac{2L_rC_1\Delta V_o}{((1-D)T_s)^2}-\frac{2L_rC_1\Delta V_o}{(DT_s)^2}$	$\frac{1}{1-D}-\frac{2L_rC_1\Delta V_o}{((1-D)T_s)^2}-\frac{2L_rC_1\Delta V_o}{(DT_s)^2}$	2/4/2/5/13	97.4%

With S/D/I/C/T: Switch/Diode/Coupled Inductor/Single Inductor/Capacitor/Total, N: turns ratio of coupled inductor, NI: No information.

As shown in Figure 11, the converters in (28), (29), (30), (9), (12) have higher voltage gain than the proposed topology. However, they also have their drawbacks.

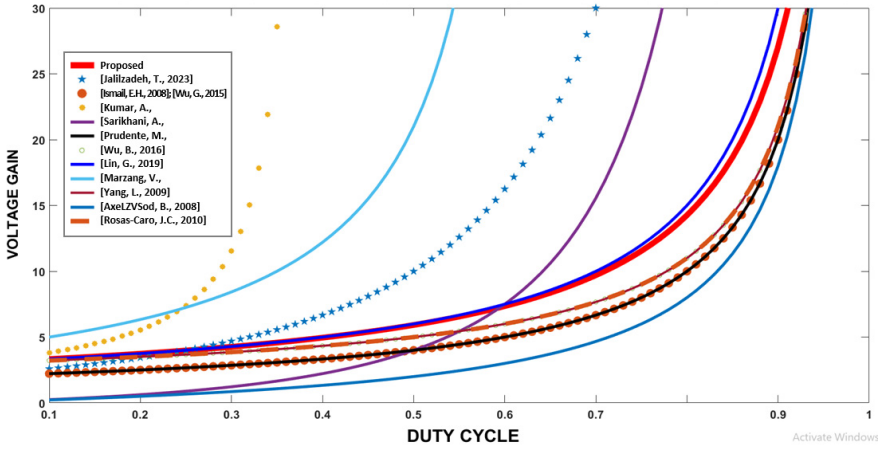

Figure 11. Voltage gain graph [Sarikhani, A., 2020 [9], Lin, G., 2019 [12], Ismail, E.H., 2008 [25] (Figure 2e), Wu, G., 2015 [26] (Figure 4c), Jalilzadeh, T., 2023 [28], Marzang, V., 2019 [29], Kumar, A., 2020 [30], Prudente, M., 2008 [35] (Figure 38), Wu, B., 2016 [40], Yang, L., 2009 [46] (Figure 2c), AxeLZVSod, B., 2008 [47], Rosas-Caro, J.C., 2010 [48] (Figure 9)].

Even though the converters in [9,12] use fewer components, the efficiency is lower due to hard switching for semiconductor components. Furthermore, the voltage stress on components on the output side is significantly high, and they both need to use two large inductors that make the volume of the circuit increase.

The converter in [28] employs three larger inductors, which results in increased volume and cost. Furthermore, the voltage stress on most components is higher compared to that in the proposed converter, and the efficiency is lower than that of our converter.

The converter in [29] utilizes three active switches and two main inductors, leading to complexity in control and an increased volume. Additionally, the voltage stress on components is higher, and the efficiency is lower compared to the proposed converter. Another significant drawback of this converter is the elevated voltage stress on components, particularly on the output-side components, compared to the proposed topology.

The converter in [30] boasts high gain with a low-duty cycle as its advantage. However, its efficiency is considerably lower compared to ours. Moreover, there is still a notable issue of high and uneven voltage stress on the components. Components near the output side, such as output diode D_O, output capacitor C_O, and capacitors C_2 and C_3, experience particularly high voltage stress.

The converter in [34] achieves a similar voltage gain and voltage stress on components (switches and diodes) with a lower component count. However, it operates with hard switching, leading to low efficiency and high volume due to the necessity of using a low switching frequency.

The converter in [39] (Figure 4) appears to achieve a higher voltage with a certain number of voltage multiplier stages compared to the proposed converter, and its efficiency is high. However, it requires the use of many components, and a low frequency is implemented since no soft switching is employed, resulting in high volume and cost. It should be noted that the proposed converter will significantly increase voltage gain by cascading more voltage doubler stages, making the design process simpler and more practical.

Figure 12 illustrates the variation in maximum voltage stress on diodes with voltage gain. The proposed converter exhibits the lowest voltage stress on diodes compared to the other converters.

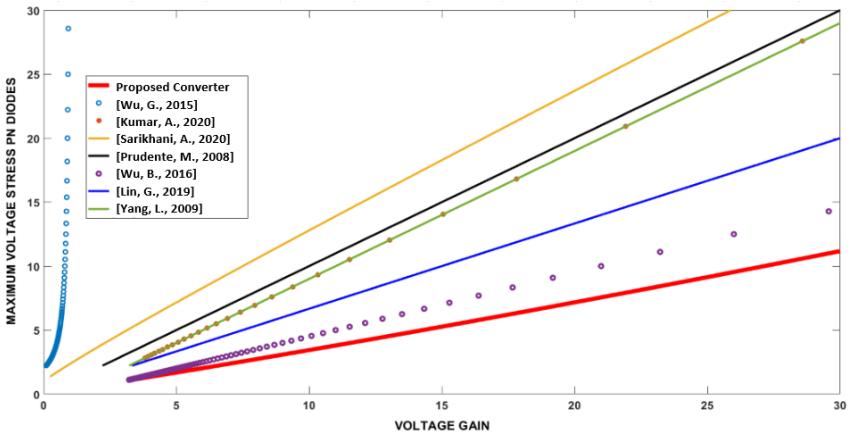

Figure 12. Maximum voltage stress on diodes graph [Sarikhani, A., 2020 [9], Lin, G., 2019 [12], Wu, G., 2015 [26], Kumar, A., 2020 [30], Prudente, M., 2008 [35], Wu, B., 2016 [40], Yang, L., 2009 [46]].

Figure 13 shows the voltage gain of the proposed converter with one, two, and three stages of the cascaded voltage doubler. It can be seen that the proposed converter can easily obtain ultra-high gain flexibly by cascading more VD stages or using higher-duty cycles.

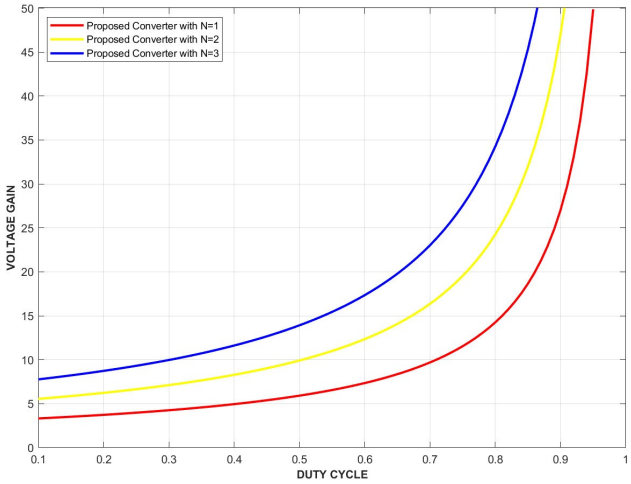

Figure 13. The proposed converter voltage gain with 1 stage, 2 stages, and 3 stages of VDs.

It is important to note that, as discussed in Part II, when cascading more VD stages, the voltage stress on components is not affected. In fact, it will be lower since the voltage stress on components only depends on the source voltage and the duty cycle. If cascading more VD stages, it could obtain a higher gain with a low-duty cycle, consequently reducing the voltage stress on components.

Figure 14 shows the accuracy of the simplified theoretical analysis in (30) in comparison to the experimental results with an input voltage of 40 V, output power of 300 W. It can be seen that the accuracy of the theoretical analysis in (30) decreases with the increase of duty cycle. This is attributed to the growing influence of parasitic components, which become more dominant at higher duty cycles.

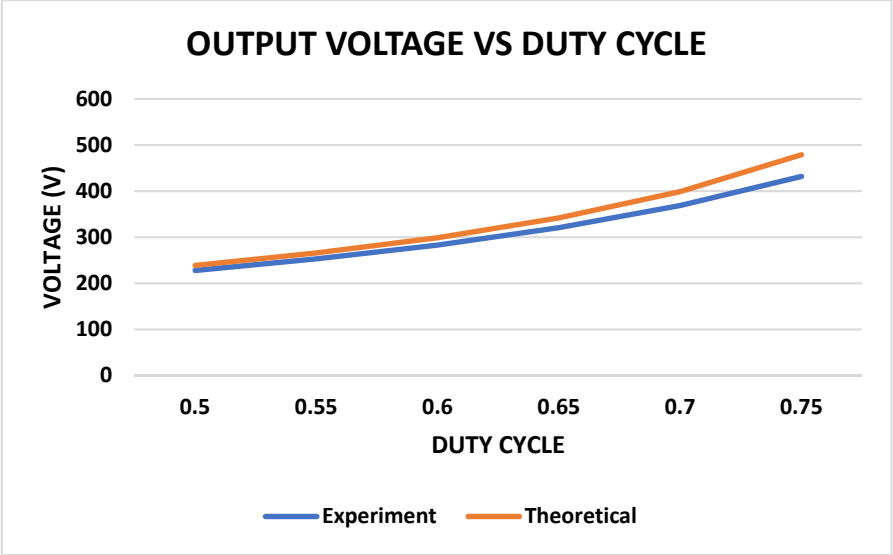

Figure 14. The output voltage comparison between theoretical and experiment.

6. Conclusions

This paper presents a non-isolated high step-up boost converter designed for low voltage stress on components and high efficiency while maintaining a high step-up voltage gain. Its effectiveness and practicality have been validated through experiments with a 360 W prototype converter. Compared to other non-isolated high voltage gain boost converters, this proposed converter achieves a relatively high voltage gain with a maximum efficiency of 97.4%. It also ensures significantly lower voltage stress on switches and passive components than other high voltage gain non-isolated converters. An added benefit is

the ability to further increase the voltage gain by simply adding more voltage doublers. However, the input and output do not share a common ground, and pulsating input current remains a disadvantage of this converter. In the future, further studies will be conducted to optimize the design, perform comprehensive analysis, and explore specific applications of the proposed converter.

This converter is ideally suited for distributed power generation systems utilizing renewable energy sources that require high voltage gain without the need for a transformer.

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