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Improved Genetic Algorithm-Based Harmonic Mitigation Control of an Asymmetrical Dual-Source 13-Level Switched-Capacitor Multilevel Inverter

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Abstract: A single-phase multilevel inverter with a switched-capacitor multilevel (SC-MLI) configuration is developed to provide 13-level output voltages. An improved genetic algorithm (GA) with adaptive mutation and crossover rates is employed to achieve robust harmonic mitigation by avoiding local optima and ensuring optimal performance. The topology introduces an SC-MLI that generates AC output voltage at desired levels using only two capacitors, two asymmetrical DC sources, one diode, and 11 switches. This allows the inverter to use fewer gate drivers and, hence, increases the power density of the converter. A significant challenge in the normal operation of SC-MLI circuits relates to the self-voltage balance of the capacitors, which easily becomes unstable, particularly at low modulation indices. The proposed design addresses this issue without the need for ancillary devices or complex control schemes, ensuring stable self-balanced operation across the entire spectrum of the modulation index. In this context, the harmonic mitigation technique optimized through GA applied in this inverter ensures low harmonic distortion, achieving a total harmonic distortion (THD) of 6.73%, thereby enhancing power quality even at low modulation indices. The performance of this SC-MLI is modeled under various loading scenarios using MATLAB/Simulink® 2023b with validation performed through an Opal-RT real-time emulator. Additionally, the inverter's overall power losses and individual switch losses, along with the efficiency, are analyzed using the simulation tool PLEXIM-PLECS. Efficiency is found to be 96.62%.

Keywords: renewable energy; SC-MLI; power quality; THD; GA; power loss analysis

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1. Introduction

Multilevel inverter (MLI) technology has advanced significantly as a result of the increasing need for dependable and efficient power conversion systems, particularly in the areas of grid integration, electric vehicle systems, and renewable energy applications [1]. MLIs have become more well known because of their ability to produce high-quality output voltage with less harmonic distortion, which makes them appropriate for contemporary power systems where system efficiency and power quality are crucial. Unlike traditional two-level inverters, MLIs produce stepped voltage waveforms that approximate sinusoidal output, minimizing the need for bulky passive filters and thus enhancing overall power quality. The increasing relevance of MLIs has driven a search for innovative topologies and control strategies that balance performance, reliability, and cost-effectiveness [2,3].

In particular, switched-capacitor-based MLIs (SC-MLIs) offer several merits, such as self-voltage-boosting and -balancing features that reduce the component count dramatically. Such merits make SC-MLIs more appealing for compact and low-cost applications. In

designing an SC-MLI, there are a number of challenges owing to the main requirement of keeping the capacitor voltages at stable levels under variable conditions for both loading and modulation. While traditional approaches require more circuitry or intricate control schemes for balancing the voltages, which further increases the cost and complication in the system, this gets worse in asymmetrical configurations where the inverter requires unequal-magnitude DC sources to achieve multiple levels of output. One challenge that remains open in the design of SC-MLIs is to ensure that capacitors maintain self-balancing over the whole range of modulation indices without auxiliary devices [4–6].

Another important aspect of MLI systems is harmonic mitigation. If left unchecked, harmonic distortion can lead to considerable power losses and overheating, and it can even lead to the eventual burning out of the connected equipment and thus the setback in efficiency and durability of the power system. Standard harmonic mitigation approaches include the SHE and PWM techniques [7]. The techniques, though effective, mostly disappoint in cases where they are applied to SC-MLIs because of the peculiar operational characteristics of such inverters. In turn, optimized harmonic mitigation strategies have become a high-intensity research area, with the objective of improvemnet in power quality with minimum total harmonic distortion (THD) in the largest operating range. This is where the GA turns out to be a very strong optimization tool in MLIs for harmonic mitigation and, with its optimal switching angles that minimize THD, can flexibly and effectively be searched. In particular, the optimization carried out with the GA turns out to be suitable for those complex topologies of MLIs, such as the SC-MLI, for which the determination of an analytical solution may result in some tediousness. The effectiveness of the proposed harmonic mitigation approach, without any compromise in the inverter efficiency and extra control complexities, is ensured via leveraging the capability of GA-based optimization. In particular, in this paper, the GA is used to fine-tune the SHM control strategy so that the inverter is able to meet a tight power-quality requirement even at low modulation indices, which have always been considered as a regime of high harmonic distortion [8].

This paper proposes an innovative 13-level single-phase asymmetrical dual-source SC-MLI with a GA-based SHM control strategy for improved harmonic performance and high efficiency. The proposed inverter topology is unique because it requires only 11 switches, two unequal DC sources, two capacitors, and one diode. Consequently, the numbers of components and gate drivers are distinctly decreased when compared to a conventional topological design. This reduction in components leads not only to a simplification in the hardware structure of the inverter but also to an increase in its power density, thus qualifying the converter for high-performance applications where space and efficiency are the critical variables. Moreover, the proposed design addresses the challenge of self-voltage balancing without ancillary devices and thus maintains the capacitor voltage within a full range of modulation indices.

The objectives of this work are threefold:

1. To present the design and operational principles of the proposed 13-level SC-MLI, detailing the role of asymmetrical DC sources and the SC-based voltage-boosting mechanism.
2. To develop and implement an improved GA-optimized SHM control technique that preserves power quality and reduces THD under a range of operating circumstances.
3. To conduct thorough simulations and real-time emulation tests in order to verify the suggested inverter's performance, including an examination of efficiency, switching losses, and harmonic performance.

The rest of this document is structured as follows. Section 2 reviews the literature on topologies of MLIs and harmonic mitigation techniques along with applications of genetic algorithms in power electronics. Section 3 describes the architecture of the proposed 13-level SC-MLI: the configuration of its components, self-voltage-balancing mechanism,

and switching strategy. The details of the proposed SHM control approach based on the genetic algorithm will be elaborated in Section 4; the optimization process and implementation of the control method for different modulation indices are given in Section 5. Efficiency and switching loss analysis is given in Section 6. Simulation and modeling of the SC-MLI are given in Section 7, with a description of the setup for real-time experimental validation and related results. Finally, Section 8 summarizes the contributions of the work by providing its shortcomings and pointing out possible further research avenues.

2. Literature Review

2.1. Existing Multilevel Inverter Topologies

Multilevel inverters (MLIs) play a crucial role in modern power systems, offering high-quality output with minimal harmonic distortion, suitable for applications like industrial systems, renewable energy, and electric vehicles. Key MLI types include the cascaded H-bridge (CHB) [9], diode-clamped or neutral-point clamped (NPC) [10], flying capacitor (FC) [11], switched capacitor (SC) [6], and modular multilevel converters (MMC) [12].

It is highly renowned for its modularity feature, as the CHB inverter connects several H-bridge cells, with each having its own DC source. Further, the stepped waveforms created by it are much nearer to sinusoidal waveforms, hence having low harmonic content [13]. Allowing this topology to be scaled in order to address high-voltage applications allows it now to need isolated DC sources and hence higher cost and complicated arrangement in compact settings. The NPC inverter realizes different levels of voltage with the help of diodes as clamping elements, ensuring smooth output with efficient operation in medium-voltage industrial applications. However, higher levels introduce more diodes, raising the complexity and thermal management accordingly [14].

The FC inverter uses capacitors for voltage sharing instead of diodes. This makes multiple levels possible without adding more DC sources but also increases the count of capacitors and control complexity. SC inverters recently have attracted popularity due to their voltage-boosting capability and self-balancing ability, suitable for compact, high-power-density designs. Compared to the traditional VSI or CSI, the SC inverter reduces the component counts but needs sophisticated control to regulate its performance under various operating conditions due to the fact that it is sensitive to switching sequences and operating conditions [15].

In a nutshell, each topology has definite advantages. Among these, the area of suitable application for particular needs consists of the following: NPC and FC topologies are suited for medium-voltage industrial applications, whereas the CHB topology is best suited for high-voltage applications. Compact applications benefit greatly from the SC inverter's high power density and reduced component count, but it requires precise management to produce the optimum results. The SC-based MLI is investigated here since this topology provides the advantages mentioned above in compact, high-power-density applications with self-balancing features. The proposed 13-level SC MLI employs a harmonic mitigation control strategy optimized by the use of a genetic algorithm, which leverages the specific characteristics of the SC inverter topology, introducing further challenges in terms of switching losses, harmonic distortion, and control complexity [15–18].

2.2. Harmonic Mitigation and Optimization Techniques in MLIs

Effective harmonic mitigation in MLIs is important because this will ensure that the obtained THD will be minimized and the quality of power is improved. It normally involves optimization of switching angles, for which many techniques were pursued with varied strengths and weaknesses. Classically, the optimization techniques are among the core approaches that were widely used in power electronics using mathematical models

of the objective functions to solve a problem. However, their applicability to complex, nonlinear MLI systems is rather limited. Gradient-based approaches include steepest descent and conjugate gradient, which work only in smooth, differentiable problems and have problems with MLIs in view of the multilevel switching sequence. Because of this complexity, convergence usually occurs within a local minimum rather than towards a global solution. The other classical approach is linear programming (LP), which, though useful in linear problems, is bound by the inability to cope with the nonlinear nature of THD in MLIs. Nonlinear programming (NLP) allows a more complex objective function but is computationally intensive, mainly for high-level inverters, where it usually converges to local optima; this further restricts usefulness in harmonic minimization [19–21].

Heuristic optimization techniques, on the other hand, are much more adaptable. Such methods use a probabilistic or nature-inspired mechanism for searching near-optimal solutions in complex landscapes and, hence, are normally fitted to highly nonlinear and multi-modal issues such as harmonic mitigation in MLIs. Particle Swarm Optimization (PSO) is an optimization method inspired by nature that models social interaction in populations to identify near-optimal solutions effectively. Although PSO is rapid and practical for real-time applications, it tends to converge prematurely in complex landscapes, hence its ineffectiveness in minimizing THD over all the switching angles. Influenced from the method of annealing in metallurgy, Simulated Annealing (SA) is a statistical optimization approach, which is employed to escape local minima and search for global optima. SA has been used to find the near-optimal switching angles in MLIs but often converges slowly and hence does not serve rapid applications such as real-time control of MLIs. The genetic algorithm (GA) is an evolutionary optimization approach involving selection, crossover, and mutation to evolve solutions over generations. It makes GA very good at finding global or near-global optima in complex solution spaces—a quality useful in harmonic optimization. Its iterative nature provides balance in exploration and exploitation, and flexibility in the definition of fitness functions in GA enables it to address several objectives simultaneously, for example, minimization of THD, along with efficiency and power density optimizations [22].

GA enjoys a number of advantages over other methods. Such a method allows flexibility in the design of objective functions, with scope for custom-designed fitness functions in multi-objective optimization related to harmonic mitigation. Given that efficiency and harmonic reduction are inextricably balanced in switched capacitor MLIs, such an algorithm will be even more relevant. It also cuts down the risk of converging into a local minimum, which is so important in MLI applications where the THD objective function is nonlinear. Its flexibility for complicated topologies, even without explicit mathematical formulations, makes it highly suitable for a range of MLI designs, including SC-MLIs, where other methods often struggle. Moreover, for real-time applications, pre-calculated switching angles can also be stored to enhance practicality in GA-based SHM strategies [23].

While there are a number of topologies and optimization techniques, most of the existing MLI topologies have their merits; due to complexity and component count, practical adoption of such topologies is very limited, apart from their high sensitivity to switching sequences. CHB and NPC inverters need a lot of switches and DC sources, which increases costs and degraded power density. SC-MLIs alleviate some of these problems; however, they also require advanced control for capacitor voltage balancing, whereas traditional harmonic mitigation techniques such as SPWM and SHE will result in considerable switching losses or may not possess the flexibility required for complex structures. While the GA indeed provides a sound framework for harmonic mitigation, its computational burden, especially in high-level MLIs where many switching angles should be optimized, is prohibitive. Real-time applications require faster responses, and GAs can get stuck in a local

optimum without careful tuning of parameters such as population size and mutation rate, generally requiring skilled optimization to obtain reliable results [7,8].

Current approaches suffer from a number of serious limitations that, once improved, could bring much better solutions by merging advanced topologies with optimized control strategies. In addition, the design of SC-MLI should be able to achieve self-voltage balancing for a wide range of modulation indices without auxiliary devices. Moreover, the implementation of advanced harmonic mitigation strategies using the GA or any other evolutionary algorithm has to be introduced to attain high-quality output without heavy computational burden. The 13-level asymmetrical SC-MLI proposed here utilizes a GA-optimized SHM control strategy that is capable of fully meeting these needs and hence provides a holistic approach toward harmonic mitigation, efficiency, and system stability in MLI applications.

3. Proposed SC-MLI Design

SC-MLIs have begun to attract more attention because they can provide higher voltage levels with fewer components, and an increase in the power density and efficiency can be achieved while simultaneously reducing the overall cost of the system. The capacitors of SC-MLIs can easily switch between charging or discharging states. Hence, a self-balancing mechanism would help them maintain their voltages without any additional effort of control. This makes SC-MLIs applicable to renewable energy applications where compact and efficient inverters are critical.

3.1. Architecture of the 13-Level Asymmetrical Dual-Source SC-MLI

In the proposed 13-level SC-MLI, there is an asymmetrical configuration which uses a different DC supply, V_{DC1} and V_{DC2}, where $V_{DC2} = 3V_{DC1}$ as presented in Figure 1. Eleven switches, two capacitors, and two uneven DC sources are used in this setup to provide thirteen distinct voltage levels. The output maximum voltage $V_{o,\max}$ is given by:

$$V_{o,\max} = 6V_{DC1} \tag{1}$$

The topology achieves a voltage gain (VG) of 1.5, calculated as:

$$VG = \frac{V_{o,\max}}{V_{DC1} + V_{DC2}} = \frac{6V_{DC1}}{4V_{DC1}} = 1.5 \tag{2}$$

This asymmetrical arrangement provides a higher number of output levels with fewer components, enhancing both power density and efficiency.

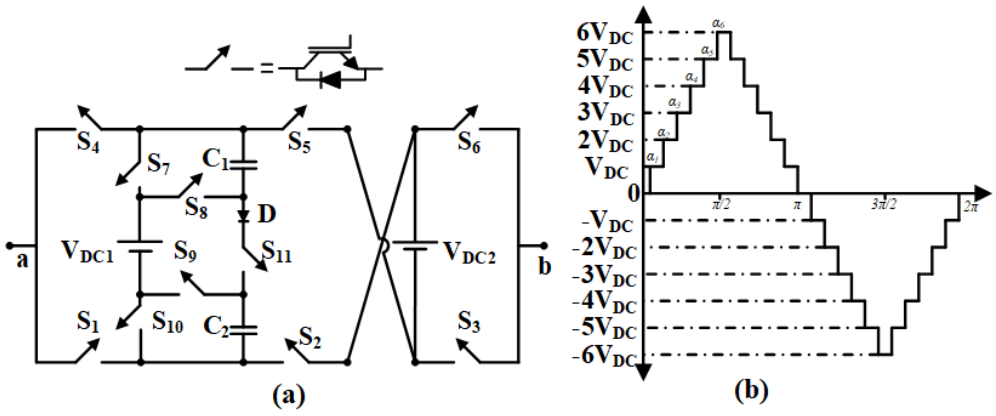


Figure 1. Thirteen-level SC-MLI: (**a**) circuit topology and (**b**) output voltage waveform.

3.2. Components and Configuration

The SC-MLI uses two capacitors, C_1 and C_2, with charging and discharging cycles that vary across switching states. Each state produces a unique output voltage level by controlling specific switches, thus contributing to the overall 13-level output.

Switching States

The inverter operates in 13 switching states, labeled L_1 through L_{13} as shown Table 1. Each state activates specific switches and manages the capacitor charging, along with discharging C_1 and C_2, shown in Figure 2 as follows:

- **State** L_1: Switches $S_2, S_4, S_6, S_7, S_{10}$ are ON, generating an output of V_{DC1}. No capacitor charging or discharging occurs.
- **State** L_2: Switches $S_2, S_4, S_6, S_7, S_9, S_{11}$ are ON, producing an output of $2V_{DC1}$. Capacitor C_1 charges while C_2 discharges.
- **State** L_3: Switches $S_1, S_2, S_3, S_8, S_{10}, S_{11}$ are ON, resulting in $3V_{DC1}$. C_2 charges while C_1 remains uncharged.
- **State** L_4: Switches $S_2, S_3, S_4, S_7, S_{10}$ are ON, generating $4V_{DC1}$. No capacitor charging or discharging occurs.
- **State** L_5: Switches $S_2, S_3, S_4, S_7, S_9, S_{11}$ are ON, with an output of $5V_{DC1}$. C_1 charges while C_2 discharges.
- **State** L_6: Switches S_2, S_3, S_4, S_8, S_9 are ON, yielding $6V_{DC1}$, with both C_1 and C_2 discharging.
- **State** L_7: Switches $S_1, S_2, S_6, S_8, S_{10}, S_{11}$ are ON, resulting in zero output voltage, and C_1 charges.

Table 1. Switching states and capacitor behavior for the 13-level SC−MLI, highlighting charging, discharging, and output voltage levels.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	C_1	C_2	V_{ab}	Level
0	1	0	1	0	1	1	0	0	1	0	-	-	V_{DC}	L_1
0	1	0	1	0	1	1	0	1	0	1	↑	↓	$2V_{DC}$	L_2
1	1	1	0	0	0	0	1	0	1	1	-	↑	$3V_{DC}$	L_3
0	1	1	1	0	0	1	0	0	1	0	-	-	$4V_{DC}$	L_4
0	1	1	1	0	0	1	0	1	0	1	↑	↓	$5V_{DC}$	L_5
0	1	1	1	0	0	0	1	1	0	0	↓	↓	$6V_{DC}$	L_6
1	1	0	0	0	1	0	1	0	1	1	-	↑	zero	L_7
1	0	1	0	1	0	1	0	0	1	0	-	-	$-V_{DC}$	L_8
1	0	1	0	1	0	0	1	0	1	1	↓	↑	$-2V_{DC}$	L_9
0	0	0	1	1	1	1	0	1	0	1	↑	-	$-3V_{DC}$	L_{10}
1	0	0	0	1	1	1	0	0	1	0	-	-	$-4V_{DC}$	L_{11}
1	0	0	0	1	1	0	1	0	1	1	↓	↑	$-5V_{DC}$	L_{12}
1	0	0	0	1	1	0	1	1	0	0	↓	↓	$-6V_{DC}$	L_{13}

(where "↑"—charging, "↓"—discharging, and "-"—no change).

For the negative half-cycle (states L_8 through L_{13}), the switching sequence mirrors the positive half-cycle, but with opposite polarities:

- **State** L_8: Switches $S_2, S_4, S_5, S_7, S_{11}$ are ON, generating $-V_{DC1}$. Capacitors remain unchanged.
- **State** L_9: Switches $S_2, S_4, S_5, S_7, S_9, S_{12}$ are ON, yielding $-2V_{DC1}$. C_1 charges, while C_2 discharges.
- **State** L_{10}: Switches $S_1, S_3, S_4, S_8, S_{11}, S_{12}$ are ON, producing $-3V_{DC1}$ with C_2 charging.
- **State** L_{11}: Switches $S_2, S_3, S_5, S_7, S_{11}$ are ON, resulting in $-4V_{DC1}$, with no capacitor change.

- **State** L_{12}: Switches $S_2, S_3, S_5, S_7, S_9, S_{12}$ are ON, yielding $-5V_{DC1}$, with C_1 charging and C_2 discharging.
- **State** L_{13}: Switches S_2, S_3, S_5, S_8, S_9 are ON, resulting in $-6V_{DC1}$, with both C_1 and C_2 discharging.

This systematic switching enables the generation of 13 levels and ensures the optimal charging and discharging of capacitors.

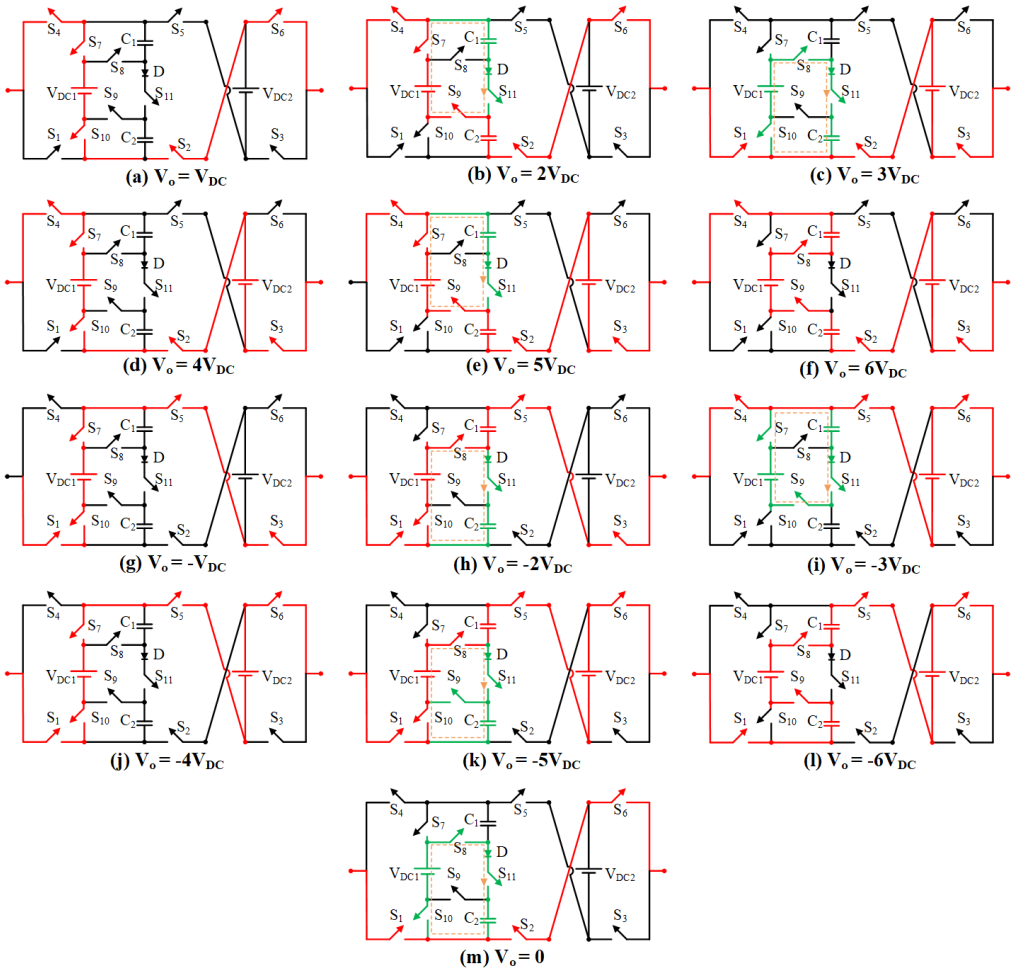


Figure 2. Conduction states of 13-level SC-MLI: (**a**–**f**) positive levels, (**g**–**l**) negative levels, and (**m**) zero voltage state

3.3. Self-Voltage Balancing Mechanism for Capacitors

Self-voltage balancing in SC-MLIs is achieved by the natural charging along with discharging cycles of C_1 and C_2 due to properly designing the topology, as shown in Figure 3. The switching states are designed to maintain capacitor voltage balance without external circuits, even at low modulation indices. This ensures consistent output voltage stability across different load conditions, supporting stable power delivery across the inverter's entire operating range. In Section 7, the self-voltage mechanism is verified by simulating at various fixed and changing states of load and modulation index.

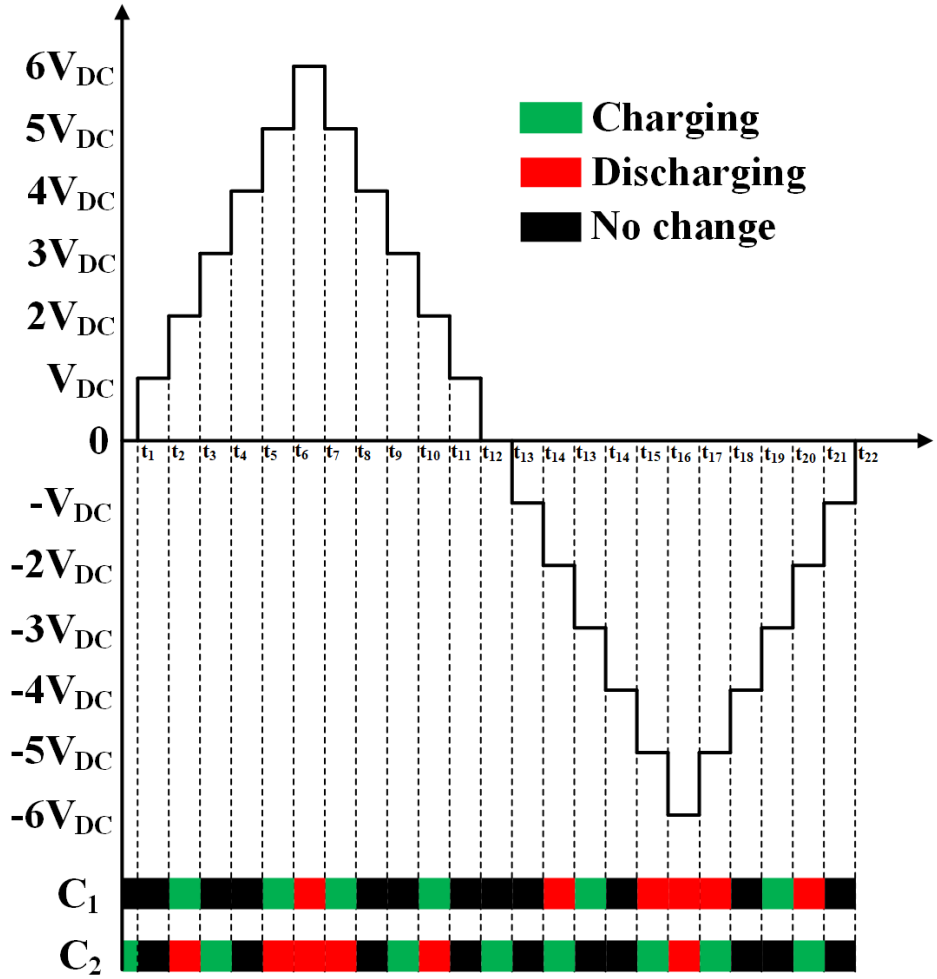


Figure 3. Capacitor states at each level.

3.4. Comparative Study

To demonstrate its superiority over other topologies, the suggested SC-MLI is contrasted with previously reported MLI topologies. Table 2 offers a thorough comparison analysis and is arranged as follows: The converter's cost factor (C_F), output voltage levels (N_L), power switch count (N_{SW}), total standing voltage (TSV), capacitor count (N_C), voltage gain (V_G), diode count (N_D), output voltage level-to-power switch ratio (N_L/N_{SW}), gate driver circuit count (N_{GD}), voltage boosting (V_B), and number of sources (V_S).

Table 2. Comparison of performance metrics for 13-level SC-MLI topologies.

Topology	N_L	N_{SW}	N_L/N_{SW}	N_S/N_L	N_C	V_G	V_B	N_D	N_{GD}	N_S	TSV_{PU}	CF
[8]	13	14	0.93	0.07	3	6	6	1	14	1	5.66	2.67
[24]	13	18	0.72	0.07	6	2	4	6	9	3	8.00	3.58
[25]	13	13	1.00	0.07	2	1.5	6	0	9	2	5.66	4.77
[26]	13	14	0.93	0.07	4	3	6	2	14	2	5.66	7.81
[27]	13	16	0.81	0.07	4	3	4	4	8	2	9.00	5.38
[28]	13	10	1.30	0.07	1	2	6	1	9	2	6.50	4.57
[29]	13	10	1.30	0.07	5	6	6	10	10	1	5.66	5.82
[30]	13	12	1.08	0.07	3	6	6	4	13	1	6.00	2.83
[31]	13	11	1.18	0.07	4	2	4	4	11	2	8.00	5.85
[32]	13	13	1.00	0.07	4	1.25	6	4	13	2	5.33	7.20
P	13	11	1.18	0.07	2	1.5	6	1	11	2	5.16	4.55

All of the voltage peaks at which a power diode or power switch becomes operational are added up to form the total standing voltage (TSV). The sum of the maximum voltages

that each power diode and power switch might potentially block is what it is known as mathematically. The TSV can be computed using the formula in (3)

$$\text{TSV} = \sum_{N_{\text{sw}}} V_{\text{sw,max}} + \sum_{N_D} V_{D,\text{max}} = 31V_{\text{DC}} \tag{3}$$

where the peak blocking voltages of the power electronic switch and diode are $V_{\text{sw,max}}$ and $V_{\text{D,max}}$, respectively. The comparison of TSV with the greatest voltage value ($V_{\text{o,max}}$) can be used to evaluate the TSV per unit (TSV_{PU}), which is then computed utilizing (4) in the way described below.

$$\text{TSV}_{PU} = \frac{\text{TSV}}{V_{\text{o,max}}} = \frac{31V_{DC}}{6V_{DC}} = 5.16 \tag{4}$$

An MLI topology's cost function (*CF*) often provides an approximation of its implementation feasibility. The following method can be used to calculate *CF* using (5):

$$CF = \frac{N_s(N_{SW} + N_D + N_{GD} + N_C + TSV_{PU})}{N_L} \tag{5}$$

The proposed topology "P" excels in several areas when compared to other topologies. It achieves a voltage boost (V_B) of 6, which is among the highest values in the comparison and comparable to topologies like [29,30]. The voltage gain is decent, along with high voltage boost applicability for boost signal topologies. A cost factor of 2.67 was derived for the proposed configuration, which is far less than many other topologies reported in [31,32], where the values of CF are 5.85 and 7.20, respectively. It can also be derived from the above interpretation that the proposed topology is more economical, offering similar or better performance at lower costs [33].

Furthermore, the ratio of output voltage levels with respect to the power switch count N_L/N_{SW} also reaches 0.93 and is hence competitive and reflecting an effective utilization of the power switches. That gives good enough agreement with [26] and [30], proving effective to reach higher numbers of levels for a limited switch count. Further, the proposed topology gives a TSV_{PU} of 5.16, thus ensuring a good balance in the design such that the stress on each of the components will be reduced in order to enhance both reliability and lifetime. The proposed configuration optimizes (N_{GD}) and (N_S) at 11 and 2, respectively, showing much emphasis on its efficiency and applicability in real-world applications.

Other competitive metrics are also introduced by topologies such as [24,28,29]. For example, ref. [29] achieves the high ratio of N_L/N_{SW}, which is 1.30, indicating the effective utilization of power switches, but it may face difficulties in applications requiring higher capacitance since it has zero capacitors (N_C). Refs. [24,25] have the same number of levels (N_L), but they are different with respect to other metrics such as N_{SW} and CF, which reflects a difference in design priorities and performance.

In summary, the proposed topology "P" offers a well-rounded and superior solution for SC-MLI applications, balancing high performance with cost-effectiveness and reliability. By optimizing key parameters, it stands out among the compared topologies as a versatile and practical choice for modern power electronics applications. The choice of the proposed topology was based on a balanced evaluation of all critical parameters rather than focusing solely on the CF. While its CF value is competitive, the topology excels in other key performance metrics, such as lower component count, superior voltage boosting capability, and reduced total standing voltage. These features make it a robust and practical choice for real-world applications requiring compact and efficient power conversion systems.

4. Control Strategy for Harmonic Mitigation

Figure 1b illustrates how the output voltage of the 13-level SC-MLI can be expressed as

$$V(t) = V_{DC}\left[\sum_{i=1}^{6} u(t-\alpha_i) - \sum_{i=1}^{6} u(t-(\pi-\alpha_i)) - \sum_{i=1}^{6} u(t-(\pi+\alpha_i)) + \sum_{i=1}^{6} u(t-(2\pi+\alpha_i))\right] \quad (6)$$

where $u(t-\alpha_i) = \begin{cases} 1 & \text{for } t \geq \alpha_i \\ 0 & \text{for } t < \alpha_i \end{cases}$ such that α_i are the switching angles. The multilevel inverter's waveform creation is controlled by this unit step function, which explains how every stage of the final voltage waveform is turned on or off at particular periods α_i. A multilayer inverter's output voltage waveform is symmetric and periodic, making it possible to depict it as a Fourier series. When there are only odd harmonics in a signal with quarter-wave uniformity, it can be written as:

$$V_n = \frac{2}{T_o}\int_0^{t_0} V(t)\sin(n\omega_o t)\,dt \quad \forall n = 1,3,5,\ldots \quad (7)$$

By replacing (6) with $V(t)$ in (7), the following equation can be produced.

$$V_n = \frac{4}{n\pi}\left[\sum_{i=1}^{6} V_{DC}\cos(n\alpha_k)\right] \quad \forall n = 1,3,5,\ldots \quad (8)$$

$$\text{where } 0 < \alpha_1 < \alpha_2 < \alpha_3 < \ldots < \alpha_6 < \frac{\pi}{2}$$

$$\text{THD} = \sqrt{\frac{\sum_{n=3,5,\ldots}^{\infty}\left[\frac{4V_{DC}}{n\pi}\sum_{k=1}^{6}\cos(n\alpha_k)\right]}{\left(\frac{4V_{DC}}{\pi}\sum_{k=1}^{6}\cos(\alpha_k)\right)}} \quad (9)$$

For an inverter with six switching angles $\alpha_1, \alpha_2, \ldots, \alpha_6$, the harmonic components of the output voltage $V(t)$ can be written as:

$$V_n = \frac{4V_{DC}}{\pi}\sum_{k=1}^{6}\cos(n\alpha_k) \quad (10)$$

where: V_{DC} is the *DC* source voltage, n represents the harmonic order (e.g., 1, 3, 5, etc.), α_k are the switching angles, with $0 < \alpha_1 < \alpha_2 < \ldots < \alpha_6 < \frac{\pi}{2}$.

4.1. Objective of Harmonic Mitigation

The primary objective of harmonic mitigation is to determine the switching angles $\alpha_1, \alpha_2, \ldots, \alpha_6$ such that:

1. The fundamental component V_1 is maintained at a specified reference value V_{ref};
2. The 3rd, 5th, 7th, 9th, and 11th harmonics are minimized.

4.2. Formulating the Harmonic Equations

The harmonic equations for selective harmonic mitigation (SHM) can be formulated as follows:

1. Fundamental Component Equation:

$$V_1 = \frac{4V_{DC}}{\pi}\sum_{k=1}^{6}\cos(\alpha_k) = V_{ref} \quad (11)$$

2. Harmonic Component Equations for Mitigation: To minimize the 3rd, 5th, 7th, 9th, and 11th harmonics, we set their components to zero:

$$V_3 = \frac{4V_{DC}}{\pi}(\cos(3\alpha_1) + \cos(3\alpha_2) + \cos(3\alpha_3) + \cos(3\alpha_4) + \cos(3\alpha_5) + \cos(3\alpha_6)) = 0 \quad (12)$$

$$V_5 = \frac{4V_{DC}}{\pi}(\cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) + \cos(5\alpha_4) + \cos(5\alpha_5) + \cos(5\alpha_6)) = 0 \quad (13)$$

$$V_7 = \frac{4V_{DC}}{\pi}(\cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) + \cos(7\alpha_4) + \cos(7\alpha_5) + \cos(7\alpha_6)) = 0 \quad (14)$$

$$V_9 = \frac{4V_{DC}}{\pi}(\cos(9\alpha_1) + \cos(9\alpha_2) + \cos(9\alpha_3) + \cos(9\alpha_4) + \cos(9\alpha_5) + \cos(9\alpha_6)) = 0 \quad (15)$$

$$V_{11} = \frac{4V_{DC}}{\pi}(\cos(11\alpha_1) + \cos(11\alpha_2) + \cos(11\alpha_3) + \cos(11\alpha_4) + \cos(11\alpha_5) + \cos(11\alpha_6)) = 0 \quad (16)$$

The nonlinear system formed by Equations (11)–(16) must be solved in order to determine the ideal switching angles $\alpha_1, \alpha_2, \ldots, \alpha_6$ that produce the required harmonic profile.

4.3. Defining the Cost Function for Harmonic Mitigation

Reducing the amplitudes of the chosen harmonics and minimizing the fundamental component's deviation from its reference are the goals of the cost function F for harmonic mitigation [7,8]. It can be described as:

$$F(\alpha_1, \alpha_2, \ldots, \alpha_6) = \left|V_1 - V_{ref}\right| + w_3|V_3| + w_5|V_5| + w_7|V_7| + w_9|V_9| + w_{11}|V_{11}| \quad (17)$$

where:

- V_1, V_3, V_5, V_7, V_9, and V_{11} are the amplitudes of the fundamental, 3rd, 5th, 7th, 9th, and 11th harmonics, respectively;
- w_3, w_5, w_7, w_9, and w_{11} are weighting factors that determine the importance of each harmonic in the cost function.

Reducing $F(\alpha_1, \alpha_2, \ldots, \alpha_6)$ is the goal in order to obtain the fundamental reference value and eliminate undesired harmonics. The determination of the weighting factors in Equation (17) is crucial for balancing the trade-offs among the various harmonics and the fundamental voltage component in the cost function, along with computation burden. In this work, the weighting factors were determined empirically based on certain considerations. First, the fundamental voltage component (V_1) is assigned the highest priority to ensure that the inverter meets the required output voltage specification, giving its associated term in the cost function the greatest emphasis. Among the harmonics, the lower-order harmonics (3rd, 5th, and 7th) are weighted more heavily than the higher-order harmonics (9th and 11th) because lower-order harmonics tend to have a more significant impact on power quality. Additionally, the weighting factors are chosen to comply with the IEEE-519 harmonic standards, which dictate that the total harmonic distortion (THD) should remain below 8% and individual harmonics should be below 5%. These standards guided the prioritization and relative importance of each harmonic term in the cost function. Based on these criteria, the values of the weighting factors used in this work are $w_3 = 1.0$, $w_5 = 0.8$, $w_7 = 0.6$, $w_9 = 0.4$, and $w_{11} = 0.2$. These values were selected to strike a balance between harmonic mitigation and computational efficiency while ensuring compliance with the harmonic standards. The empirical determination of the weighting factors ensures flexibility and adaptability for various applications. This method allows the cost function to be fine-tuned for specific performance objectives, such as optimizing power quality or balancing trade-offs in real-world implementations.

5. Proposed Improved Genetic Algorithm (GA) for Harmonic Mitigation

The optimal switching angles $\alpha_1, \alpha_2, \ldots, \alpha_6$ will be determined by using the GA to provide the minimum value of the cost function F. The use of the GA is justified because the harmonic equations will create nonlinear and complex relations [7,8].

5.1. GA Initialization and Setup

1. Initialization of the Population: Create a starting population of chromosomes, each of which has six switching angles $[\alpha_1, \alpha_2, \ldots, \alpha_6]$ that indicate potential solutions.
2. Population Size: Define the size of the population, typically between 50 and 100, based on computational resources and the desired accuracy.
3. Selection Criteria: Select chromosomes based on their fitness, with higher fitness corresponding to lower values of the cost function.

5.2. Fitness Function

The fitness function for each chromosome is derived from the cost function F defined in Equation (17):

$$\text{Fitness} = \frac{1}{1 + F(\alpha_1, \alpha_2, \ldots, \alpha_6)} \tag{18}$$

Chromosomes with higher fitness values are more likely to be selected for reproduction.

5.3. Improved GA Steps

Figure 4 demonstrates the same angles as mentioned in (11)–(16). The other steps required to properly implement the GA are as follows.

1. Selection: Using a selection technique such as a roulette wheel or tournament selection, two parents are chosen based on the fitness values of their parent chromosomes. In this art, parents are chosen using a roulette wheel. The solution space is investigated as thoroughly as feasible by choosing parents at random.
2. Adaptive Crossover and Mutation: Crossover is performed by combining pairs of parent chromosomes to produce offspring as shown in Figure 4a. A single-point crossover may be used, where a crossover point is chosen randomly, and portions of the parents' chromosomes are swapped to create offspring.
   For example, given parents:

$$\text{Parent 1} = [\alpha_1^A, \alpha_2^A, \alpha_3^A, \alpha_4^A, \alpha_5^A, \alpha_6^A] \tag{19}$$

$$\text{Parent 2} = [\alpha_1^B, \alpha_2^B, \alpha_3^B, \alpha_4^B, \alpha_5^B, \alpha_6^B] \tag{20}$$

   The offspring after crossover could be:

$$\text{Offspring 1} = [\alpha_1^A, \alpha_2^A, \alpha_3^B, \alpha_4^B, \alpha_5^A, \alpha_6^A] \tag{21}$$

$$\text{Offspring 2} = [\alpha_1^B, \alpha_2^B, \alpha_3^A, \alpha_4^A, \alpha_5^B, \alpha_6^B] \tag{22}$$

   Mutation: Random changes are introduced to some chromosomes to maintain diversity, as shown in Figure 4b. For example, a small perturbation might be added to a randomly selected angle α_i in an offspring chromosome. Furthermore, it is prohibited to alter the entire child population.
   In this adaptive GA approach for selective harmonic mitigation in multilevel inverters, we aim to optimize switching angles $\alpha_1, \alpha_2, \ldots, \alpha_6$ to achieve minimal Total Harmonic Distortion (THD). By dynamically adjusting mutation and crossover rates based on population diversity and fitness variance, the GA can effectively navigate the search space and improve convergence. First, an estimate of diversity is computed, typically

in the form of average Hamming distance D_H or fitness variance σ^2, which returns the spread of the population. We then set the mutation rate adaptively, $m(t)$, based on this measure, allowing for higher mutation rates when the population is less diverse in hope of escaping local optima and promoting exploration.
The mutation rate $m(t)$ is defined as

$$m(t) = [m_{\min} + (m_{\max} - m_{\min})\left(1 - \frac{D_H}{D_{H,0}}\right)] \tag{23}$$

where $D_{H,0}$ is the starting diversity and $m_{\min}$ and $m_{\max}$ are the minimum and maximum mutation rates, respectively.
To concentrate on fine-tuning, the crossover rate $c(t)$ is also decreased over generations, described by

$$c(t) = [c_{\min} + (c_{\max} - c_{\min}) \cdot \exp(-\alpha \cdot t)] \tag{24}$$

This expression permits high crossover rates initially for broad exploration, tapers down gradually, and emphasizes exploitation as the algorithm converges. By balancing the two adaptive ways, exploration and exploitation, the GA strikes a very effective balance and iteratively modifies the angles $\alpha_1, \alpha_2, \ldots, \alpha_6$ for minimum THD. Each generation refines the values of angles that allow a reduction in harmonic distortion, thus providing a robust solution for multilevel inverter applications. It, at the same time, optimizes computational effort while minimizing THD, thus making the approach suitable for real-time harmonic mitigation in a power system.

3. Evaluation: The cost function is used to determine each new chromosome's fitness.
4. Replacement: Replace the old generation with the new generation by replacing chromosomes based on their relative fitness. Repeat until a stopping criterion is reached.

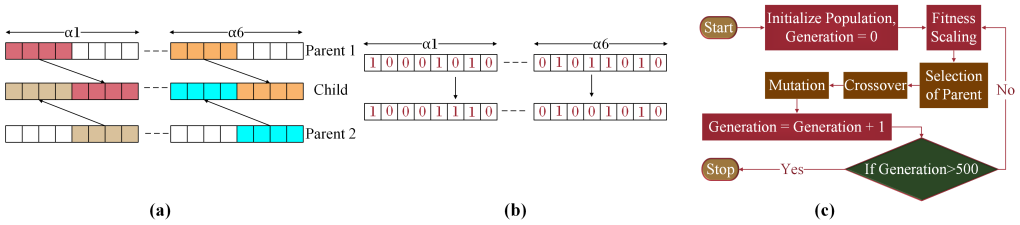


Figure 4. GA: (**a**) Crossover. (**b**) Mutation. (**c**) Flowchart.

5.4. Solving for Optimal Switching Angles

Optimizing using the technique of the GA gives the values of $\alpha_1, \alpha_2, \ldots, \alpha_6$, which minimizes the cost function F from Equation (17). In fact, this solution actually gives the switching angles to obtain the desired fundamental voltage V_{ref} with the elimination of the 3rd, 5th, 7th, 9th, and 11th harmonics.

5.5. Methodology

The initial population in the GA methodology consists of a set of possible solutions generated and then evaluated by means of the so-called fitness function that computes the suitability of the solution for the problem at hand. Based on computed fitness, the population is sorted in descending order, where the fittest are selected to reproduce. It generates new offspring using crossover and mutation operators, which are devised to explore the wide solution space while retaining and refining the characteristics of the superior solutions. This is followed by a selection process in which some of the best-fit individuals within the new generation retain a few from the original population and newly

generated offspring. This is an iterative process, continuing for a number of generations specified or until a convergence criterion is attained.

In the particular application discussed, the GA is applied to an optimization problem concerning switching angles in multilevel inverter applications, minimizing the THD for different modulation indices. Here, switching angles (denoted as $\alpha_1, \alpha_2, \alpha_3, \ldots, \alpha_6$) are optimized across varying modulation indices. For comprehensive analysis, a 3D surface plot as shown in Figure 5 can be utilized to visualize the relationship among THD, modulation index (m), and each individual switching angle $\alpha_1, \alpha_2, \ldots, \alpha_6$. This plot provides insights into how variations in modulation index and each switching angle affect the THD, offering a clear representation of the optimal angle configurations that minimize THD across different operational conditions.

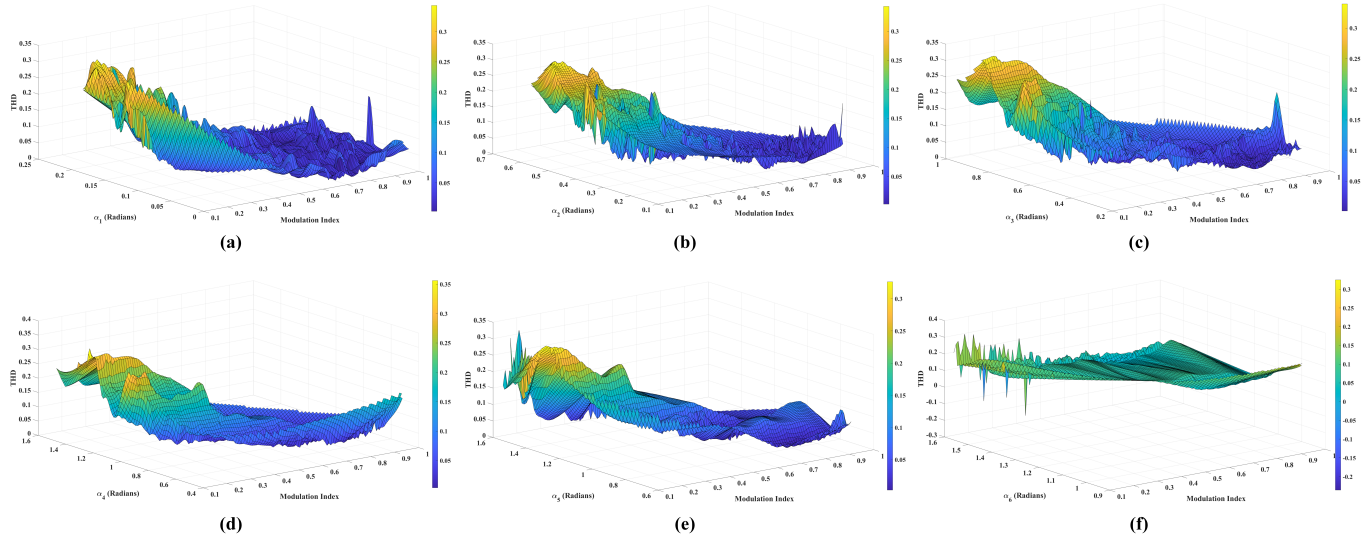


Figure 5. Variation in corresponding THD and modulation index with different switching angles: (**a**) α_1; (**b**) α_2; (**c**) α_3; (**d**) α_4; (**e**) α_5; (**f**) α_6.

6. Power Loss Analysis

There are three main categories of power loss: switch loss, forward conduction loss, and capacitor ripple loss. After the theoretical study of loss, which is detailed in depth by the authors of [7], an analysis of power loss is carried out using PLEXIM-PLECS 4.6.9 software.

The efficiency computation and total loss analysis for the suggested 13-level SC-MLI are performed using the PLECS 4.6.9 software and the Infineon IKW40N65ES5IGBT and IKW40N65ES5Diode models [34], and their turn-on and-off and conductance loss characteristics are shown in Figure 6a, Figure 6b, and Figure 6c, respectively. Figure 6d shows the junction temperature profiles of the power switches and diode under dynamic operation. Figure 6e displays efficiency and loss at various loads. Monitoring junction temperature ensures that the components remain within safe thermal limits, preventing overheating and ensuring reliable operation. With a surrounding temperature of 25 °C, the maximum efficiency of the proposed topology is determined to be 96.62% at a load of 70 W, as seen in Figure 6f. Also, the power loss distribution across various component of the topology is presented in Figure 6g. The total losses of switched-capacitor MLIs can be divided into three categories: switching loss from the switching transition, conduction loss from conductivity, and capacitor voltage ripple loss.

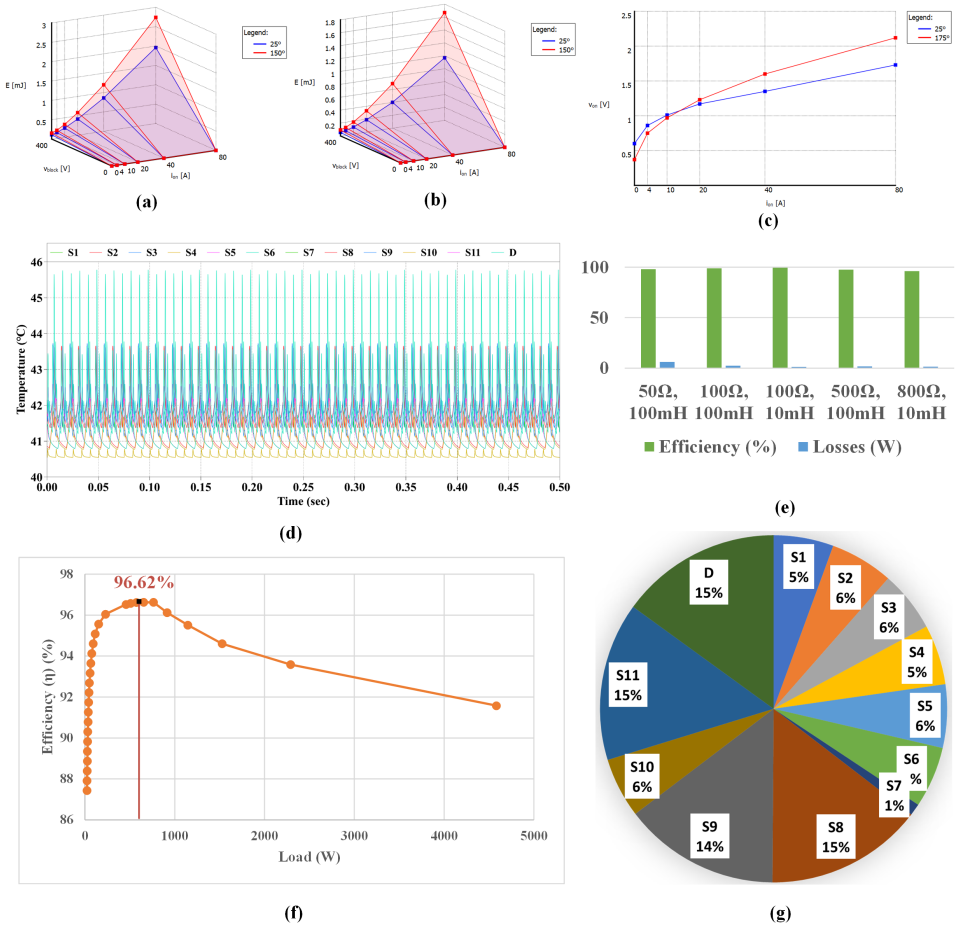


Figure 6. Detailed loss and performance characteristics of SC-MLI inverter: (**a**) IGBT turn-on energy losses, (**b**) IGBT turn-off energy losses, (**c**) conduction losses in IGBTs, (**d**) thermal profiles of switches and diodes at 25 °C ambient temperature, (**e**) comparison of efficiency and losses across different load conditions, (**f**) efficiency variation with load, and (**g**) distribution of power losses among switches and diodes.

6.1. Switching Losses

Switching losses occur in power semiconductor devices when they transition from an on to an off state and vice versa. These slow changes, which involve non-zero voltage and current during the switching phase, lead to power dissipation. There is a power loss when turning things on and off. The loss of power for a single switch-on can be summed up as follows:

$$P_{\text{sw\_on}} = \int_0^{t_{\text{on}}} v(t)i(t)\,dt \tag{25}$$

Likewise with the turning off of switches:

$$P_{\text{sw\_off}} = \int_0^{t_{\text{off}}} v(t)i(t)\,dt \tag{26}$$

After accounting for switching losses in Equations (25) and (26) during turning on and off, the following is obtained:

$$P_{\text{sw,on}} = \frac{V_{\text{sw}} \cdot I_{\text{on}}}{6} \tag{27}$$

$$P_{\text{sw,off}} = \frac{V_{\text{sw}} \cdot I_{\text{off}}}{6} \tag{28}$$

Similar to this, V_{sw} is the voltage across the switch, $I_{t_{on}}$ and $I_{t_{off}}$ are the currents flowing through it when it is turned on and off, respectively, and t_{on} and t_{off} are the times at which it is turned on and off, respectively. P is equivalent to the switching loss for one whole switching cycle.

$$P_{sw,inverter} = \frac{V_{sw} \times (I_{t_{on}} + I_{t_{off}})}{6} \tag{29}$$

6.2. Conduction Losses

Conductivity causes switches and diodes to lose energy. Since switches are the only components of circuits, any switch's conduction losses are

$$P_{cond,inverter} = [V_s + R_s i^{\gamma}(t)]i(t) \tag{30}$$

V_s represents the voltage drop across the power switch, R_s the switch's resistance, and γ a value specified by the switch's specs. The estimation of the overall conduction loss depends on the following calculation:

$$P_{cond,inverter} = \frac{1}{T}\int_0^{2\pi} \sum_{i=1}^{N_{switch}} P_{ci}(t)\, dt \tag{31}$$

6.3. Capacitor Voltage Ripple Losses

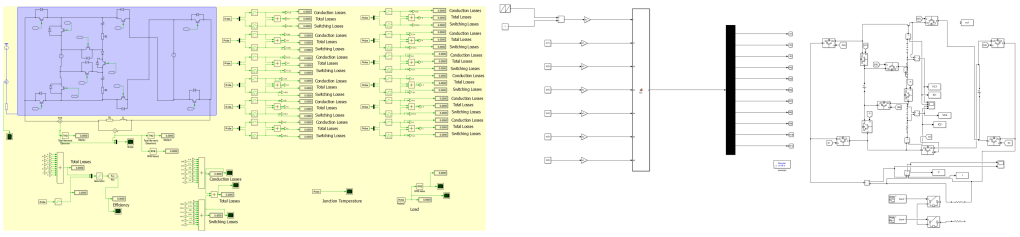
Capacitors have their own non-zero internal resistance, which is equivalent series resistance (ESR). Due to this ESR, the losses in a capacitor have a value that is non-zero at steady state. This ESR causes a voltage drop Δv_c in the SC-MLI output voltage waveform, which causes ripple power losses (P_{ripple}) in a capacitor. A capacitor's ripple losses, $P_{ripple,inverter}$, are calculated as follows:

$$P_{ripple,inverter} = \frac{f_{sw} C (\Delta v_c)^2}{2} \tag{32}$$

Consequently, the converter will experience a complete loss of

$$P_{loss,inverter} = P_{sw,inverter} + P_{cond,inverter} + P_{ripple,inverter} \tag{33}$$

In summary, the power loss analysis demonstrates that the proposed 13-level SC-MLI achieves a balance between switching, conduction, and capacitor voltage ripple losses. The use of PLECS software and validated semiconductor models as shown in Figure 7a ensures accurate loss computations, supporting the reported maximum efficiency of 96.62% as shown in Figure 6f. These findings confirm the topology's ability to maintain high efficiency under various load conditions while minimizing thermal stress, as indicated by the junction temperature profiles. This efficient loss management, combined with voltage boosting capability, highlights the SC-MLI's potential for reliable and sustainable microgrid applications.



(a) (b)

Figure 7. Snapshot of working model from (**a**) PLEXIM-PLECS and (**b**) MATLAB/Simulink.

7. Results and Discussion

Here, asymmetrical DC power sources are employed to simulate the proposed design using MATLAB/Simulink 2023b. Under various loading and modulation value situations, different outcomes are displayed, in addition to the outcomes with different modulation indices and loads. The real-time results of the suggested topology are then demonstrated using Opal RT OP5700 real-time simulator.

7.1. Simulation Results

The outcomes of a simulation of the proposed 13-level topology are shown in this section. This subsection's goal is to demonstrate how well the recommended design works for a range of loading conditions, as shown in Figure 8. The parameters of the simulation, which are listed and can be seen in Table 3, are displayed. This simulation is performed using the MATLAB/Simulink 2023b software as shown in Figure 7b.

Table 3. Simulation parameters

Parameters	Values
V_{DC1} and V_{DC2}	50 V, 150 V
Capacitors	2200 µF, 200 V; 2200 µF, 200 V
Resistance at load	40 Ω, 50 Ω
Inductance at load	80 mH
Frequency	60 Hz
M variation	1.0 to 0.8 to 0.5

For Figure 8a,b, the output voltage and current waveforms under fixed-load conditions—firstly resistive load (40 Ω) and then RL load ($R = 40\ \Omega, L = 80$ mH)—exhibit well-defined sinusoidal profiles. This demonstrates the capability of the proposed 13-level inverter topology to produce high-quality voltage and current waveforms. The Total Harmonic Distortion (THD) of the output voltage in both scenarios is measured at 6.73%, which complies with the IEEE-519 standard for harmonic distortion (THD < 8%) [35]. These results confirm the inverter's ability to maintain high power quality under fixed-load conditions. Also, in this same plot, the capacitor voltage across C_1 and C_2 is also shown, which is pretty much fixed at around 50 V, suggesting the capability of self-balancing the voltages across C_1 and C_2 in this work.

For Figure 8c–e, the voltage and current profiles remain stable during the transitions between varying load conditions. In Figure 8c, the transition from R-load ($R = 40\ \Omega$) to ($R = 50\ \Omega$) shows minimal overshoot and rapid stabilization after the transition, but the voltage across the capacitors C_1 and C_2 is still fixed at 50 V, which can be the strength of this work. Figure 8d highlights the transition from R load of ($R = 40\ \Omega$) to an RL load of ($R = 40\ \Omega, L = 80$ mH), demonstrating no observable oscillations or deviations in the output waveforms. Similarly, Figure 8e shows the transition from RL load from ($R = 40\ \Omega, L = 80$ mH) to an RL load of ($R = 80\ \Omega, L = 80$ mH), resulting in no overshoot in current amplitude, as expected due to the increased load impedance. In this case too, voltage across capacitor is fixed at 50 V.

For Figure 8f,g, the output waveforms for dynamic modulation indices m = 1.0, m = 0.8, and m = 0.5 exhibit a proportional reduction in voltage amplitude while maintaining waveform integrity, along with maintaining the voltage across both capacitors C_1 and C_2. The Figure 8f shows the output voltage and output current when the modulation index is changing. The harmonic profile at these modulation indices indicates that the GA-optimized switching angles effectively mitigate harmonics, even at lower modulation indices. Figure 8h shows the zoomed voltage waveform for both capacitors C_1 and C_2 at $R = 40\ \Omega$ when the modulation index is transitioning from 1 to 0.8 and then to 0.5. It

can be seen that the voltage variation across both C_1 and C_2 is less than 2% even at low modulation index or 0.5, which justifies the suitablity and applicability of the proposed system. The THD values at different modulation indices are observed in Figure 9a as 6.73% at m = 1.0, in Figure 9b as 8.38% at m = 0.8, and in Figure 9c as 12.33% at m = 0.5. These results highlight the efficacy of the harmonic mitigation strategy across a wide range of modulation indices.

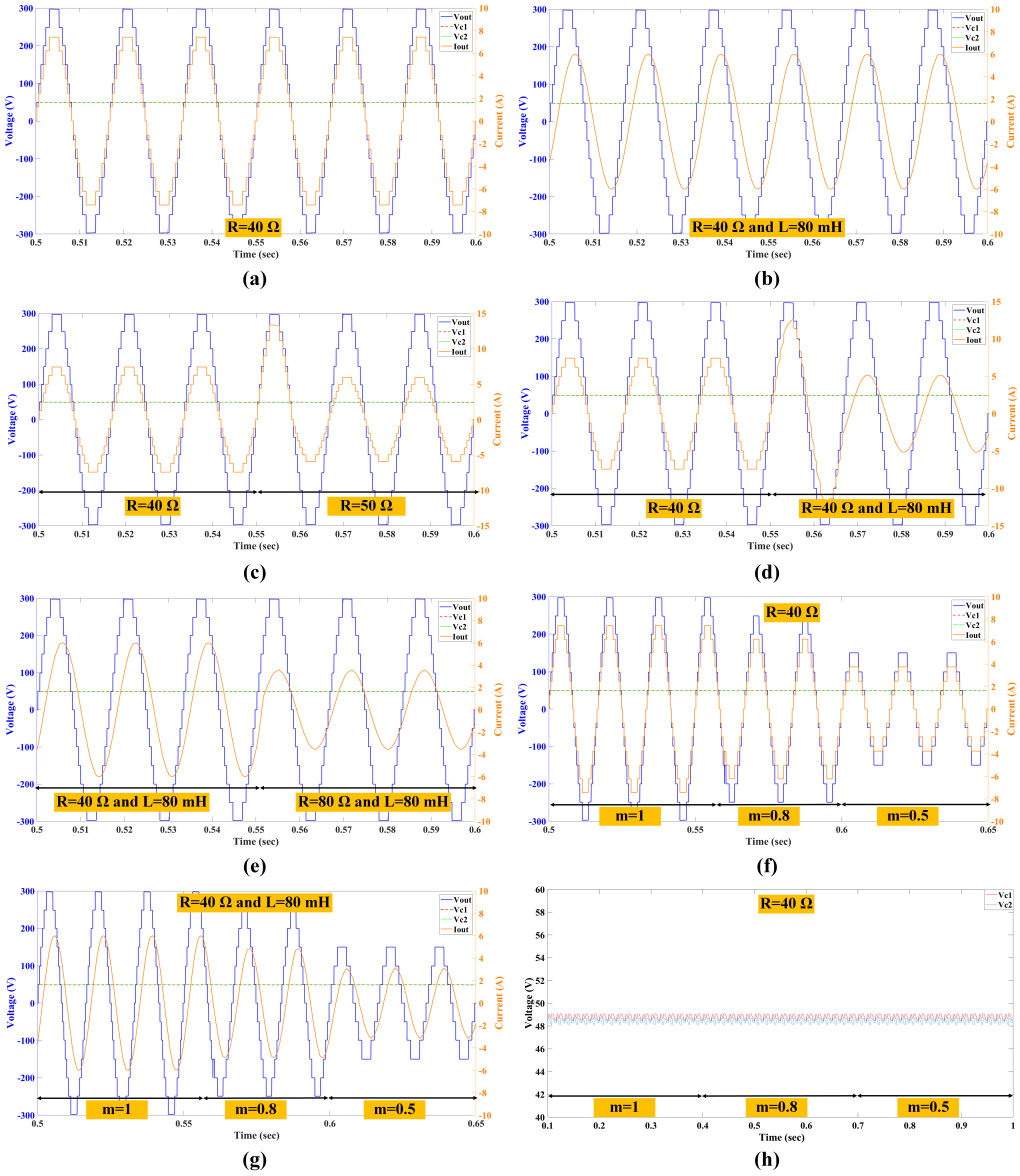


Figure 8. Waveforms of load voltage, capacitor voltages (V_{C1} and V_{C2}), and converter output current (I_{out}) of the 13-level inverter under different conditions: (**a**) fixed R-load ($R = 40\,\Omega$), (**b**) fixed RL-load ($R = 40\,\Omega, L = 80$ mH), (**c**) transition from $R = 40\,\Omega$ to $R = 50\,\Omega$ for R-load, (**d**) transition from $R = 40\,\Omega$ to $R = 50\,\Omega$ for RL-load ($L = 80$ mH), (**e**) transition from $R = 40\,\Omega, L = 80$ mH to $R = 80\,\Omega, L = 80$ mH, (**f**) modulation indices (m) reduced from 1.0 to 0.8 to 0.5 ($R = 40\,\Omega$), (**g**) modulation indices (m) reduced from 1.0 to 0.8 to 0.5 ($R = 40\,\Omega, L = 80$ mH), and (**h**) zoomed waveforms of voltages of capacitors C_1 and C_2 with modulation indices (m) reduced from 1.0 to 0.8 to 0.5 at ($R = 40\,\Omega$).

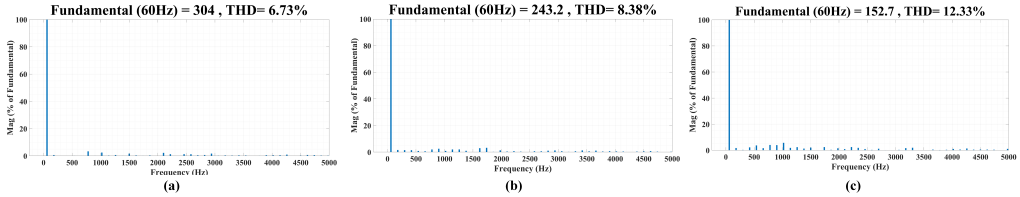


Figure 9. Voltage THD analysis for R load of $(R = 40\ \Omega)$ at (**a**) $m = 1.0$, (**b**) $m = 0.8$, and (**c**) $m = 0.5$.

A comparative analysis of the proposed improved GA and the conventional GA control systems was conducted to evaluate their performance in terms of efficiency and harmonic distortion. As shown in Figures 10 and 11, the improved GA outperforms the conventional GA by achieving higher efficiency and lower THD under various operating conditions. The adaptive mutation and crossover mechanisms in the improved GA enable better optimization of switching angles, leading to reduced system losses and improved harmonic performance.

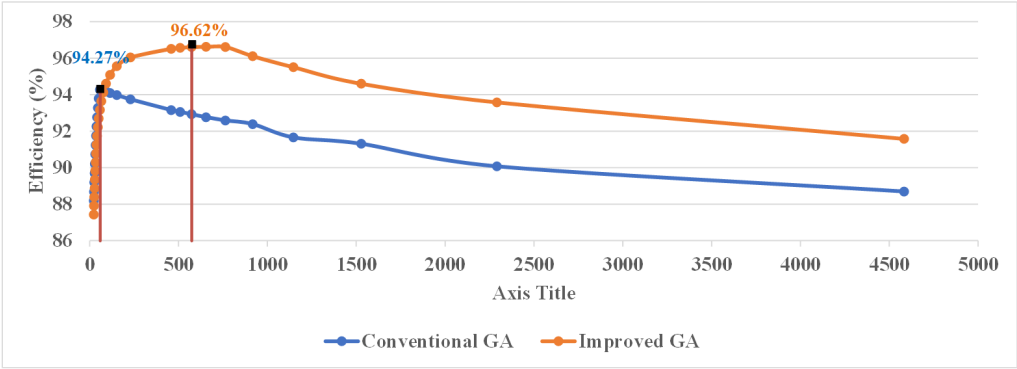


Figure 10. Efficiency comparison between the conventional GA and improved GA of this work.

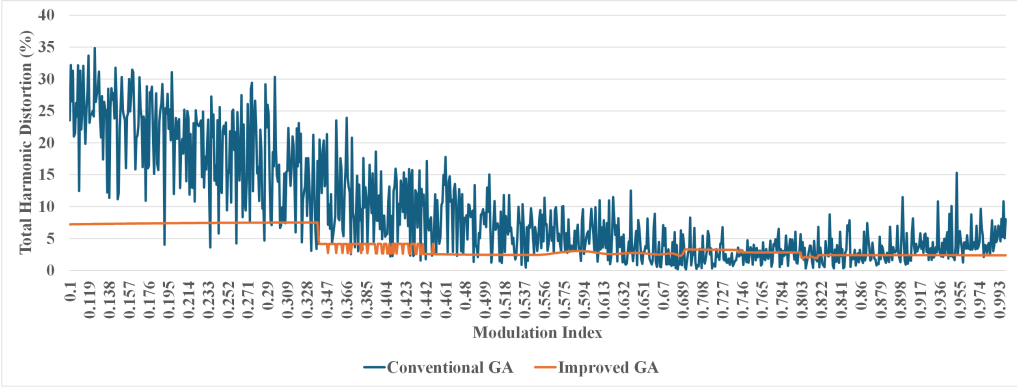


Figure 11. THD Comparison between the conventional GA and improved GA of this work.

7.2. Real-Time Simulation Results

Opal Rt OP5700 is utilized to demonstrate the performance of the topology in a real-time setup as shown in Figure 12. In order to verify the proposed improved genetic algorithm for this inverter, real-time analysis is performed using an OPAL RT OP5700 device simulator. To have a harmonic mitigation control scheme, we utilized the Opal RT-LAB 2024.3 version. Findings from the MATLAB/Simulink simulation conducted in the preceding section are consistent with the outcomes of the proposed inverter's real-time testing.

Figure 12. Real-time simulation setup using Opal-rt OP5700.

The waveforms in Figure 13 illustrate the real-time output voltage (V_{out}) and current (I_{out}) responses under varying conditions of load type and modulation index (m). Figure 13a shows the waveforms for a purely resistive load ($R = 40\,\Omega$) with full modulation ($m = 1.0$). The voltage (V_{out}) and current (I_{out}) are in phase, exhibiting high peak amplitudes with clean 13-level waveforms, indicating the absence of reactive components. Figure 13b extends this setup to an RL load of ($R = 40\,\Omega, L = 80$ mH) with the same modulation index ($m = 1.0$). Here, I_{out} lags behind V_{out} due to the inductive reactance of the load, though the amplitudes remain similar to (a), reflecting full modulation.

In Figure 13c, the resistive load ($R = 40\,\Omega$) is revisited, but the modulation index is reduced to $m = 0.8$. The voltage and current amplitudes decrease compared to full modulation, although they remain in phase due to the absence of reactive elements. Figure 13d repeats this for the RL load, where a noticeable lag between I_{out} and V_{out} persists. The reduction in modulation index is evident in the lower peak amplitudes of both waveforms.

Figure 13e depicts the resistive load under a further reduced modulation index of $m = 0.5$. The voltage and current amplitudes decrease significantly, with waveforms maintaining their phase alignment. In Figure 13f, the RL load at $m = 0.5$ further emphasizes the lag in I_{out} relative to V_{out}, with amplitudes reflecting the reduced modulation.

Figure 13g begins the exploration of dynamic transitions in the modulation index. For a resistive load ($R = 40\,\Omega$), the modulation changes from $m = 1.0$ to $m = 0.8$, which causes a gradual reduction in the amplitude of both V_{out} and I_{out} during the transition while maintaining their phase alignment. Figure 13h presents a similar transition for the RL load, where the amplitude of both waveforms decreases, and the phase lag in I_{out} persists throughout the transition.

Figure 13i highlights the transition for a resistive load from $m = 0.8$ to $m = 0.5$. As before, the amplitudes decrease dynamically, maintaining phase alignment. Finally, Figure 13j shows the RL load under the same transition. A similar reduction in amplitude is observed, with a consistent lag in I_{out} relative to V_{out}.

Overall, these results demonstrate the impact of modulation index on waveform amplitude and the distinct behavior of resistive and RL loads, particularly the lag in current for inductive loads and the in-phase behavior for purely resistive loads. Transition plots reveal smooth changes in waveform characteristics as the modulation index varies. These results in Figure 8 are in comparison with Figure 8, where both of these are under the same loading conditions or modulation indices. This demonstrates the applicability of this work in real time.

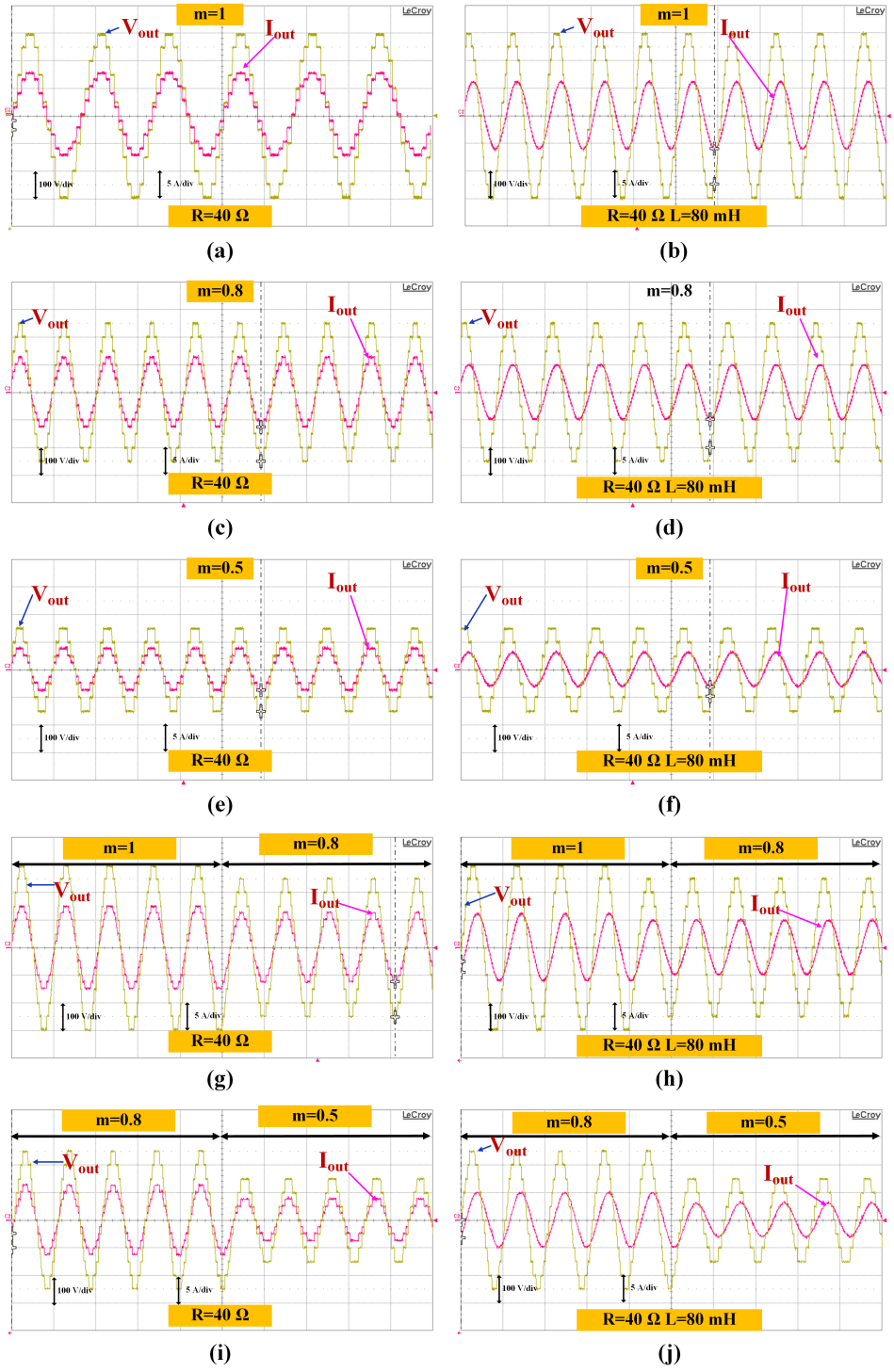


Figure 13. Real-time implementation using OP5700 output voltage (V_{out}) and current (I_{out}) waveforms under various conditions: (**a**) resistive load ($R = 40\,\Omega$) with modulation index (m) of 1.0, (**b**) RL load ($R = 40\,\Omega, L = 80\,\text{mH}$) with $m = 1.0$, (**c**) resistive load ($R = 40\,\Omega$) with $m = 0.8$, (**d**) RL load ($R = 40\,\Omega, L = 80\,\text{mH}$) with $m = 0.8$, (**e**) resistive load ($R = 40\,\Omega$) with $m = 0.5$, (**f**) RL load ($R = 40\,\Omega, L = 80\,\text{mH}$) with $m = 0.5$, (**g**) resistive load ($R = 40\,\Omega$) transitioning from $m = 1.0$ to $m = 0.8$, (**h**) RL load ($R = 40\,\Omega, L = 80\,\text{mH}$) transitioning from $m = 1.0$ to $m = 0.8$, (**i**) resistive load ($R = 40\,\Omega$) transitioning from $m = 0.8$ to $m = 0.5$, and (**j**) RL load ($R = 40\,\Omega, L = 80\,\text{mH}$) transitioning from $m = 0.8$ to $m = 0.5$.

8. Conclusions

A single-phase asymmetric thirteen-level SC-MLI with excellent voltage gain is shown in this study, along with an improved genetic algorithm for proper harmonic mitigation. This architecture consists of two capacitors, a single diode, dual-voltage power sources, and eleven power switches. This study also incorporates an improved genetic algorithm (GA) that dynamically adjusts mutation and crossover rates based on population diversity and fitness variance, ensuring robust convergence to optimal solutions. These enhancements effectively address the challenge of local optima and significantly improve the algorithm's performance for harmonic mitigation in the proposed inverter topology. Compared to current topologies, the provided architecture uses fewer components, which lowers the system's overall size and cost. The roles and transitions of each of the thirteen stages of operation are thoroughly addressed. After analyzing the power loss and efficiency of the proposed converter, it was found to have a maximum efficiency of 96.62%, which is very good in terms of industrial applicability. Additionally, the PLEXIM-PLECS software is used to determine the power loss distribution for various IGBTs and diodes. The 13-level SC-MLI is simulated using basic frequency-based NLC algorithms under various loading scenarios. Additionally, the modulation index and load are modified and examined. The voltage of the capacitors self-balances at their reference value even when the modulation index is low. Real-time verification using OPAL RT OP5700 is utilized to implement this work, which in return verifies the applicability of this work in real time. It was also discovered that the voltage THD is 6.73%, which is under the limit of the IEEE-519 standards.

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Abbreviations

The following abbreviations are used in this manuscript:

AC	Alternating Current
CF	Cost Function
CHB	Cascaded H-Bridge
DC	Direct Current
ESR	Equivalent Series Resistance
FC	Flying Capacitor
FFT	Fast Fourier Transform
GA	Genetic Algorithm
IGBT	Insulated Gate Bipolar Transistor
LP	Linear Programming
MMC	Modular Multilevel Converters
NLP	Nonlinear Programming
NPC	Neutral-Point Clamped
PSO	Particle Swarm Optimization
RL	Resistive–Inductive (Load)
SA	Simulated Annealing

SC-MLI	Switched-Capacitor Multilevel Inverter
SHM	Selective Harmonic Mitigation
THD	Total Harmonic Distortion
TSV	Total Standing Voltage

References

1. Anjaneya Vara Prasad, P.; Dhanamjayulu, C. An Overview on Multi-Level Inverter Topologies for Grid-Tied PV System. *Int. Trans. Electr. Energy Syst.* **2023**, *2023*, 9690344. [CrossRef]
2. Han, D.; Peng, F.Z.; Dwari, S. Advanced PWM Techniques for Multi-Level Inverters with a Multi-Level Active CM Noise Filter. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**, *10*, 6865–6879. [CrossRef]
3. Dhanamjayulu, C.; Sanjeevikumar, P.; Muyeen, S.M. A Structural Overview on Transformer and Transformer-Less Multi-Level Inverters for Renewable Energy Applications. *Energy Rep.* **2022**, *8*, 10299–10333.
4. Hosseinzadeh, M.A.; Sarebanzadeh, M.; Garcia, C.F.; Babaei, E.; Rodriguez, J.; Kennel, R. Reduced Multisource Switched-Capacitor Multilevel Inverter Topologies. *IEEE Trans. Power Electron.* **2022**, *37*, 14647–14666. [CrossRef]
5. Anand, V.; Singh, V. A 13-Level Switched-Capacitor Multilevel Inverter with Single DC Source. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**, *10*, 1575–1586. [CrossRef]
6. Barzegarkhoo, R.; Forouzesh, M.; Lee, S.S.; Blaabjerg, F.; Siwakoti, Y.P. Switched-Capacitor Multilevel Inverters: A Comprehensive Review. *IEEE Trans. Power Electron.* **2022**, *37*, 11209–11243. [CrossRef]
7. Iqbal, H.; Tariq, M.; Sarfraz, M.; Sarwat, A.I.; Alhosaini, W.; Aldosari, O.; Aziz, A. Selective Harmonic Mitigation Based Two-Scale Frequency Control of Cascaded Modified Packed U-Cell Inverters. *Energy Rep.* **2022**, *8*, 1009–1020. [CrossRef]
8. Iqbal, H.; Tufail, S.; Tariq, M.; Sarwat, A.I.; Sarwar, A. GA-Based Integrated SHM-NLC Control for a Single Sourced Switched Capacitor Multi-Level Inverter with Boosting Capability for Microgrid. In Proceedings of the 2023 IEEE International Conference on Energy Technologies for Future Grids (ETFG), Wollongong, Australia, 3–6 December 2023; pp. 1–6.
9. Villanueva, E.; Correa, P.; Rodríguez, J.; Pacas, M. Control of a Single-Phase Cascaded H-Bridge Multilevel Inverter for Grid-Connected Photovoltaic Systems. *IEEE Trans. Ind. Electron.* **2009**, *56*, 4399–4406. [CrossRef]
10. Rodriguez, J.; Bernet, S.; Steimer, P.K.; Lizama, I.E. A Survey on Neutral-Point-Clamped Inverters. *IEEE Trans. Ind. Electron.* **2009**, *57*, 2219–2230. [CrossRef]
11. He, L.; Cheng, C. A Flying-Capacitor-Clamped Five-Level Inverter Based on Bridge Modular Switched-Capacitor Topology. *IEEE Trans. Ind. Electron.* **2016**, *63*, 7814–7822. [CrossRef]
12. Perez, M.A.; Ceballos, S.; Konstantinou, G.; Pou, J.; Aguilera, R.P. Modular Multilevel Converters: Recent Achievements and Challenges. *IEEE Open J. Ind. Electron. Soc.* **2021**, *2*, 224–239. [CrossRef]
13. Lingom, P.M.; Song-Manguelle, J.; Nyobe-Yome, J.M.; Doumbia, M.L. A Comprehensive Review of Compensation Control Techniques Suitable for Cascaded H-Bridge Multilevel Inverter Operation with Unequal DC Sources or Faulty Cells. *Energies* **2024**, *17*, 722. [CrossRef]
14. Odeh, C.I.; Lewicki, A.; Morawiec, M.; Jąderko, A. Enhanced Four-Level Active Nested Neutral Point-Clamped Inverter. *Energies* **2024**, *17*, 3213. [CrossRef]
15. Rohner, G.; Huber, J.; Mirić, S.; Kolar, J.W. Comparative Evaluation of Three-Phase Three-Level Flying Capacitor and Stacked Polyphase Bridge GaN Inverter Systems for Integrated Motor Drives. *Electronics* **2024**, *13*, 1259. [CrossRef]
16. Iqbal, H.; Tayyab, M.; Rehman, H.; Sarwar, A.; Hussan, M.R. 13 Level Switched-Capacitor Multilevel Converter with High Gain for Grid Connected Solar Photovoltaic Applications. In *Multilevel Converters*; Scrivener Publishing LLC: Beverly, MA, USA, 2024; pp. 147–163.
17. Seifi, A.; Hosseini, S.H.; Tarafdar Hagh, M.; Hosseinpour, M. Capacitor Based Topology of Cross-Square-Switched T-Type Multi-Level Inverter. *Sci. Rep.* **2024**, *14*, 3166. [CrossRef]
18. Srinivasan, G.K.; Rivera, M.; Loganathan, V.; Ravikumar, D.; Mohan, B. Trends and Challenges in Multi-Level Inverter with Reduced Switches. *Electronics* **2021**, *10*, 368. [CrossRef]
19. Bano, K.; Abbas, G.; Hatatah, M.; Touti, E.; Emara, A.; Mercorelli, P. Phase Shift APOD and POD Control Technique in Multi-Level Inverters to Mitigate Total Harmonic Distortion. *Mathematics* **2024**, *12*, 656. [CrossRef]
20. Pan, Q.; Zhang, C.; Guo, S.; Sun, H.; Du, J.; Guo, P. An Interval Multi-Objective Fuzzy-Interval Credibility-Constrained Nonlinear Programming Model for Balancing Agricultural and Ecological Water Management. *J. Contam. Hydrol.* **2022**, *245*, 103958. [CrossRef]
21. Iqbal, H.; Khalid, A.; Riggs, H.; Sarwat, A. *Kalman Filter-Based Harmonic Distortion Mitigation Technique for Microgrid Applications*; IntechOpen: London, UK, 2024.
22. Yiğit, H.; Ürgün, S.; Mirjalili, S. Comparison of Recent Metaheuristic Optimization Algorithms to Solve the SHE Optimization Problem in MLI. *Neural Comput. Appl.* **2023**, *35*, 7369–7388. [CrossRef]

23. Katoch, S.; Chauhan, S.S.; Kumar, V. A Review on Genetic Algorithm: Past, Present, and Future. *Multimed. Tools Appl.* **2021**, *80*, 8091–8126. [CrossRef]
24. Saeedian, M.; Hosseini, S.M.; Adabi, J. Step-Up Switched-Capacitor Module for Cascaded MLI Topologies. *IET Power Electron.* **2018**, *11*, 1286–1296. [CrossRef]
25. Iqbal, A.; Siddique, M.D.; Reddy, B.P.; Maroti, P.K.; Alammari, R. A New Family of Step-Up Hybrid Switched-Capacitor Integrated Multilevel Inverter Topologies with Dual Input Voltage Sources. *IEEE Access* **2020**, *9*, 4398–4410. [CrossRef]
26. Roy, T.; Sadhu, P.K. A Step-Up Multilevel Inverter Topology Using Novel Switched Capacitor Converters with Reduced Components. *IEEE Trans. Ind. Electron.* **2020**, *68*, 236–247. [CrossRef]
27. Peng, W.; Ni, Q.; Qiu, X.; Ye, Y. Seven-Level Inverter with Self-Balanced Switched-Capacitor and Its Cascaded Extension. *IEEE Trans. Power Electron.* **2019**, *34*, 11889–11896. [CrossRef]
28. Siddique, M.D.; Mekhilef, S.; Sarwar, A.; Alam, A.; Mohamed Shah, N. Dual Asymmetrical DC Voltage Source Based Switched Capacitor Boost Multilevel Inverter Topology. *IET Power Electron.* **2020**, *13*, 1481–1486. [CrossRef]
29. Ye, Y.; Cheng, K.W.E.; Liu, J.; Ding, K. A Step-Up Switched-Capacitor Multilevel Inverter with Self-Voltage Balancing. *IEEE Trans. Ind. Electron.* **2014**, *61*, 6672–6680. [CrossRef]
30. Ye, Y.; Zhang, G.; Wang, X.; Yi, Y.; Cheng, K.W.E. Self-Balanced Switched-Capacitor Thirteen-Level Inverters with Reduced Capacitors Count. *IEEE Trans. Ind. Electron.* **2021**, *69*, 1070–1076. [CrossRef]
31. Alishah, R.S.; Bertilsson, K.; Blaabjerg, F.; Sathik, M.A.J.; Rezaee, A.Y. New Grid-Connected Multilevel Boost Converter Topology with Inherent Capacitors Voltage Balancing Using Model Predictive Controller. In Proceedings of the 2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe), Lyon, France, 7–11 September 2020; pp. 1–7.
32. Shalchi Alishah, R.; Hosseini, S.H.; Babaei, E.; Sabahi, M.; Zare, A. Extended High Step-Up Structure for Multilevel Converter. *IET Power Electron.* **2016**, *9*, 1894–1902. [CrossRef]
33. Kumari, P.; Singh, A.K.; Kumar, N.; Mandal, R.K. Self-Balanced High Gain Switched-Capacitor Boosting Inverter with Lower Cost Function. *Int. J. Electron.* **2023**, *111*, 1301–1318. [CrossRef]
34. Infineon Technologies. IKW40N65ES5 Discrete IGBT Product Page. Available online: https://www.infineon.com/cms/en/product/power/igbt/igbt-discretes/ikw40n65es5/ (accessed on 14 November 2024).
35. *IEEE Std 519-2022*; IEEE Standard for Harmonic Control in Electric Power Systems. IEEE: Piscataway, NJ, USA, 2022; pp. 1–31. Available online: https://ieeexplore.ieee.org/document/9848440 (accessed on 14 November 2024).