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A Semiconductor Current-Limiting Device Based on a DC Converter

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Abstract: Short-circuit currents in autonomous and isolated electrical complexes today are approaching the switching capacity of operated circuit breakers. Since the existing equivalents cannot ensure the necessary reliability of power supply to consumers in emergency situations, it is pertinent to assess the need for developing new types of current-limiting devices (CLDs). This paper proposes an electrical circuit of a semiconductor current-limiting device based on a step-down DC-DC converter, where the main switch is a thyristor with an artificially switched circuit. Transient processes during the operation of the device are considered in detail. A mathematical model of the device is also provided. This model was verified by modeling the CLD circuit in MATLAB Simulink. In turn, the validity of the computer model used was proven experimentally. During the experiments, the current-limiting efficiency of the circuit was demonstrated, and its proposed mathematical model was also confirmed. This research was carried out as part of the project within the State Assignment FSEG-2023-0012.

Keywords: semiconductor device; current limiting; short circuit; DC-DC converter; resonance scheme

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1. Introduction

The overwhelming majority of autonomous and isolated-from-the-common-power-grid electrical complexes rely on high-power energy storage devices (such as storage banks (SBs), supercapacitors, etc.) for their functioning. Such storage devices can cause large-scale accidents, which the power system, due to its autonomy, must handle on its own with minimal consequences for itself. Complexes with such problems include large mobile power systems involving electric propulsion (electric planes [1,2] and some modern ships [3–5]), as well as industrial mining facilities (e.g., oil platforms [6–8]).

The power systems under consideration are characterized as short networks without significant reactance of connecting lines, having a high degree of electrification and a high density of power generation. These properties result in several negative consequences: high speed and maximum level of short-circuit currents (up to 200–300 kA [1,8]). These problems are most clearly observed in the DC supply system, which is closely related to the prospect of developing such power sources as magnetogasdynamic generators and fuel cells. In addition, we should note the growing use of lithium-ion SB in the complexes under consideration. This type of battery has a reduced internal resistance, which can cause a further increase in short-circuit currents.

One of the few experimental methods for a comprehensive solution to these problems is the use of blast fuses, which are capable of disconnecting a short circuit of this level [8,9]. Compared to circuit breakers, blast fuses are significantly simpler in design, faster-acting,

more compact, and cheaper [10]. However, their use can lead to a decrease in the reliability of the power supply due to the duration of operations necessary for replacing tripped fuses, and, consequently, long pauses in the power supply to the consumer [11]. In addition, the use of fuses to disconnect short-circuit shock currents creates a significant threat of selective shutdown of the damaged sections of the circuit [12,13].

Circuit breakers based on fully or semi-controlled (artificial zero current circuits, or the so-called resonant circuits) semiconductor devices are quite well studied and have many options for circuit solutions for various types of electrical complexes [14–20]. Due to the continuous development of technologies for high-power semiconductor devices, such circuit breakers already achieved relatively satisfactory cost and good mass-dimensional characteristics. The main advantage of such switches is their ability to quickly—within several hundred μs from the beginning of the detection of an emergency state of the grid—disconnect a high short-circuit current. This significantly reduces the risks to power supplies. However, the high accuracy of the sequence of shutdown of such devices is achieved under the premise of the complete replacement of all switching equipment of the power system with semiconductor switches (with an integrated control system), which, depending on the scale of the power system in question, can be vastly excessive [21].

For an autonomous system not having a connection to an external power system (as to an emergency power source), it is important to ensure a high degree of reliability of operation, i.e., in the event of an accident, as many electric loads as possible should remain in operation. Furthermore, we will consider a three-level system of the sequence of operation of the switching system used in practice in the following example [22] (the first level (L1) is the power supply (PS), the second level (L2) is the distribution system and the consumers (C), and the third level (L3) is the consumers (C) in Figure 1). We assigned the following values to the response time of switching devices at different levels: t_1 (ACB1) > t_2 (ACB2 and ACB3) > t_3 (ACB4 and ACB5) (e.g., t_1 = 1 s, t_2 = 0.38 s, and t_3 = 0.1 s).

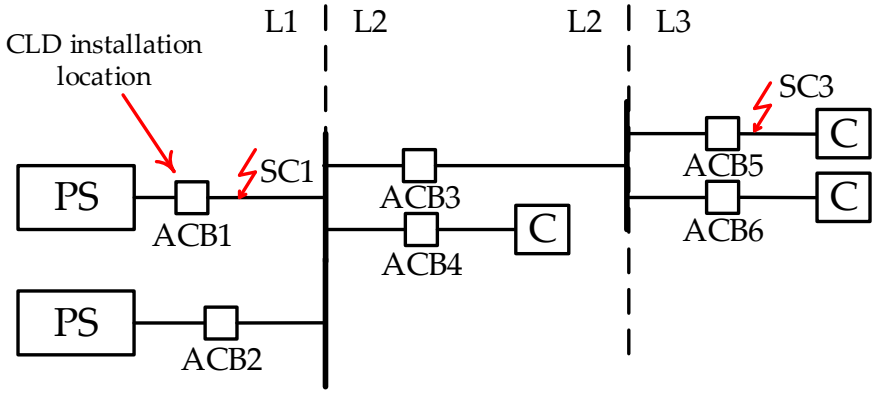


Figure 1. Sample diagram of a power system section for clarification of the principle of the selective operation of switching equipment.

In the event of a short circuit occurring at point SC3, only one ACB5 switch will trip, while ACB1 and ACB2 switches will not have time to trip due to their longer tripping time, and the consumers C connected via ACB4 and ACB6 will remain powered (due to the selectivity of the relay protection), which will result in the lowest cost outcome of the accident. However, the principle under consideration also has negative consequences. For example, in the event of a short circuit at point SC1, the PS will remain in emergency mode at the maximum set tripping delay, which poses a significant threat to the safety of the electrical complex (transition from a metal short circuit to an arc fault, overheating of generating units, SB explosion, etc.).

To solve this problem, it is advisable to install in series with the PS not a circuit breaker, but a current-limiting device (CLD) capable of limiting the short-circuit current for a relatively long time (at the level of the ACB system tripping time). This will significantly reduce the risks of further escalation of the accident.

As previously noted, the connecting elements of autonomous networks have low reactance. Due to this, if a short circuit occurs at almost any point in the power system, ACB will cut off the current close to the maximum possible. Here, the CLD connected to the PS will contribute to improving the conditions for disconnecting emergency currents through the ACB.

Let us consider another, more specific example. Figure 2 shows a diagram of the power system of a prospective marine vessel equipped with an electric propulsion system.

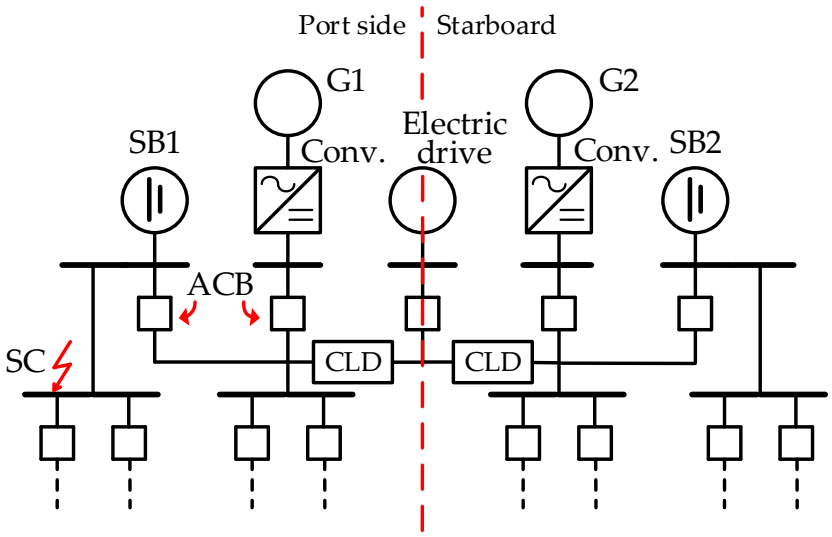


Figure 2. A diagram of the power system of a prospective vessel equipped with electric propulsion.

In the event of a short circuit in the vicinity of the SB (for example, at point SC in Figure 2), it is necessary to reduce the fault currents to the level of the switching capacity of the ACB. To this end, it is necessary to disconnect all possible sources from the accident as soon as possible.

To do this, firstly, the blast current-limiting fuses connecting the power system of the two sides are triggered. Such fuses are today generally considered the main CLD for ship power systems (in Figure 2, they are denoted with the block of the same name). This is where the first problem arises—if both fuses trip, a complete shutdown and subsequent prolonged shutdown of the electric drive can occur.

Secondly, the emergency side generator (G1) will shut down by disconnecting the converters (stopping the supply of control pulses). The port side will be completely de-energized. For the main electrical loads of the vessel (various types of electrical drives), an interruption in the power supply is unacceptable in most cases, since it leads to the disruption of the operation of the power plants and critical ship systems (cooling pumps, fans of power plants, etc.).

Here, too, a possible solution to the problem would be the use of adjustable short-circuit current-limiting devices (in the CLD location in Figure 2, to replace the fuses), i.e., without interrupting the electrical connection between the two sides. Let us consider the advantages of an adjustable current limiter between the sides for the same short circuit.

Firstly, there will be no need to shut down the generator G2. Here, the emergency current from G2 will be significantly less (due to the limitation of the flow through the CLD), and with the correct setting of the emergency current setpoint, it is possible to achieve the

continuous operation of the converter at the output of G2. Usually, semiconductor switches (in particular, thyristors) as part of the converter and generator winding can withstand relatively small current overloads for a short time.

Secondly, after the converter protection at the output G1 and SB is tripped with the subsequent isolation of the emergency section of the circuit from the main part of the power system, part of the consumers on the port side (the volume of this part will depend on the coverage of the ES operation) remains powered by the power plant on the starboard side, which increases the reliability of the power system as a whole.

Thirdly, the ability of the prospective CLD to remain in operation for a long time before, during, and after the SC allows the power supply to the electric drive not to be interrupted.

Fourthly, limiting the flow of short-circuit current between the sides will avoid a significant voltage drop on the non-emergency side, thereby increasing the reliability of consumer operation.

The simplest method here is to use a current-limiting reactor. Such a reactor must pass through a large rated current and short-circuit current for a relatively long time, which will lead to large weight and size parameters of the device [23]. The reactor can also cause a problem with the switching of inductive DC circuits [24]. It is necessary to look for new ways for the long-term (regulated) limitation of short-circuit currents.

From the point of view of effective current limitation, materials that are capable of autonomously (under the influence of fault current), sharply changing their active resistance look advantageous. Such materials include superconductors and PTC-thermistors. The main limitation for the use of superconductor materials is the dimensions of the cooling system, and for PTC-thermistors—insufficient study of the problem of application for limiting large currents [25].

There are some circuits of semiconductor current-limiting devices. They can be subdivided by the type of the main switch—transistor [18] and thyristor [26]. The former, due to insufficient power per unit, requires the assemblies of a large number of transistors. This increases their cost, complexity of assembly, and problems of operation. Known thyristor-based limiters, due to the features of the transient process of charging/discharging capacitor banks (necessary to create an artificial zero of the thyristor current), have the problem of additional overcurrent of the main switch.

The rest of the article presents the following: a proposed diagram of a semiconductor current-limiting device and a description of the principle of its operation; a mathematical description of the transient processes of the presented circuit; the results of computer simulation of the current-limiting device in MATLAB Simulink; and the results of operation of an experimental prototype of the current-limiting device.

2. Electrical Diagram of the CLD

Figure 3 presents a diagram of the proposed semiconductor current-limiting device, the main property of which is its ability to limit the short-circuit current:

The circuit of the current-limiting device (Figure 3) contains a thyristor 1 (main thyristor) and a circuit with a capacitor bank (CB) 2 connected in parallel, for the discharge of which thyristors 3 and 4 (discharge thyristors) and a saturating inductor 5 (saturation reactor or di/dt protection device) are connected in series with the CB. To charge the CB, an IGBT transistor 6, an IGBT transistor with inverse diode 7 (charging transistors), a diode 8, and a resistor 9 are also connected to it in series. Here, reverse diode 8 and the diode part of element 7 prevent the backfeed on the IGBT transistors, while resistor 9 is designed to limit the charging current of the CB. To maintain the short-circuit current at a given level, a circuit is connected in series to the thyristor 1, including an inductor 10 and a diode 11 (a reactor and a diode of the current maintenance circuit, respectively). In the event of a short

circuit at the output, the CLD (terminals "+" and "−" on the right side of Figure 3) forms a "short-circuit maintenance circuit" consisting of a diode 11 and a reactor 10. In addition, the CLD contains a current measurement unit 12 and a semiconductor device control unit 13.

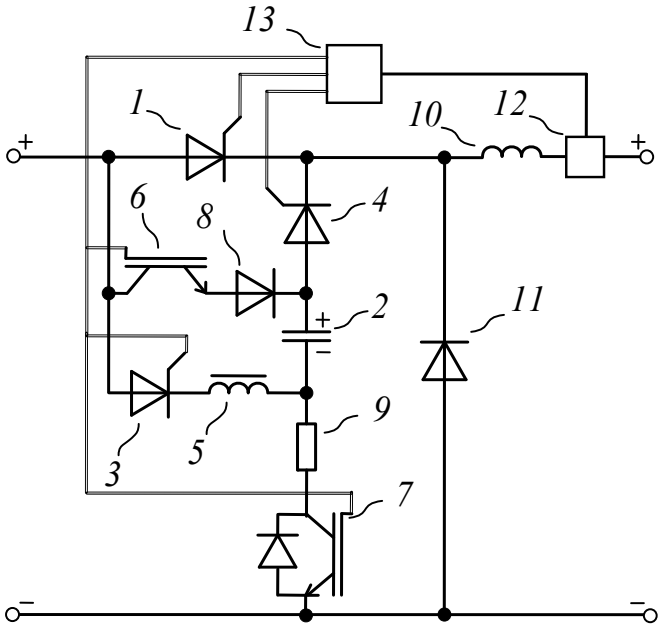


Figure 3. Electrical diagram of a semiconductor current-limiting device.

In the nominal operation mode of the power system, the thyristor 1 (in this paper, also known as the main thyristor) is in the switched-on state (time interval 0–T_0 in Figure 4 and diagram "a" in Figure 5). In the event of a short circuit in the power system (time interval T_0–T_1 in Figure 4 and diagram "b" in Figure 5), discharge thyristors 3 and 4 connect the CB of the counter-current, thereby forming an artificial switching loop of the main thyristor 1, bringing its current to zero with the application of reverse voltage (time moment T_1 in Figure 4 and diagram "c" in Figure 5). After the main thyristor 1 is switched off, the short-circuit current continues to circulate in the 10–11–SC circuit, slowly attenuating. At the same time, charging transistors 6 and 7, a circuit of "+"–6–8–2–9–7–"−" is formed, through which the counter-current CB is charged (time interval T_1-T_2 in Figure 4 and diagram "d" in Figure 5). The next step in the operation of the CLD is to re-engage the main thyristor for a short circuit and so on, repeating the operating cycle described above (time intervals T_3–T_2 and T_2–T_3 in Figure 4).

The foremost advantage of the proposed CLD is the use of a semiconductor thyristor as the main switching element. This type of semiconductor device has a practically unlimited switching resource, has a relatively low voltage drop, and is able to withstand short-term significant current overloads [27].

The specific features of this scheme are the following. The limited operating time of this CLD (up to 1 s) allows the use of diodes and thyristors at currents significantly exceeding their rated values (operating overload currents) but without reducing the reliability of the operation of these semiconductor devices. This allows for a significant reduction in the number of semiconductor devices in assemblies, which in turn will increase the reliability of the current-limiting device or increase its power (with an unchanged number of components). As a consequence of the above, an additional advantage of this device is the reduction in the weight and dimensions of the CLD by the declared power. The reactor (10 in Figure 3) will have a relatively small inductance. This also allows for the reduction in its mass and size parameters.

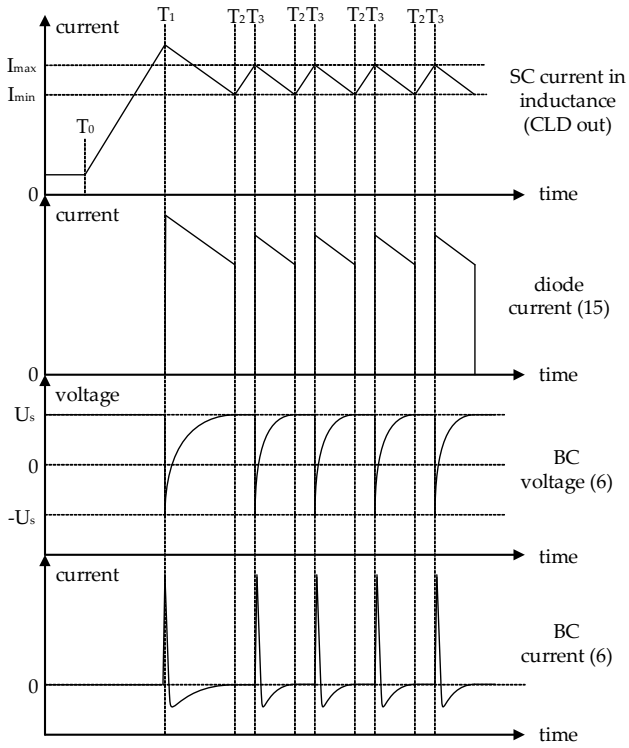


Figure 4. Oscillograms of transient processes during various stages of CLD operation.

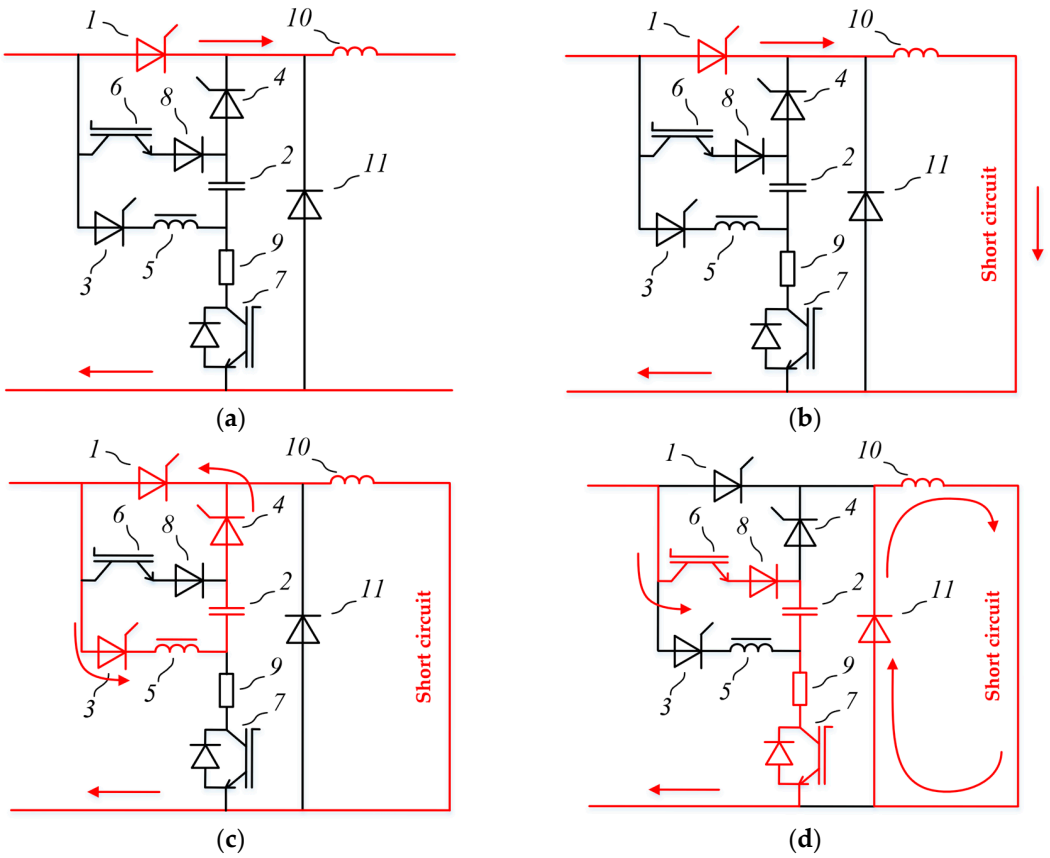


Figure 5. The stages of operation of the current-limiting device. (**a**) Nominal operation mode (time interval 0–T_0 in Figure 4). (**b**) The occurrence of a short circuit or the activation of the main thyristor (time intervals T_0–T_1 or T_2–T_3, respectively, in Figure 4). (**c**) The artificial switching of the thyristor (time moment T_1 in Figure 4). (**d**) The current pause of the CLD (time intervals T_1–T_2 and T_3–T_2 in Figure 4).

In order to create a valid computer model and evaluate the electrical parameters of the circuit of the current-limiting device under study, it is necessary to mathematically describe the transient processes considered.

3. CLD Transients

Figure 6 shows the equivalent circuit of the CLD under consideration (Figure 3). Here, for now, the artificially switched thyristor has been replaced by an abstract, fully controllable switch. This omission greatly simplifies the analysis of the transients in the circuit, but depending on the electrical parameters of the circuit elements of the device, it can have a significant impact on the accuracy of the calculation results. We will address this circumstance a little later. For now, this circuit can be considered a classic DC converter (breaker, chopper, etc.) based on a transistor.

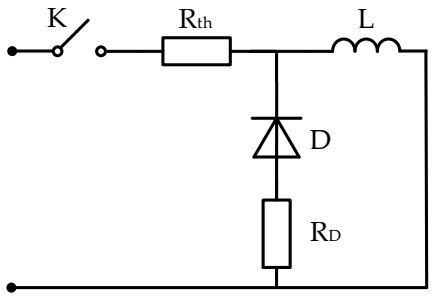


Figure 6. Current-limiting device equivalent circuit.

The following designations are present on this diagram: K is the fully controlled switch (replaces the main thyristor with an artificial switching circuit); L is the inductance of the reactor of the short-circuit current maintenance circuit; D is the diode of the short-circuit current maintenance circuit; Rth is the constant impedance of the main thyristor corresponding to the linear section of the I-V curve; and R_D is the same for the diode.

The circuit in Figure 6 has two states: when the switch K is in a closed position (Figure 7a) and in an open position (Figure 7b). In the first state, the current of the power supply is closed along the circuit (shown by the red bypass arrow) "power supply—main thyristor—reactor" and grows rapidly (Figure 7c, t_{on}). In the second state, the power supply is turned off, and the current continues to flow in the "reactor—diode" circuit due to the self-induction of the reactor and slowly attenuates due to the presence of active resistance of the diode (Figure 7c, t_{off}).

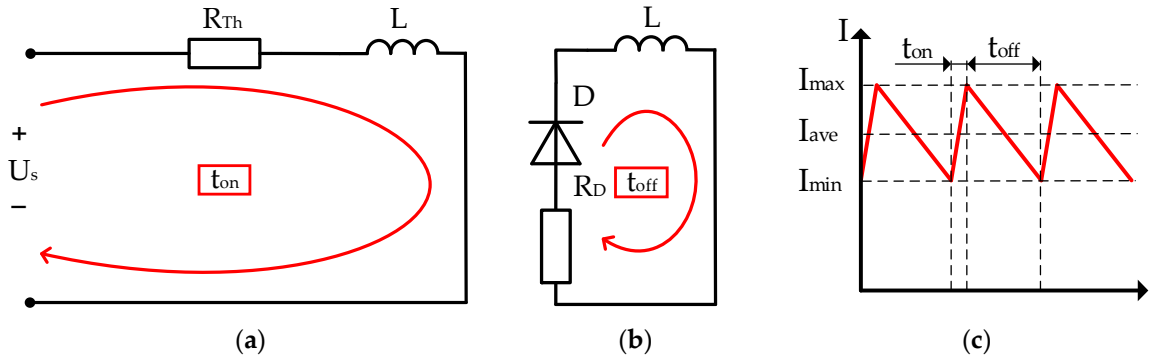


Figure 7. The transients of the current-limiting device: (**a**) the main thyristor is on; (**b**) the main thyristor is off; and (**c**) the current at the output of the current limiter/converter.

At the moment when the thyristor is on (Figure 7a), the following expression is true:

$$U_s = U_{Th} + U_L \quad (1)$$

where U_s is the voltage of the power supply, U_{Th} is the voltage drop across the thyristor, and U_L is the voltage drop across the inductor.

At another point, when the thyristor is off (Figure 7b), the following expression is true:

$$U_L + U_d = 0 \quad (2)$$

where U_d is the voltage drop across the diode.

The voltage drop across the inductor at the moment of switching on the main thyristor (Figure 7a) will be

$$U_L = -L \cdot dI/dt \approx -L \cdot (I_{max} - I_{min})/t_{on} \quad (3)$$

Similarly, for the off state of the main thyristor (Figure 7b)

$$U_L = -L \cdot dI/dt \approx -L \cdot (I_{min} - I_{max})/t_{off} \quad (4)$$

Here, I_{max} is the maximum pulsation current at the CLD output, I_{min} is the minimum pulsation current at the CLD output, t_{on} is the time interval the main thyristor spends on, and t_{off} is the time interval the main thyristor spends turned off (Figure 7c).

The voltage drop across semiconductor devices is assumed to be constant, equal to

$$U_D = R_D \cdot (I_{max} + I_{max})/2 \quad (5)$$

$$U_{Th} = R_{Th} \cdot (I_{max} + I_{max})/2 \quad (6)$$

We should note that if it is necessary to take into account the resistance of the power supply (or, in other words, the source of the short-circuit current supply), this resistance can be added to R_{Th}. Furthermore, if it is necessary to connect additional resistance to the short-circuit maintenance circuit (for example, to change the duty cycle of the main switch), then this resistance must be added to R_D (if it is connected in series to the diode) or separately to R_D and R_{Th} (if it is connected in series to the reactor).

Taking into account Equations (3)–(6), the system of equations for transient processes of the current-limiting device, consisting of Equations (1) and (2), will take the following form:

$$\begin{array}{c} L \cdot (I_{max} - I_{min})/t_{on} + R_{Th} \cdot (I_{max} + I_{min})/2 = U_S \\ -L \cdot (I_{max} - I_{min})/t_{off} + R_D \cdot (I_{max} + I_{min})/2 = 0 \end{array} \quad (7)$$

After simple transformations, from system (7), we can obtain I_{min} and I_{max} as follows:

$$I_{min} = \frac{-\frac{2 \cdot t_{on} \cdot U_S \cdot (R_D \cdot t_{off} - 2 \cdot L)}{(2 \cdot L + R_D \cdot t_{off}) \cdot (2 \cdot L + R_{Th} \cdot t_{on})}}{1 + \frac{(R_{Th} \cdot t_{on} - 2 \cdot L) \cdot (2 \cdot L - R_D \cdot t_{off})}{(2 \cdot L + R_D \cdot t_{off}) \cdot (2 \cdot L + R_{Th} \cdot t_{on})}} \quad (8)$$

$$I_{max} = \frac{-I_{min} \cdot (R_{Th} \cdot t_{on} - 2 \cdot L) + 2 \cdot t_{on} \cdot U_S}{(2 \cdot L + R_{Th} \cdot t_{on})} \quad (9)$$

From the analysis of Equations (8) and (9), the following conclusions can be drawn:

- The switching frequency of the main switch (F) of the CLD and the inductance of the current maintenance circuit (L) do not affect the average ($I_{ave} = (I_{max} + I_{max})/2$) limited current, but they do affect the magnitude of the limited current pulsations. The magnitude of the pulsations will also remain unchanged while maintaining the

L/F ratio. Note that the changes in the limited current observed in the experiment with a change in frequency are caused by a dynamic change in the active resistance of the reactor due to the uneven distribution of the current in the turns.

- The active resistance of the main switch has little effect on the shape of the limited current curve.
- The limited current pulsations strongly depend on the resistance of the current-maintaining circuit. For this reason, the dynamic resistance of the diode (its volt-ampere characteristic) and the active resistance of the reactor must be taken into account when modeling.
- The main influence on the current I_{ave} is the on–off time ratio of the main switch D ($D \sim I_{ave}$) and the voltage drop across the resistance of the diode assembly R_d ($R_d \sim 1/I_{ave}$).

4. Accounting for the Impact of the CB Discharge on the SC CLD

The discharge of an artificial switching capacitor bank can be divided into two stages. The first stage is when the battery is discharged to the main thyristor, bringing the current in it to zero, thereby locking it (Figure 8a). The second stage is the residual charge of the capacitor continuing to be discharged through the emergency section of the circuit along the circuit shown in Figure 8b. It is at this point that the discharge of the capacitor can somewhat inadvertently increase the current at the output of the CLD, which must be taken into account.

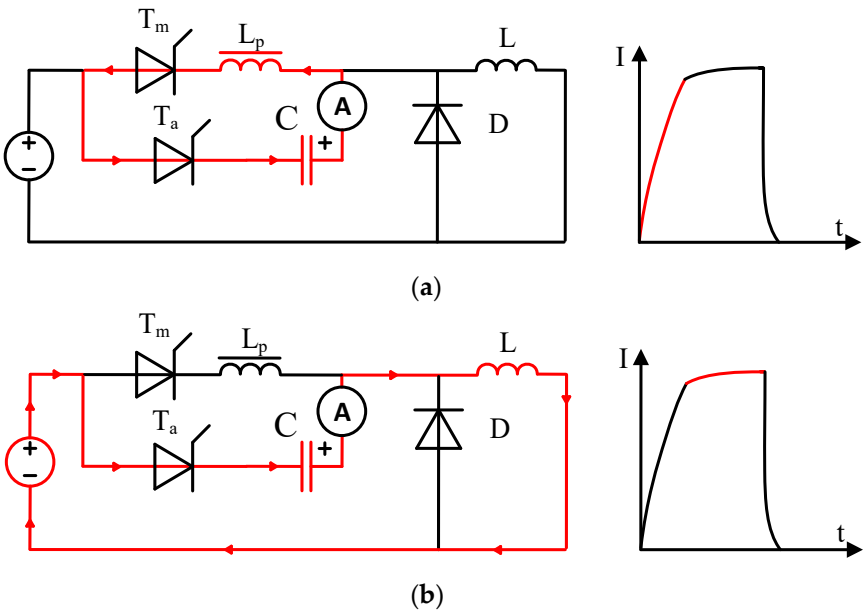


Figure 8. The transients of the CB discharge: (**a**) an approximate view of the substitution scheme and the oscillogram of the current at the output of the CLD, transients of the first stage; (**b**) transients of the second stage.

This addition of current is denoted as I_{add}. The system of Equation (7) will become the following:

$$\begin{gathered} L \cdot (I_{max} - I_{min})/t_{on} + R_{Th} \cdot (I_{max} + I_{min})/2 = U_S \\ -L \cdot (I_{max} + I_{add} - I_{min})/t_{off} + R_D \cdot (I_{max} + I_{min})/2 = 0 \end{gathered} \quad (10)$$

We will obtain a new expression for calculating I_{min} (8):

$$I_{min} = \frac{-\frac{R_D \cdot t_{off} - 2 \cdot L}{2 \cdot L + R_D \cdot t_{off}} \cdot \left(I_{add} + \frac{2 \cdot t_{on} \cdot U_S}{2 \cdot L + R_{Th} \cdot t_{on}} \right)}{1 + \frac{(R_{Th} \cdot t_{on} - 2 \cdot L) \cdot (2 \cdot L - R_D \cdot t_{off})}{(2 \cdot L + R_D \cdot t_{off}) \cdot (2 \cdot L + R_{Th} \cdot t_{on})}} \quad (11)$$

Equation (9) for calculating I_{max} remains unchanged.

We should note that now the designation I_{max} corresponds to the maximum current of the main thyristor, while the highest current in the short-circuit maintenance circuit will be determined by the sum of I_{max} and I_{add}.

The additional I_{add} CB discharge current consists of two components, designated I' and I'':

$$I_{add} = I' + I'' \quad (12)$$

The increase in current in the short-circuit maintenance circuit by the value I' occurs during the first stage of CB discharge, as can be seen from Figure 9 (time interval t_1). At this time, the main thyristor has not yet been completely artificially switched, and through it, the power supply is still electrically connected to the fault point, which in turn causes a further increase in the short-circuit current during this time interval.

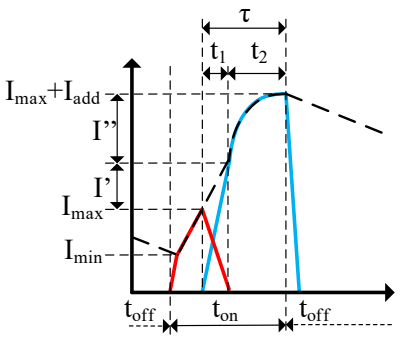


Figure 9. A more detailed picture describing the transient processes of the CB discharge. The black dashed curve is the current in the SC circuit; the red curve is the current of the main thyristor; and the blue curve is the current of the CB discharge.

Therefore, I' can be calculated using the following formula:

$$I' = (U_S \cdot t_1)/L_2 \quad (13)$$

The source of the component I'' is the second stage of CB discharge (time interval t_2 in Figure 9) or, in other words, the continuation of CB discharge through the SC circuit after the main thyristor is switched off. Expressions for the calculation of the I'' are as follows:

$$I'' = t_2 \cdot (U'_C + U_S)/(2 \cdot L_2) \quad (14)$$

where U'_C is the residual voltage of the CB after the discharge of the first stage.

Next, we will define the calculation of time intervals t_1 and t_2. The classical solution of the differential equation of the circuit current in Figure 8a is as follows:

$$I(t) = I_1 \cdot \cos(\omega_1 \cdot t - \varphi_1) \quad (15)$$

where I_1 is the maximum current of the circuit in question, while ω_1 is its natural resonant frequency.

Therefore,

$$t_1 = (\arccos(I^*/I_1) - \varphi_1)/\omega_1 \quad (16)$$

where I* is the value of the thyristor current immediately before the initialization of artificial switching ($\approx I_{max}$); φ_1 is the initial phase of the CB discharge ($\varphi_1 = \pi$).

To express the time t_2, it is necessary to first determine the residual voltage on the CB after the first stage, which will equal

$$U^*_{CB} = -\omega_1 \cdot L_1 \cdot I_0 \cdot \sin(\omega_1 \cdot t + \varphi_1) \quad (17)$$

At the beginning of the second stage,

$$U^*_{CB} + U_S = \omega_2 \cdot L_2 \cdot I_0 \cdot \sin(\omega_2 \cdot t + \varphi_2) \quad (18)$$

where ω_2 is the natural frequency of the circuit oscillation in Figure 8b.

From (18), we get

$$\varphi_2 = \text{arc sin}((U^*_{CB} + U_S)/(\omega_2 \cdot L_2 \cdot I_0)) \quad (19)$$

To calculate the time t_2, an expression similar to (18) will be used, but with the following initial conditions. The current in the circuit of artificial switching stops at the moment of the beginning of current attenuation in the current maintenance circuit, as the diode D at this moment begins to shunt the inductance L_2, thereby significantly reducing the inductance of the circuit and restoring its high-frequency oscillatory character. In turn, this locks the semiconductor devices of this circuit relatively quickly. Therefore, $dI/dt = 0$, and we obtain the following:

$$\omega_2 \cdot L_2 \cdot I_0 \cdot \sin(\omega_2 \cdot t_2 + \varphi_2) = 0 \quad (20)$$

or

$$t_2 = \omega_2 / \varphi_2 \quad (21)$$

The sum of t_1 and t_2 is the total time of the CB discharge.

$$\tau = t_1 + t_2 \quad (22)$$

The described formulas determine the maximum and minimum value of the limited current at the output of the device quite accurately, which can be easily checked using a circuit model similar to the one in Figure 3, implemented in the MATLAB Simulink 2020b software package.

5. Experiment

For the presented circuit of the current-limiting device, an experimental confirmation of the functionality of its operation was carried out. The photographs in Figure 10 show an assembled experimental current limiter.

A capacitor bank with an electrical capacity of 12.5 mF is used as a source of short-circuit current.

A complete electrical diagram of the experimental setup is shown in Figure 11. Here, electrical elements simulating parasitic parameters of connecting wires are indicated by red dotted frames.

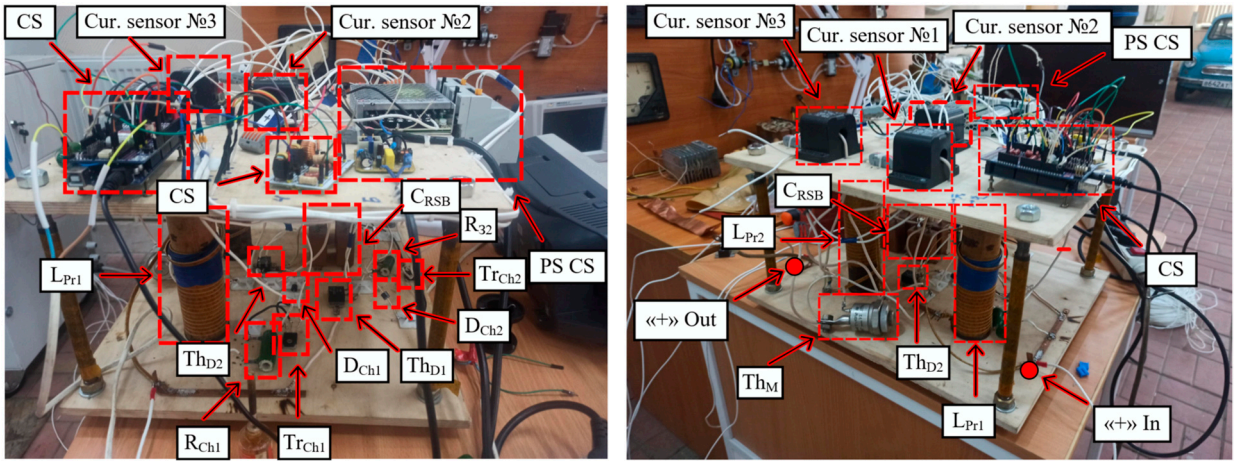


Figure 10. Appearance of the created prototype of the current-limiting device. (**a**) Photograph, view 1. (**b**) Photograph, view 2.

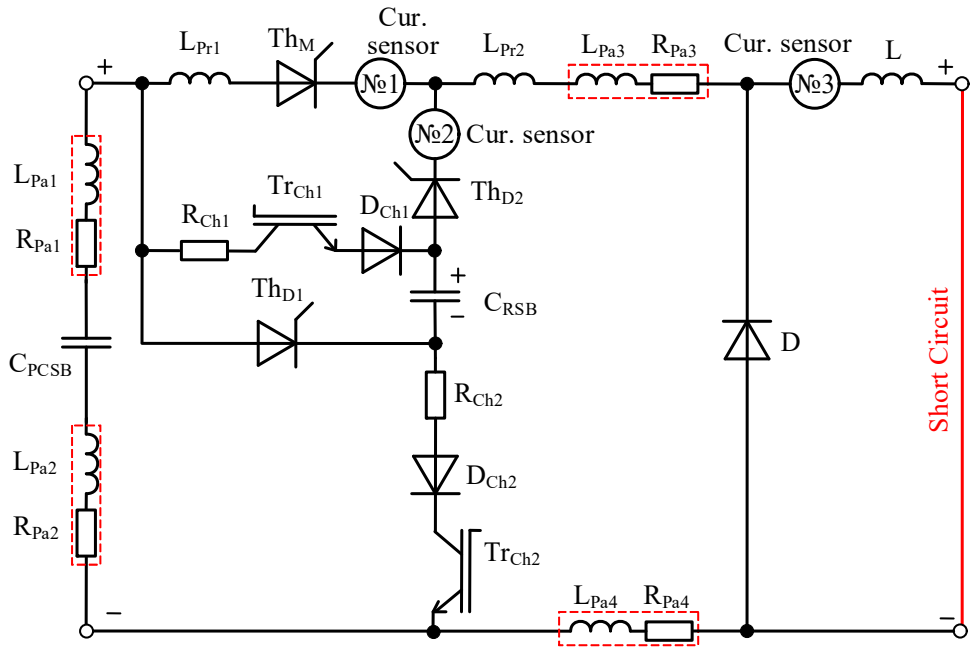


Figure 11. An electrical diagram of the experimental setup.

This electrical diagram and the photos show the following: C_{RSB} is an artificial switching battery; $L_{Pa1–2}$ and $R_{Pa1–2}$ are the parasitic inductance and resistance of wires connecting the source and the current-limiting device; $L_{Pa3–4}$ and $R_{Pa3–4}$ are the parasitic inductance and resistance of the wires connecting the current-limiting device and the circuit section with a short circuit; $L_{Pr1–2}$ are the inductors protecting thyristors from the di/dt effect; Th_M is the main thyristor; Cur. sensor No. 1–3 are the current sensors; $R_{Ch1–2}$ is the resistor for limiting the charge current of the C_{RSB} capacitor bank; $Tr_{Ch1–2}$ are IGBT transistors for charging the C_{RSB} capacitor bank during a currentless pause of the device; $D_{Ch1–2}$ are diodes for protecting IGBT charging transistors from reverse voltage; $Th_{D1–2}$ are thyristors for initializing the discharge of the C_{RSB} capacitor bank; and D and L are the diode and reactor of the current maintenance circuit.

Essentially, CLD operation during the experiment begins with the activation of the main Th_M thyristor or, in other words, begins with connecting the fault current source directly to the short circuit. Subsequently, after some time t_{on} of the CLD in the enabled

state, the Th_M thyristor and other elements are artificially turned off according to the algorithm described in Section 2 of this article. We should note that the control system (CS) is not closed, i.e., only a signal is sent to the CS input to initialize the CLD operation without current feedback or other electrical quantities.

Using the current sensors, the following current oscillograms were recorded: Cur. sensor No. 1—current of the main thyristor Th_M; Cur. sensor No. 2—discharge current of the C_{RSB} capacitor bank of the artificial switching branch; and Cur. sensor No. 3—current at the output of the CLD (limited short-circuit current). The measurement results are shown in Figures 12–14.

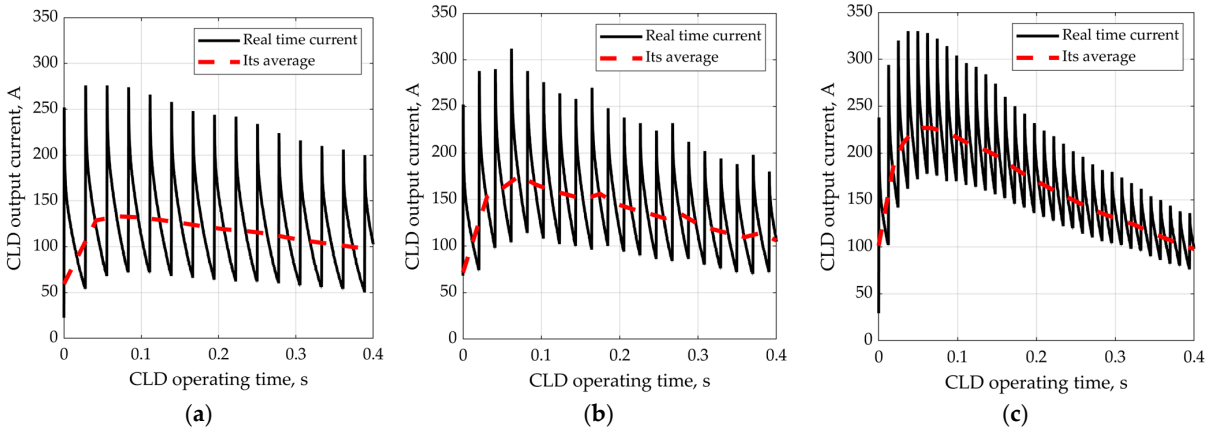


Figure 12. The current oscillograms at the CLD output (black solid line denotes experimental results; red dotted line is the average value) at a C_{PCSB} precharge voltage of 500 V. The CLD operating frequency is (**a**) 36 Hz; (**b**) 48 Hz; and (**c**) 81 Hz.

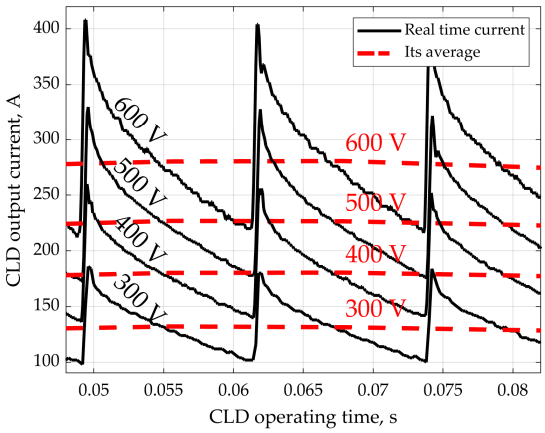


Figure 13. The current waveforms at the CLD output (the black solid line denotes the experimental results; the red dotted line is the average value) for the CLD operating at 81 Hz. The C_{PCSB} precharge voltage is indicated directly at the waveforms.

The experiments were carried out at several frequencies of CLD operation: 36 Hz (Figure 12a), 48 Hz (Figure 12b), and 81 Hz (Figures 12c and 13). For each of these frequencies, the C_{PCSB} precharge voltage rose to 300, 400, 500, and 600 V. The time of the switched-on state of the main thyristor Th_M in all experiments was $t_{on} \approx 220$ µs. The total time of current limitation in the experiments was approximately 400–600 ms.

To increase the accuracy of the calculation, the following additional substitution schemes were used in the MATLAB Simulink model. First, the diode in the current maintenance loop is modeled with its full I–V curve (without reverse current) through a controlled voltage source using a third-degree polynomial $I_d = f(U_d)$, the coefficients of

which are as follows: $p_1 = 1731$, $p_2 = -4971$, $p_3 = 5516$, and $p_4 = -2386$. Second, in order to take into account the dependence of the inductance and active resistance parameters in the reactor of the current maintenance circuit on frequency (the influence of the skin effect and the proximity effect), its equivalent circuit was supplemented, as shown in Figure 14 [28]. The following parameters of the substitution scheme in the figure were adopted: $L_{p1} = 700$ µH; $L_{p2} = 350$ µH; $R_{p1} = 1.5$ Ω; and $R_{p2} = 43$ mΩ.

Figure 15a,b show experimental waveforms of currents in the CLD and simulation results for comparison. From these oscillograms, it is possible to conclude that the developed computer model of the CLD under consideration is highly accurate.

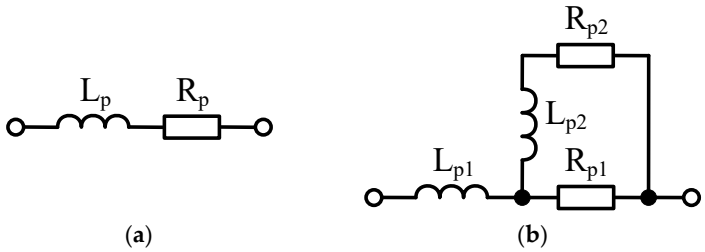


Figure 14. The equivalent circuit of the electromagnetic reactor of the DC circuit: (**a**) excluding the influence of skin effect and proximity effect; (**b**) taking into account the influence of the skin effect and the proximity effect.

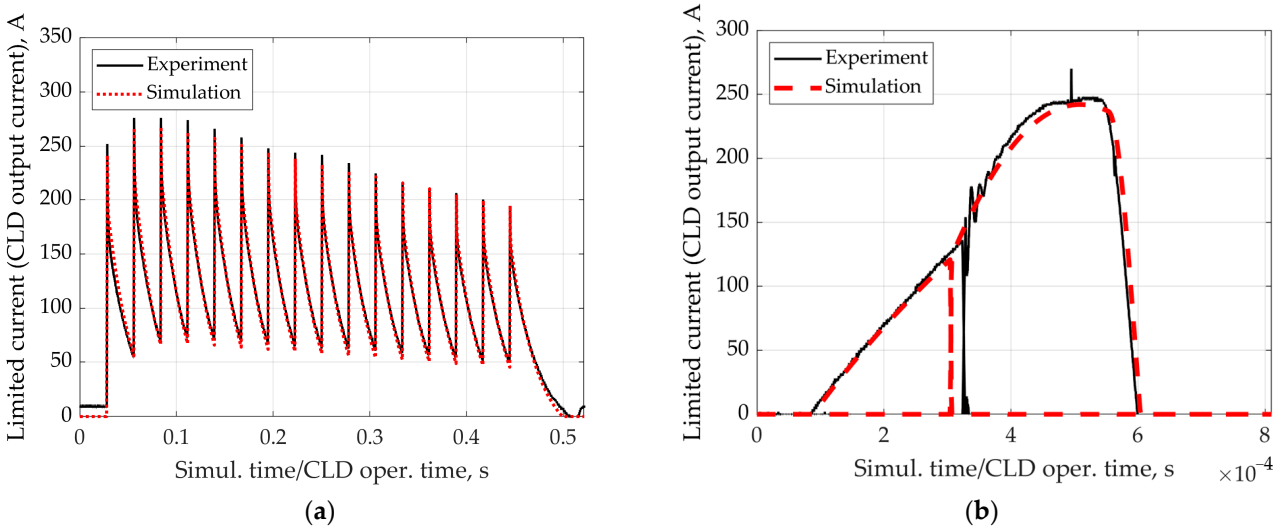


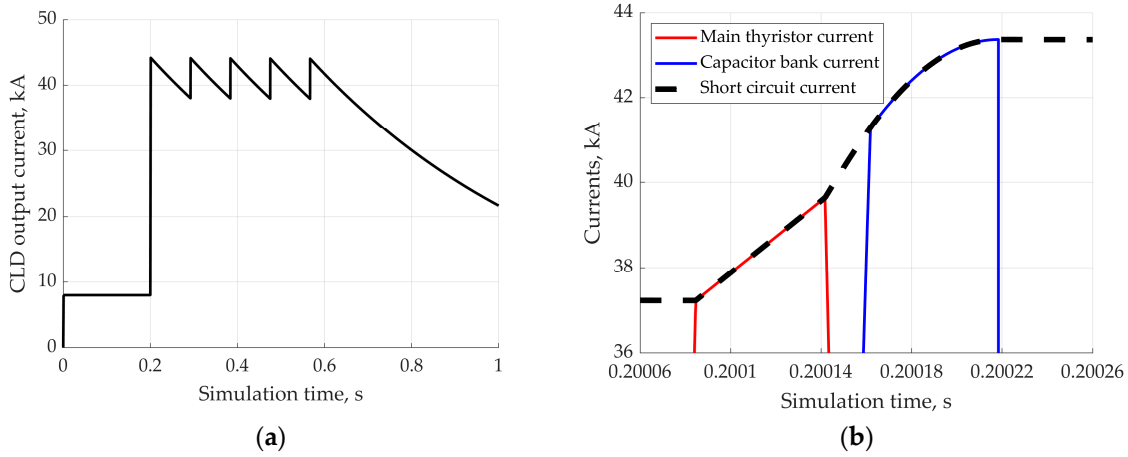
Figure 15. A comparison of the computer simulation and experimental results. (**a**) The output current of the current-limiting device. (**b**) The transients in the CLD at the time of artificial switching of the thyristor and the CB discharge.

Figure 15 shows that the maximum and minimum limited current values are not consistent throughout the operation time of the CLD. This circumstance is due to the gradual discharge of C_{PCSB}. However, the high accuracy of the model indirectly indicates the validity of the mathematical system discussed in detail in Section 3 of this article. The average deviation of the model results from the experiment for different settings was as follows: U = 606 V, F = 81 Hz—3.09%; U = 502 V, F = 36 Hz—3.53%; U = 405 V, F = 36 Hz—4.88%; U = 302 V, F = 36 Hz—4.52%; U = 502 V, F = 81 Hz—3.95%; U = 402 V, F = 81 Hz—3.89%; U = 301 V, F = 81 Hz—10.09%; U = 502 V, F = 49 Hz—3.18%; U = 405 V, F = 49 Hz—4.78%; U = 306 V, F = 49 Hz—5.46%.

6. A Simulation of a High-Power Prototype of the Current-Limiting Device

The ability to connect semiconductor devices in series/parallel allows you to flexibly control the power of the switches. This allows for the creation of a current-limiting device for a wide range of voltages and normal and fault currents. The reactor (10 in Figure 3) power at the CLD output is also relatively easy to scale.

At the moment, a prototype of the described device is being developed for approximately the following system parameters: mains voltage of 600 V, rated current of 8 kA, and steady-state short-circuit current of 200 kA. The electrical parameters of the circuit of the prototype under development are as follows: the electrical capacitance of the resonant loop capacitor: C_{RSB} = 1 mF; the current maintenance loop inductance: L = 9.5 μH; the CLD operating frequency: f = 20 Hz; and the time of the switched-on state of the main thyristor: t_{on} = 60 μs. The set task is to limit the short-circuit current to 40 kA during 400 ms with a current ripple of no more than 15%. The results of modeling the circuit for such parameters are shown in Figure 16.



(**a**) (**b**)

Figure 16. The simulation results of a powerful prototype of a current-limiting device. (**a**) The output current of the current-limiting device. (**b**) The transients in the CLD at the time of artificial switching of the thyristor and the CB discharge.

When selecting the parameters of the high-power prototype, a lot of attention must be paid to the two most critical aspects: calculating the resistance of the semiconductor devices to significant current overloads [27] (main thyristor and diode of the current maintenance circuit) and calculation of the permissible load of capacitor banks of the resonant circuit.

7. Potential Future Research

This article is the second in a series devoted to the use of semiconductor converter systems for limiting emergency currents. The first paper addressed the issue of improving the control of energy dissipation in semiconductor devices for CLD [27]. Special computer models were developed for this purpose. These models take into account the influence of temperature on the change in the volt-ampere characteristics of the diode/thyristor. A method for calculating the parameters of the thermal circuit of the diode/thyristor was also proposed. At the moment, the authors consider the following issues to be most important:

- The mathematical model does not describe the influence of the external parameters of the power system. From the point of view of the reliable operation of the CLD, it is necessary to take into account the parameters of the short-circuit current source (synchronous generator, storage battery, etc.). It is also necessary to pay attention to the rest of the energy system because complex cases of short circuits may require adjustment to the operating mode of the CLD.

- During the operation of a current-limiting device, semiconductor devices switch many times to a current that is many times greater than the rated current of the device over a relatively short period of time. Significant current values, current speed, and changes in pn-junction temperature have a strong impact on the process of turning off a semiconductor device—recovery current curve parameters. It is necessary to study the influence of this process on the reliability of the CLD.
- Some settings of the parameters of the electric circuit (for certain systems) require high speeds of switching on the semiconductor devices, since relatively short time intervals of the main switch-on state are necessary. In other words, the time of full switching on and the required time of the on state are values of the same order. Since this switching time also depends on the operating mode of the device, there is a need for its precise control using computer modeling of the CLD operation.
- For the above-described phenomena, it is necessary to create accurate mathematical and computer models in order to create a functional digital twin of the semiconductor CLD.

8. Conclusions

The analysis of power systems of autonomous and isolated complexes demonstrates the problem of reliability of power supply to consumers in cases of short circuits. To increase reliability, it is most advantageous to limit the short-circuit current for a sufficient time (the time during which the system switches to emergency power supply circuits). For this purpose, this paper proposes an electrical diagram of a semiconductor current-limiting device based on a step-down DC-DC converter, where the main switch is a thyristor with an artificially switched circuit. An important advantage of this circuit is the flexibility of its parameters, which makes it possible to manufacture a current-limiting device for a wide range of power systems.

Based on a detailed consideration of the stages of CLD operation, a mathematical model of the device was created. This model allows for the assessment of the influence of the electrical parameters of the circuit on the characteristics of the limited current: the magnitude of ripples and the minimum and maximum values. This model was verified and validated by the results of modeling the circuit in MATLAB Simulink and the results of experiments. Also, in general, the effectiveness of the current limitation by the proposed circuit has been experimentally confirmed.

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9. Patents

Based on the work described in this manuscript, patent RU226244U1 was obtained. URL: https://patents.google.com/patent/RU226244U1/en (accessed on 23 December 2024).

Author Contributions: Conceptualization, V.Y.F.; Data curation, E.P.S.; Formal analysis, E.P.S.; Investigation, E.P.S.; Methodology, A.V.B. and R.S.D.; Project administration, V.Y.F.; Resources, E.P.S.; Software, E.P.S.; Supervision, V.Y.F.; Writing—original draft, E.P.S.; Writing—review and editing, V.Y.F. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: The data will be made available on request.

Conflicts of Interest: The authors declare no conflicts of interest.

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