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A Modulation Strategy for Suppressing Current Ripple in H7 Current Source Inverters Through Coordinated Switching Operations

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Abstract: The DC bus current ripple is a critical performance parameter affecting the operation of current source inverters (CSIs). In high-power applications, CSIs often operate at lower switching frequencies to minimize losses. However, maintaining low levels of DC bus current ripple necessitates the use of large inductors on the DC side, which increases the size, weight, and cost of the system. This paper first explores the inherent limitations of conventional CSI designs. Subsequently, it proposes a hierarchical coordinated switching modulation strategy based on the H7 current source inverter (H7-CSI) to address the issue of DC bus current ripple. By segmenting the zero-vector states, the proposed method fully utilizes the modulation freedom of the H7-CSI, achieving high-frequency chopping effects on the DC-side current. Experimental results show that the new modulation strategy reduces the amplitude of DC bus current ripple to 43% of that achieved by conventional CSIs under similar switching loss conditions. Furthermore, the dynamic performance of the proposed scheme remains consistent with conventional CSIs. Spectrally, this method exhibits improved performance in the low-frequency range and slightly degraded performance in the high-frequency range, although the latter remains within acceptable limits.

Keywords: current source inverter; current ripple; modulation

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1. Introduction

In recent years, the application of three-phase current source inverters (CSIs) has been promoted in various fields, especially in renewable energy generation [1–4], electric vehicles [5,6], and motor drives [7,8]. With the popularization of new energy technologies and the rise of the electrization trend, CSIs have become an important component in these systems due to their unique advantages, such as their high reliability and fault tolerance capability in medium-power applications. In photovoltaic systems and wind power generation [9–14], the power quality and stability are particularly important for power conversion, and CSIs can better adapt to the grid requirements through their constant output current characteristic. Furthermore, in the drive and onboard charging systems of electric vehicles [15], the efficient current control and modular design of inverters can effectively improve the performance of the whole system [16,17].

As the application scope and demand of three-phase CSIs expands, the issue of current ripple has gradually become a focal point [18]. Current ripple refers to the fluctuating

component in the inverter's current, which not only affects power quality but also negatively impacts the equipment's lifespan. In grid-connected power generation systems, excessive current ripple may lead to instability in the power system and even compromise the operational stability of other grid-connected equipment [19]. In motor drive applications, current ripple can also directly affect motor efficiency and increase electromagnetic interference [20]. Obviously, suppressing the current ripple has become a key challenge for improving CSI systems' performance.

In practical applications, increasing the switching frequency and adding DC inductance value are the conventional primary means for suppressing current ripple. However, these two methods have contradictory effects on the performance of the converter and are usually hard to balance. On the one hand, the higher the switching frequency, the greater the switching losses. On the other hand, low switching frequency requires the inverter to increase the DC bus inductance, which may lead to larger space/weight occupation and higher costs.

To solve the ripple problem, many scholars have made fruitful attempts. Shen et al. proposed method that can reduce current ripple by constructing a current sampling window that satisfies the minimum sampling time and obtaining the mean value of two sampling values in the in-phase dynamic current [21]. Amol et al. optimized voltage ripple in VSIs by dynamically sequencing PWM based on instantaneous DC capacitor current polarity, without affecting the AC current ripple [22]. Baumann et al. proposed a method of intelligently setting zero vectors to reduce ripple, but it involved a high number of switching operations, increasing the switching losses [23]. Another approach is to adjust the action time of each vector within a switching cycle to suppress the DC-side current ripple. This method employs a Z-source inverter, as mentioned in [24,25]. In [26], a method was introduced that reduces current ripple by predicting the ripple with a variable switching frequency. However, this approach involves a complex algorithm, a large filtering device, and significantly increased switching losses. A coordinating–gating–sequence method was proposed in [27], which gives a solution for back-to-back current source converters. A more recent method to reduce current ripple is presented in [28]; it eliminates the use of zero vectors and instead synthesizes the required current vector using three non-zero vectors, thereby reducing the slope change of the current variation to lower ripple. The switching losses of this method are identical to those of the conventional CSIs using the seven-segment space vector pulse-width modulation (SVPWM) technique. In order to reduce the switching losses, the H7 current source inverter (H7-CSI) technique was proposed in [29], presenting a more flexible way to achieve the zero vectors and giving the CSI greater potential to improve its output performance.

Inspired by the above findings, this paper proposes a new modulation method based on H7-CSI, which can effectively suppress the current ripple while retaining acceptable switching losses. This paper is organized as follows: First, the common features of DC-side current ripple for CSIs are analyzed and discussed. Then, the proposed current ripple suppression strategy based on H7-CSI using hierarchical coordinated switching modulation is demonstrated in detail. Finally, simulations and experimental tests validate the effectiveness of the proposed method.

2. Commutation and Current Ripple Features of CSIs

The topology of a conventional current source inverter is shown in Figure 1. Because the commutation bridge consists of six power switches, the inverter is also called H6-CSI. The DC circuit comprises a DC voltage source U_{dc} in series with an inductor L_{dc}. The AC output is filtered by three capacitors C_a, C_b, and C_c and inductors L_a, L_b, and L_c. The power

switches S_1–S_6 retain the configuration scheme of reverse-blocking devices, such as GTO, IGCT, or RB-IGBT modules.

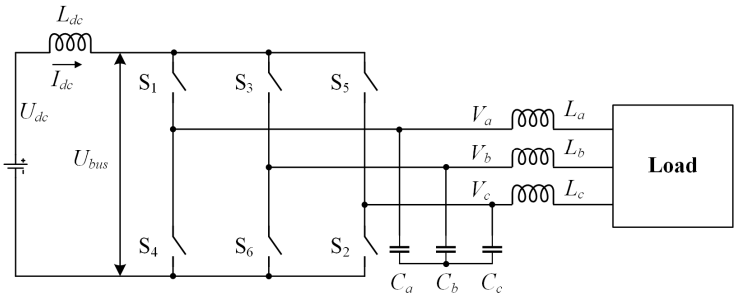


Figure 1. A schematic diagram of conventional H6-CSI topology.

The current source inverter has nine switching states, as shown in Figure 2. It consists of six active vectors (I_1–I_6) and three zero vectors (I_7–I_9). I_{ref} is the reference current vector. The DC-link inductor current ripple can be derived from

$$\Delta i = \frac{U_{dc} - U_{bus}}{L_{dc}} \Delta t \tag{1}$$

where U_{bus} is the output voltage after the DC inductor, and Δt is the charging/discharging dwell time of the inductor current.

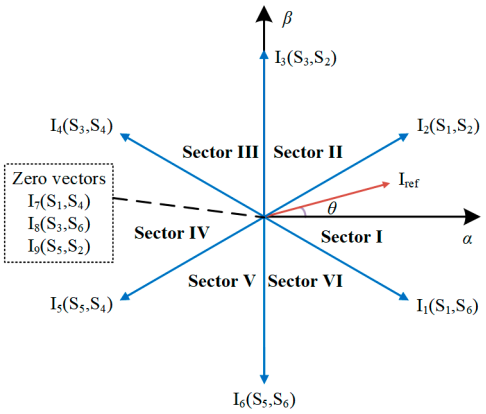


Figure 2. Current space vector diagram.

The switching states and the corresponding voltages of the H6-CSI are listed in Table 1. The three-phase line voltages can be represented as follows:

$$\begin{cases} U_{ab} = \sqrt{3} U_m \sin\left(\omega t + \frac{\pi}{6}\right) \\ U_{bc} = \sqrt{3} U_m \sin\left(\omega t - \frac{\pi}{2}\right) \\ U_{ca} = \sqrt{3} U_m \sin\left(\omega t + \frac{5\pi}{6}\right) \end{cases} \tag{2}$$

where U_m and ω represent the phase voltage amplitude and angular frequency, respectively.

Generally, the reference vector is synthesized by two adjacent active vectors and one zero vector. Taking Sector I as an example, the dwell time of the three vectors can be calculated as follows:

$$\begin{aligned} T_1 &= m T_s \sin\left(\theta + \tfrac{5\pi}{6}\right) \\ T_2 &= m T_s \sin\left(\theta + \tfrac{\pi}{6}\right) \\ T_0 &= T_s - T_1 - T_2 \end{aligned} \tag{3}$$

where m is the modulation index, T_s is the switching period, and θ is the reference vector angle. T_1, T_2, and T_0 are the dwell times of I_1, I_2, and I_0, respectively.

Table 1. Conventional H6-CSI switching stage and output voltage.

	S_1	S_2	S_3	S_4	S_5	S_6	U_{bus}
I_1	ON	0	0	0	0	ON	U_{ab}
I_2	ON	ON	0	0	0	0	$-U_{ca}$
I_3	0	ON	ON	0	0	0	U_{bc}
I_4	0	0	ON	ON	0	0	$-U_{ab}$
I_5	0	0	0	ON	ON	0	U_{ca}
I_6	0	0	0	0	ON	ON	$-U_{bc}$

Figure 3 shows the relationship between the output voltage U_{bus} (vertical axis) and the reference vector angle θ (horizontal axis). The distribution of each space sector is also illustrated in the figure.

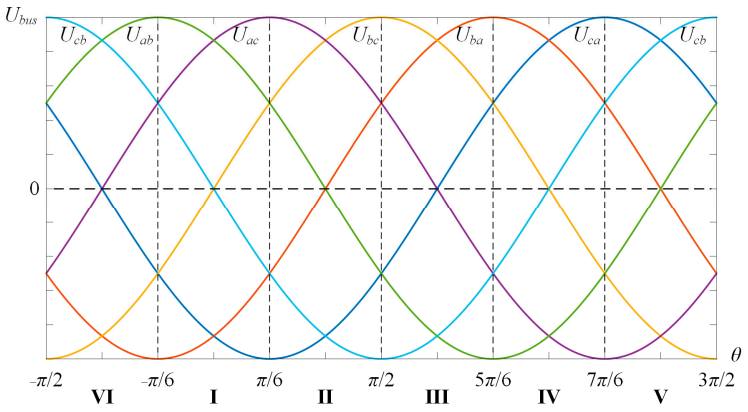


Figure 3. Illustration of the reference vector angle and its output voltage.

Figure 4 gives a zoomed view of the relationship between the line voltage and the DC voltage U_{dc} in Sector I, where U_{L-m} is the line voltage amplitude and m is the modulation index. Taking Sector I as an example, when S_1 and S_6 are ON (vector I_1), the output voltage U_{bus} after the DC inductor can be given by

$$U_{bus} = U_{ab} = U_{L-m} \sin\left(\theta + \frac{2\pi}{3}\right) \tag{4}$$

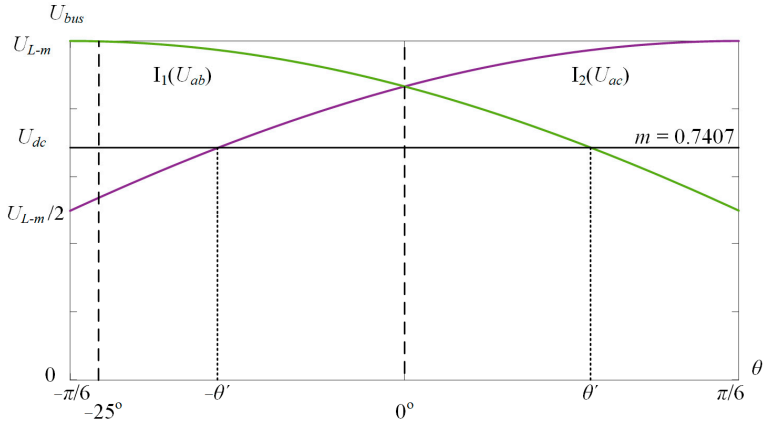


Figure 4. The relationship between the line voltage and the DC voltage in Sector I.

When S_1 and S_2 are ON (vector I_2), the output voltage U_{bus} is

$$U_{bus} = -U_{ca} = U_{L-m} \sin\left(\theta + \frac{\pi}{3}\right) \tag{5}$$

When S_1 and S_4 are ON (vector I_7), the output voltage U_{bus} is

$$U_{bus} = 0 \tag{6}$$

Ignoring the power dissipation of the conversion, $U_{dc} = \frac{3}{2} m U_m$. Based on the above analysis, the DC-side current ripple can be expressed as follows:

$$\begin{cases} \Delta I_1 = \frac{U_{dc}-U_{bus}}{L_{dc}} \frac{T_0}{4} = \frac{U_{dc}}{L_{dc}} \frac{T_0}{4} \\ \Delta I_2 = \frac{U_{dc}-U_{bus}}{L_{dc}} \frac{T_1}{2} = \frac{U_{dc}-U_{L-m}\sin\left(\theta+\frac{2\pi}{3}\right)}{L_{dc}} \times \frac{mT_s \sin\left(\theta+\frac{\pi}{6}\right)}{2} \\ \Delta I_3 = \frac{U_{dc}-U_{bus}}{L_{dc}} \frac{T_2}{2} = \frac{U_{dc}-U_{L-m}\sin\left(\theta+\frac{\pi}{3}\right)}{L_{dc}} \times \frac{mT_s \sin\left(\theta+\frac{5\pi}{6}\right)}{2} \\ \Delta I_4 = \frac{U_{dc}-U_{bus}}{L_{dc}} \frac{T_0}{2} = \frac{U_{dc}}{L_{dc}} \frac{T_0}{2} \\ \Delta I_5 = \Delta I_3 = \frac{U_{dc}-U_{L-m}\sin\left(\theta+\frac{\pi}{3}\right)}{L_{dc}} \times \frac{mT_s \sin\left(\theta+\frac{5\pi}{6}\right)}{2} \\ \Delta I_6 = \Delta I_2 = \frac{U_{dc}-U_{L-m}\sin\left(\theta+\frac{2\pi}{3}\right)}{L_{dc}} \times \frac{mT_s \sin\left(\theta+\frac{\pi}{6}\right)}{2} \\ \Delta I_7 = \Delta I_1 = \frac{U_{dc}}{L_{dc}} \frac{T_0}{4} \end{cases} \tag{7}$$

From Equation (7) and Figure 4, it can be seen that the current ripple fluctuation can be divided into two modes: Mode 1 is located in the interval $(-\theta', \theta')$, while Mode 2 is located between the intervals $(-\frac{\pi}{6}, -\theta')$ and $(\theta', \frac{\pi}{6})$. The boundary angle θ' can be obtained through Equation (8):

$$U_{bus} = U_{L-m}\sin(\theta\prime + \frac{2\pi}{3}) = U_{dc} \tag{8}$$

Obviously, Mode 2 only exists when m is greater than $\frac{\sqrt{3}}{3}$ (under the unity power factor condition). Taking 0° and -25° as examples, and employing the seven-segment SVPWM, these two modes of current ripple are illustrated in Figure 5.

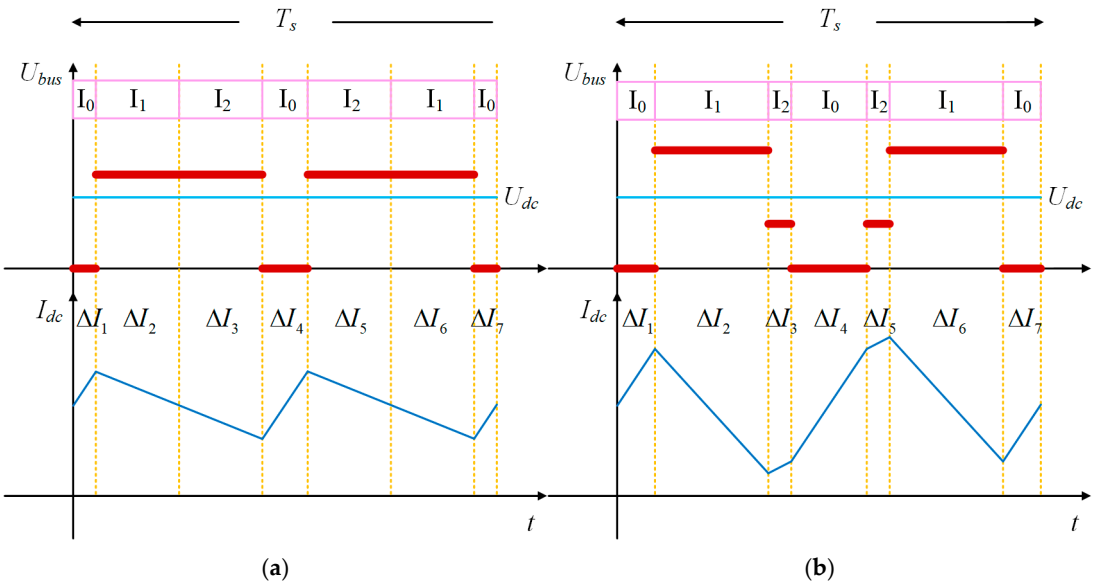


Figure 5. Current ripple waveform examples: (**a**) Mode 1 ($\theta = 0^\circ$); (**b**) Mode 2 ($\theta = -25^\circ$).

As shown in Figure 5a, in Mode 1, the vector I_1 and the vector I_2 correspond to the inductance releasing energy state, leading to a downward fluctuation in the DC-side current, and the vector I_7 corresponds to the inductive energy storage state, leading to an upward fluctuation in the DC-side current. By contrast, in Mode 2, as shown in Figure 5b, the vector I_2 corresponds to the inductive energy storage state, leading to upward fluctuation, which

a the similar trend to vector I_7. Thus, the maximum value of the DC-side current ripple for the conventional H6-CSI with seven-segment SVPWM can be expressed as follows:

$$\Delta I_{\text{peak}-1} = \begin{cases} 2\Delta I_3 + \Delta I_4 & -\frac{\pi}{6} \le \theta < -\theta' \\ \Delta I_4 & -\theta' \le \theta < \theta' \\ 2\Delta I_1 + 2\Delta I_2 & \theta' \le \theta \le \frac{\pi}{6} \end{cases} \tag{9}$$

Based on the conventional H6-CSI, the H7-CSI offers an alternative technical approach for the commutation of converters. The H7-CSI topology is drawn in Figure 6. This topology can be divided into two stages: the front end and the rear end. The front-end stage consists of a DC voltage source U_{dc}, a series-connected inductor L_{dc}, and a parallel-connected power switch S_7. The rear-end stage circuit is the same as the conventional H6-CSI structure. It should be noted that the power switch S_7 should be selected as a fully controllable device with high-speed switching capability.

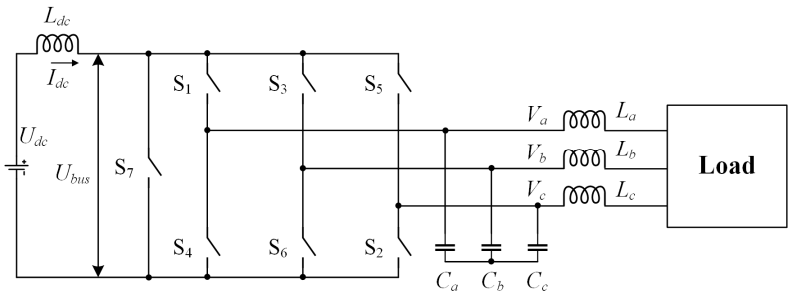


Figure 6. A schematic diagram of the H7-CSI topology.

The H7-CSI has a unique advantage that can control the presence of zero vectors using only the switch S_7, resulting in the conventional zero vectors (I_7, I_8, and I_9) being uniformly denoted as I_0. A typical modulation method is to use S_7 to realize the zero-current-switching (ZCS) capability for the rear-end switches, which is shown in Figure 7.

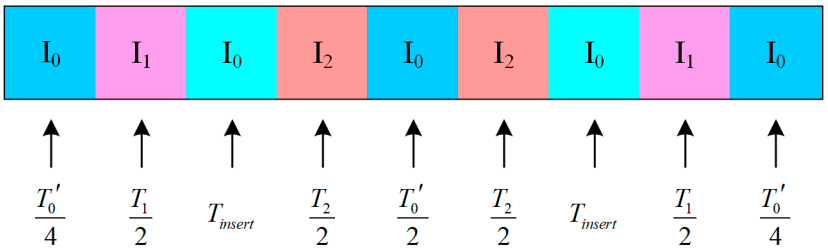


Figure 7. Typical modulation sequence of H7-CSI with ZCS insertion.

As shown in Figure 7, T_{insert} is the time interval inserted between the two different active vector states. During this time interval, the rear-end switches (S_1–S_6) can be operated with zero-current-switching (ZCS) capability, which helps significantly improve efficiency. Therefore, the H7-CSI can be configured with hybrid switches, where the front end can be selected with a low-switching-loss switch and the rear-end part employs high-power but cheap devices. The rest of the zero vector dwell time is denoted as T_0', and all of the switching states are formed into a nine-segment modulation sequence.

As for the current ripple of the H7-CSI, its fluctuation trend is almost the same as that of the conventional H6-CSI. The only difference is the inserted zero vector, which leads to an additional rise in the current ripple. If the current ripple fluctuation of the inserted zero vector is ΔI_8, then the time-domain expression of the DC-side current ripple can be

calculated as shown in Equation (10), and the maximum value of the DC-side current ripple can be expressed as shown in Equation (11):

$$\begin{cases} \Delta I_1 = \frac{U_{dc}-U_{bus}}{L_{dc}}\frac{T_0'}{4} = \frac{U_{dc}}{L_{dc}}\frac{T_0'}{4} \\ \Delta I_2 = \frac{U_{dc}-U_{bus}}{L_{dc}}\frac{T_1}{2} = \frac{U_{dc}-U_{L-m}\sin\left(\theta+\frac{2\pi}{3}\right)}{L_{dc}} \times \frac{mT_s\sin\left(\theta+\frac{\pi}{6}\right)}{2} \\ \Delta I_3 = \frac{U_{dc}-U_{bus}}{L_{dc}}\frac{T_2}{2} = \frac{U_{dc}-U_{L-m}\sin\left(\theta+\frac{\pi}{3}\right)}{L_{dc}} \times \frac{mT_s\sin\left(\theta+\frac{5\pi}{6}\right)}{2} \\ \Delta I_4 = \frac{U_{dc}-U_{bus}}{L_{dc}}\frac{T_0'}{2} = \frac{U_{dc}}{L_{dc}}\frac{T_0'}{2} \\ \Delta I_5 = \Delta I_3 = \frac{U_{dc}-U_{L-m}\sin\left(\theta+\frac{\pi}{3}\right)}{L_{dc}} \times \frac{mT_s\sin\left(\theta+\frac{5\pi}{6}\right)}{2} \\ \Delta I_6 = \Delta I_2 = \frac{U_{dc}-U_{L-m}\sin\left(\theta+\frac{2\pi}{3}\right)}{L_{dc}} \times \frac{mT_s\sin\left(\theta+\frac{\pi}{6}\right)}{2} \\ \Delta I_7 = \Delta I_1 = \frac{U_{dc}}{L_{dc}}\frac{T_0'}{4} \\ \Delta I_8 = \frac{U_{dc}-U_{bus}}{L_{dc}}T_{insert} = \frac{U_{dc}}{L_{dc}}T_{insert} \end{cases} \tag{10}$$

$$\Delta I_{\text{peak}-2} = \begin{cases} 2\Delta I_3 + \Delta I_4 + 2\Delta I_8 & -\frac{\pi}{6} \le \theta < -\theta' \\ \Delta I_4 & -\theta' \le \theta < \theta' \\ 2\Delta I_1 + 2\Delta I_2 + 2\Delta I_8 & \theta' \le \theta \le \frac{\pi}{6} \end{cases} \tag{11}$$

Upon a comprehensive comparison between the H6-CSI and H7-CSI topologies, several key points emerge: The H6-CSI represents a classic structure with a relatively lower count of components, where each power switch performs identical commutation functions. In contrast, the H7-CSI incorporates an additional power switch, which introduces a slight disadvantage in terms of cost. However, this extra switch enables the execution of zero-vector states through S_7, offering more diverse implementations of the zero vector and resulting in reduced conduction losses. Furthermore, by adjusting the modulation sequence, it is possible to allocate all switching losses to S_7. Consequently, the H7-CSI circuit can demonstrate significant efficiency advantages with an appropriate configuration strategy.

3. Hierarchical Coordinated Switching Modulation Strategy

It is obvious that the zero-vector states can greatly affect the current ripple of the CSI. Fortunately, the H7-CSI topology provides a simple and easy way to enhance the flexibility of zero-vector commutation. As a result, it gives an extra freewheeling option to implement the zero vectors, which allows the zero-vector sates to be inserted at any position among the vector sequences. Therefore, S_7 and the rear-end switches (S_1–S_6) can be operated in parallel in a hierarchical manner. That is, the rear-end switches (S_1–S_6) can keep minimal switching counts (with ZCS) to realize the interphase commutation, while S_7 can be operated with a much higher switching frequency, aiming to adjust the current ripple.

Inspired by the above analysis and discussion, it is necessary to investigate the S_7 regulation scheme of current ripple in detail. The ideal choice for S_7 should be a self-controlled switch with high speed and low switching loss characteristics, and obviously SiC MOSFET would be a good choice. In terms of the hardware costs, it is worth noting that, compared to the conventional H6-CSI, the proposed modulation solution with the H7-CSI introduces only one additional power switch, S_7 (along with its series-connected diode D_7). The cost associated with implementing this solution primarily stems from the inclusion of the SiC device. While SiC components are generally more expensive than their silicon counterparts, they offer significant advantages in terms of reduced losses, higher operating frequencies, and improved thermal performance. Therefore, the additional cost associated with the proposed method is manageable and targeted towards enhancing system performance without necessitating a complete overhaul of the existing infrastructure. The use of SiC devices, despite their higher upfront cost, aligns well with the requirements of medium-power applications, where their benefits are most pronounced.

According to the datasheets, under the same power rating, the switching loss of most SiC switches is about 1/5 to 1/10 of that of the Si switches (taking into account both 25 °C and 175 °C junction temperatures) [30]. The conventional H6-CSI with seven-segment SVPWM has six hard switching counts, which can be taken as the standard for comparison. Then, to guarantee the same power dissipation level, the upper-limited switching count of S_7, which can be inserted into the modulation sequence, is theoretically up to 30. Obviously, there is great potential for the distribution of zero vectors.

Among all of the working statuses for synthesizing the reference vector, the easiest way to reduce the ripple is to use S_7 evenly allocated into the two active vector states, which is also the most common method to manage the current ripple. Because of the symmetry of each sector, the modulation strategy can be described by only half of one sector. Taking the modulation in the half of Sector I (θ located between $(0, \frac{\pi}{6})$) as an example, Figure 8 illustrates this common situation, which is denoted here as Distribution-method 1 (D1).

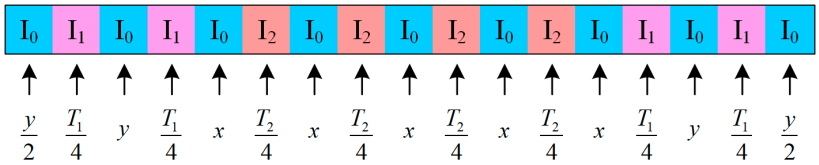


Figure 8. Illustration of Distribution-method 1 for one period.

Compared to Figure 7, the active vector states have been divided by the inserted I_0. The number of insertion times is determined by the actual requirement of the ripple range to be reduced, which has to ensure that the S_7 switching counts can be within the allowable range of switching loss. In this illustration of the example, there are nine zero-vector states, aiming to reduce the current ripple to less than half. The allocation of the zero-vector states is based on the ratio of T_1 to T_2. Let x represent the dwell time of one inserted zero-vector state allocated to T_1 proportionally, while y represents the dwell time of one inserted zero-vector state allocated to T_2 proportionally. Thus, the expression for the distribution of the zero vector states is as follows:

$$5x + 3y = T_0 \tag{12}$$

Then, x and y can be derived as follows:

$$\begin{cases} x = \frac{T_2}{5(T_1+T_2)} \cdot T_0 \\ y = \frac{T_1}{3(T_1+T_2)} \cdot T_0 \end{cases} \tag{13}$$

where T_0 represents the total dwell time for the zero-vector states.

However, there exist some special statuses that can significantly affect the ripple-suppressing performance. Near the edge of each sector, one of the dwell times of the active vectors will be very short, which produces very little effect on the overall ripple. As illustrated in Sector I, when the reference vector crosses from Sector I to the edge of Sector II, T_1 becomes significantly smaller than T_2. Therefore, the method for distributing zero-vector states needs to be adjusted accordingly.

It is worth noting that there are two possible current ripple fluctuation cases, whose current ripple fluctuation waveforms at the edge of each sector correspond to Mode 1 and Mode 2 described above. The choice between the two cases depends on whether the modulation index m is greater than $\frac{\sqrt{3}}{3}$. Figure 9 presents the schematic diagram of the sector partition that implements the proposed hierarchical coordinated switching modulation strategy in Sector I. In Figure 9, D2 and D3 denote Distribution-method 2 and Distribution-method 3, which will be elaborated on next.

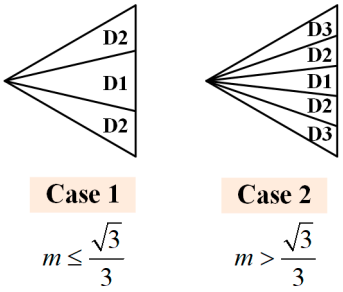


Figure 9. Schematic diagram of the sector partition for the proposed modulation method.

Case 1 ($m \leq \frac{\sqrt{3}}{3}$):

At the edge of Sector I, vector I_1 leads to the downward current fluctuation, and the allocation scheme of zero-vector states (Distribution-method 2) is illustrated in Figure 10.

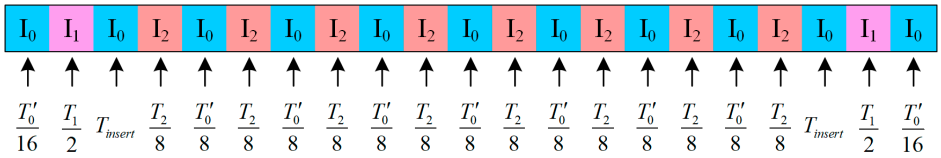


Figure 10. Illustration of Distribution-method 2 for one period.

The total number of S_7 insertion times should follow the following principle: the main active vector that can greatly affect the current ripple should be divided into approximately the same number of segments as the two active vector states in D1, in order to maintain roughly the same current ripple level. In the example of Figure 10 presented here, 10 zero-vector states exist, and their dwell times are listed. The T_{insert} section is used to implement ZCS; its dwell time is determined by T_1 and is used to offset the rising ripple fluctuations caused by I_1. T_0' refers to the total dwell time of the rest of zero vector. Therefore, T_{insert} and T_0' can be derived as follow:

$$\begin{cases} T_{insert} = \frac{T_1}{2} \cdot \frac{(U_1 - U_{dc})}{U_{dc}} \\ T_0\prime = T_0 - 2T_{insert} \end{cases} \tag{14}$$

where U_1 is the line voltage corresponding to I_1, and T_1 is the total dwell time of I_1.

At the boundary between D1 and D2, the fluctuation in the current ripple caused by I_1 should be equal to that of one I_2 segment. At this point, the specific dividing angle can be obtained by calculation using Equation (15):

$$\frac{T_1}{8} \cdot \frac{(U_{dc} - U_1)}{L_{dc}} = \frac{T_2}{2} \cdot \frac{(U_{dc} - U_2)}{L_{dc}} \tag{15}$$

Case 2 ($m > \frac{\sqrt{3}}{3}$):

Under this modulation index condition, as the reference vector rotates from the center of the sector towards the edge, the current ripple corresponding to I_1 will gradually shift from a downward trend to an upward trend, indicating that its slope will gradually transition from a negative value to a positive value. At the critical point of its slope transition, there will be a transient status similar to Case 1, so D1 and D2 are delimited in exactly the same way as Case 1.

After that, at the edge of Sector I, the current ripple will completely change to the waveform of Mode 2. Since the current ripple corresponding to I_1 has a similar upward trend to that of the zero-vector states, there is no need to use S_7 for insertion segmentation. Distribution-method 3 can be executed at this stage, as illustrated in Figure 11.

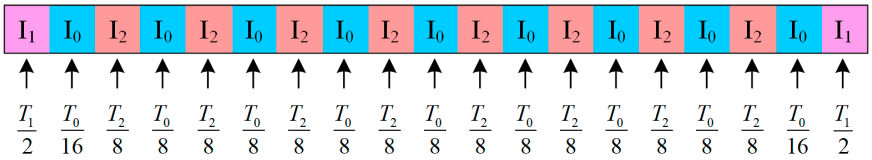


Figure 11. Illustration of Distribution-method 3 for one period.

In this presented example, there are 11 zero-vector states in the one-period modulation sequence, and the dwell times of each interval are listed. The boundary angle between the D2 and D3 regions depends on the zero-crossing transition time of I_1's slope, which can be obtained through Equation (8). It is noteworthy that, in actual engineering applications, the modulation ratio of CSIs is usually not set very low, so Case 2 will be more commonly used.

As illustrated in Figures 5 and 7 and Equations (1)–(11), the maximum current ripple appears at the edge of each sector and is related to the DC-side inductor and the dwell time of certain space vector states. As for the proposed modulation scheme, taking Sector I as an example, the peak value of current ripple can also be found at the end of the sector, where the modulation sequence is as illustrated in Figure 11. Therefore, the peak value of current ripple can be evaluated as follows:

$$\Delta^* I_{\text{peak}} = \frac{U_{dc}}{L_{dc}} \frac{T_0}{8} + \frac{U_{dc} - U_{bus}}{L_{dc}} T_1 \tag{16}$$

To be more specific, compared with the conventional H6-CSI, when the modulation frequency is set at 2 kHz and m is down to 0.876, the current ripple of the proposed modulation scheme will be reduced by half. In other words, under the same ripple requirements, the proposed H7-CSI modulation strategy can reduce the DC-side inductor to half of that required for the conventional H6-CSI solution.

4. Experimental Verifications

To verify the performance of the proposed modulation solution, an experimental prototype was built, as shown in Figure 12. The H7-CSI utilizes a SiC MOSFET (C2M0040120D from Cree, Inc., Durham, NC, USA) as S_7 and employs 6 IGBTs (FF100R12RT4 from Infineon Technologies AG, Neubiberg, Bavaria, Germany) for the rear-end switches (S_1 to S_6). All switches are connected with SiC power diodes (C2D20120D from Cree, Inc., Durham, NC, USA) to ensure the reverse-blocking capability. The overlap time during commutation was set to 2 µs.

The CSI prototype adopts an active damping control strategy. The diagram of the control structure of the whole CSI system is illustrated in Figure 13. As shown in Figure 13, HPF represents the high-pass filter, which is used to filter out the fundamental frequency components in the capacitor voltage, while H_s is the active damping coefficient [31]. The DC-side current is controlled using a PI controller, and the resulting value serves as the reference for active power. For the closed-loop feedback of the output current on the AC side of the inverter, a PR (proportional–resonant) controller is employed, and the experimental parameters are listed in Table 2. The H7-CSI is powered by a 62024P-600-8 (Chroma ATE Inc., New Taipei City, Taiwan), which supplies 180 V DC voltage. To demonstrate the ripple suppression effect more clearly, the DC inductor was not set very large, with a value of 10 mH. The modulation period was configured as 500 µs, which indicates that the switching frequency for S_1–S_6 is 2 kHz. On the AC side, the filter capacitance and inductance of each phase were configured as 10 µF and 15 mH, respectively.

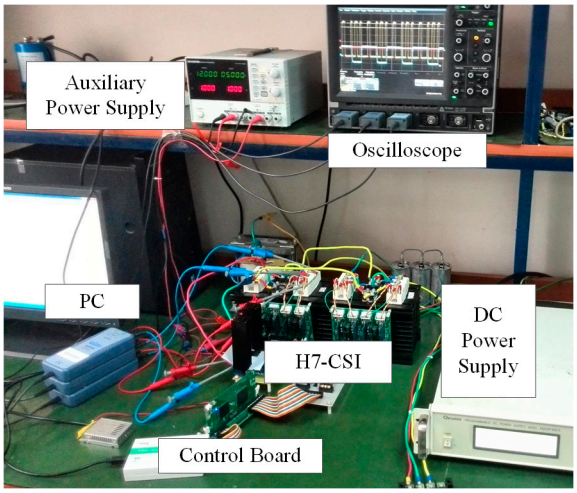


Figure 12. Experimental prototype.

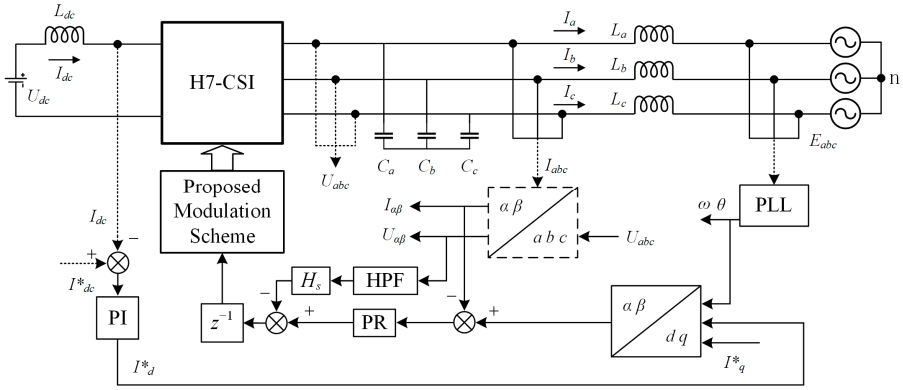


Figure 13. Diagram of the control structure.

Table 2. Experimental parameters.

Parameters	Values
Amplitude of phase voltage U_m	155 V
Modulation index m	0.77
DC voltage U_{dc}	180 V
Modulation period T_s	500 μs
DC inductance L_{dc}	10 mH
Filter inductance of one phase L	15 mH
Filter capacitance of one phase C	10 μF
Overlap time	2 μs

For the specific implementation of modulation, the actual number of insertions of the zero-vector states is the same as illustrated in the figures in Section 3. Since Case 2 includes all three distribution methods (D1, D2, D3) of proposed modulation, it was used as the experimental ripple pattern, with its modulation index set to 0.77. When the proposed hierarchical coordinated switching modulation strategy is implemented, the driving pulse of the H7-CSI is as depicted in Figure 14.

It can be seen from Figure 14 that the switching frequency of S_7 is significantly higher than that of the rear-end switches. Obviously, they perform the hierarchical coordinated operation with different switching frequencies.

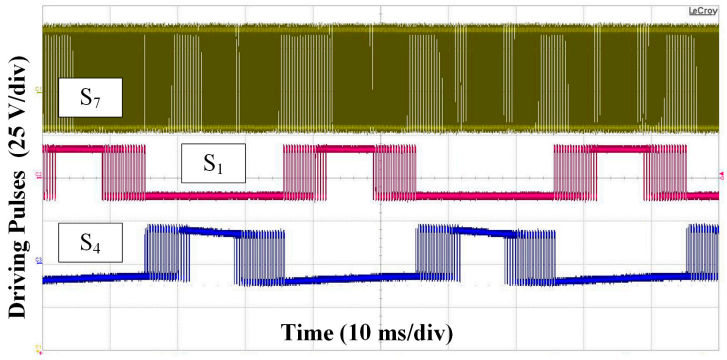
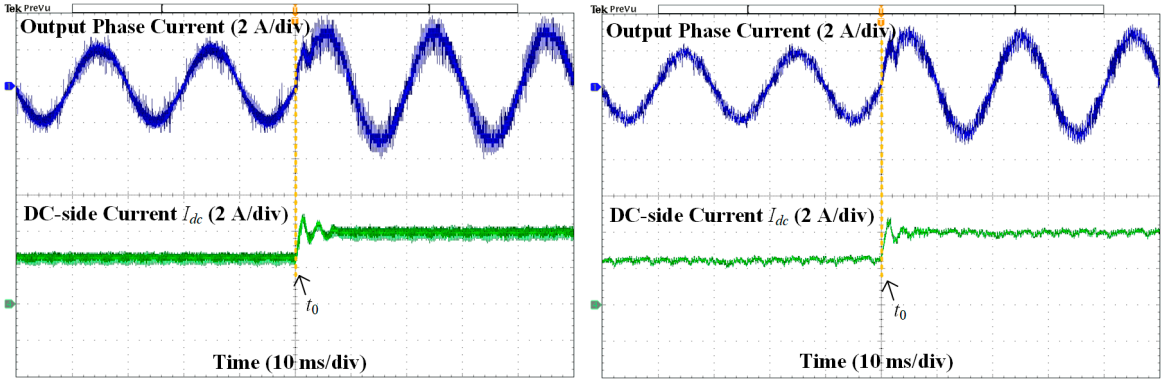


Figure 14. Driving pulses of the switches (S_1, S_4, S_7).

To evaluate the performance of current suppression and to compare it to the conventional H6-CSI solution, an H6-CSI prototype was also implemented using the same hardware suite as the H7-CSI. Figure 15 shows the two prototypes' experimental output phase current and DC-side current waveforms with load changes.



(**a**) (**b**)

Figure 15. Experimental waveforms of output phase current and DC-side current from: (**a**) conventional H6-CSI with 7-segment SVPWM and (**b**) H7-CSI with proposed modulation scheme.

Before t_0, both inverters output 50 Hz sinusoidal waves with an amplitude of 2 A, and they are supplied by a 2.5 A current on the DC side. At t_0, the experimental prototype adjusts the load current amplitude to 3 A, while keeping all hardware components of the circuit unchanged. The corresponding DC current is also increased to 4 A. The comparison results of the converters indicate that, both before and after the load change, the modulation strategy proposed in this paper can effectively reduce the DC current ripple. That is, the ripple of the H7-CSI was reduced to 43% of that of the H6-CSI, where the ripple of the H6-CSI was almost 0.7 A while that of the H7-CSI was about 0.3 A. The current waveforms of the H7-CSI appear thinner as a whole. Furthermore, the dynamic performance of the proposed modulation scheme seems similar to that of the conventional H6-CSI.

A detailed spectral analysis of the DC-side current was conducted when it was set at 4 A for the experimental prototype. The spectral comparison results are shown in Figure 16, indicating that the proposed modulation scheme demonstrates slightly better performance in the low-frequency region compared to the conventional H6-CSI scheme. However, in the high-frequency region, the spectral performance is somewhat inferior. This phenomenon can be attributed to the fact that the H7-CSI employs S_7 for high-frequency chopping, which aims to reduce current ripple.

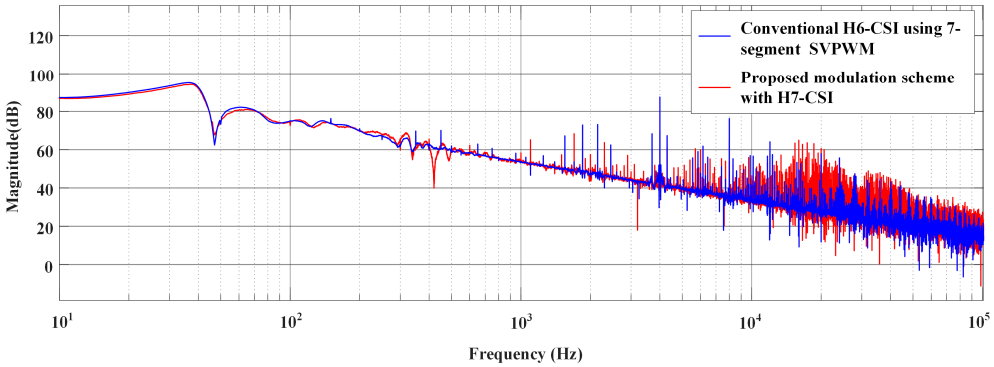


Figure 16. Spectral comparison of DC-side current.

The total harmonic distortion (THD) performances of the output phase current of both converters are drawn and compared in Figure 17, indicating that the THD values of the proposed method are slightly higher than those of the conventional H6-CSI. This phenomenon may be attributed to the two parallel hierarchical switching frequencies of H7-CSI, which would inevitably lead to its spectral distribution being more complicated than that of the conventional H6-CSI. Fortunately, it is worth noting that as the power increases, the gap between the two methods tends to narrow. This suggests that while there might be a slight increase in THD for the proposed method at lower power levels, its performance becomes more comparable to the conventional H6-CSI as the power rating rises.

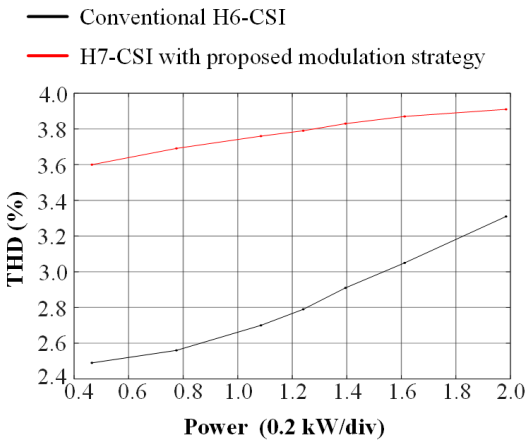


Figure 17. Graph of THD performance.

To go a step further, the working efficiency of both prototypes was tested under the same conditions using a power analyzer (PM6000 from Voltech Instruments, Inc., Fort Myers, FL, USA). The comparison results are drawn in Figure 18. The efficiency carves show that the H7-CSI with the proposed ripple suppression modulation scheme has a relatively higher efficiency compared to the conventional H6-CSI. This efficiency advantage stems from the fact that the number of S_7 switching counts in the modulation used in this experiment still has room for redundancy compared to the theoretical upper limit of the H6-CSI's switching loss. In other words, corresponding to the actual specific application scenario, the current ripple has the operational potential to be further suppressed.

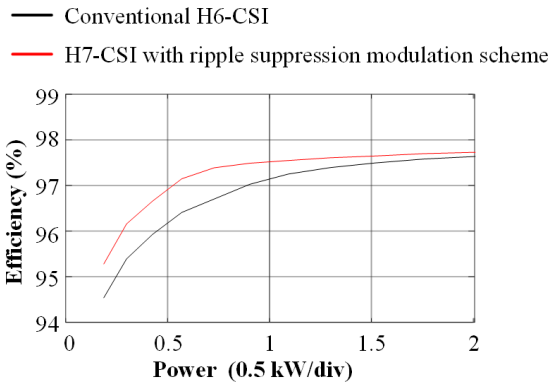


Figure 18. Graph of efficiency comparison.

5. Conclusions

This paper presents an in-depth investigation into the characteristics of current ripple in a current source inverter and introduces an innovative modulation strategy for effective ripple suppression based on the H7-CSI topology. By implementing hierarchical coordinated switching operations, the proposed modulation scheme enhances the high-frequency insertion capability of zero-vector states, resulting in a significant reduction in DC bus current ripple. This improvement is achieved without compromising conversion efficiency, as the proposed hardware configuration method addresses potential power loss concerns. The dynamic performance of the proposed scheme remains consistent with conventional CSIs. Spectrally, this method exhibits improved performance in the low-frequency range and slightly degraded performance in the high-frequency range, although the latter remains within acceptable limits. The effectiveness and performance of the proposed strategy were validated through experimental evaluations, demonstrating its practical applicability and potential for real-world implementation.

Author Contributions: W.W.: conceptualization, methodology, writing—review and editing, and supervision; L.W.: writing—original draft, formal analysis; X.F.: resources and project administration; X.L.: validation, investigation, writing—review and editing, and supervision; K.L.: software and visualization; X.X.: data curation and investigation. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: Author Xi Liang was employed by the PipeChina Northwest Company. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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