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Advanced Control Strategies for Enhancing the Performance of Phase-Shifted Full-Bridge Series Resonant DC–DC Converters in Photovoltaic Micro-Inverters

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Abstract: This article addresses the challenges of the reduced efficiency in phase-shifted full-bridge series resonant converters (PSFB-SRCs) used within micro-inverters (MIs), especially under light load and high input voltage conditions. To enhance performance, first-order and second-order time-domain equivalent models that accurately predict the output gain across a wide range of operating conditions are developed. A novel control strategy is proposed, featuring turn-on time as a feedback variable, with phase shift angle and dead time as feedforward variables, enabling precise computation of frequency, duty cycle, and phase shift time for digital controllers. This ensures optimal efficiency, stability, and dynamic response, regardless of the load conditions. Experimental results from the prototype confirmed zero-voltage switching under heavy loads and efficient frequency limiting under light loads, achieving a peak efficiency of 97.8% at a 25 V input. Notably, the light load efficiency remained above 90% even at a 50 V input. These contributions significantly advance PSFB-SRC technology, providing robust solutions for high-efficiency MI applications in photovoltaic systems.

Keywords: micro inverter; advanced control strategy; phase-shift full bridge; series resonant converter

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1. Introduction

With the global transition in energy structures and the rapid advancement of renewable energy, photovoltaic (PV) power generation has garnered significant attention for its clean and efficient characteristics [1]. Particularly in residential applications, micro-inverters (MIs) have become widely adopted as compact and efficient power conversion devices [2]. MIs excel in converting the direct current (DC) generated by PV modules into alternating current (AC), which can be directly supplied to users or fed into the grid. Unlike traditional centralized and string-type PV inverters, MIs provide maximum power point tracking (MPPT) and energy management at the component level [3]. This design offers several advantages, including high efficiency, enhanced safety, and ease of maintenance, making MIs an ideal choice for distributed PV systems.

The core strengths of MIs lie in their modularity and independence [4]. Each PV module can be paired with an individual MI, enabling each component to operate autonomously, without interference. This design simplifies system installation and maintenance, while enhancing the overall efficiency and reliability. Structurally, MIs are predominantly two-stage systems that decouple DC conversion from inversion [5]. The first stage performs

maximum power point tracking (MPPT) and converts the PV voltage to a bus voltage as high as 400 V. The second stage handles the DC/AC conversion and provides reactive power compensation, along with other functions.

As the core structure of MIs, the design of DC converters significantly influences the efficiency and quality of power conversion. Researchers have proposed various innovative DC conversion topologies, such as flyback [6,7], dual active bridge (DAB) [8,9], phase-shifted full-bridge (PSFB) [10], and LLC resonant converters [11,12], to enhance conversion efficiency, reduce system losses, and improve stability. Advanced control algorithms further optimize performance by modulating variables such as the duty cycle, phase shift angle, and frequency, thereby minimizing the power loss and improving the system response speed, to ensure stable operation of PV systems [13,14].

PSFB series resonant converters (PSFB-SRCs) are especially appealing for MIs, due to their exceptional step-up ratio, efficiency, and power density [15]. Extensive research has delved into various aspects of these converters. For example, a two-mode control strategy adept at managing wide-ranging load variations was introduced [16], while a hybrid-modulated dual-output configuration that significantly broadens the applicability of PSFB-SRCs was proposed [17]. The auxiliary circuit integrated in [18] enabled active soft-switching, leading to a notable performance boost with reduced switching losses and enhanced overall efficiency. Furthermore, the modeling of zero voltage switching (ZVS) transitions developed by [19] contributes to maintaining high efficiency. In terms of analytical modeling, Laplace transforms have been utilized [20] to conduct steady-state analyses, establishing a robust theoretical foundation. The state-of-the-art has advanced with sophisticated small-signal models that account for parasitic elements and peak current mode control, providing more accurate system-level predictions [21,22]. Concerning control strategies, a dual-loop control scheme optimized for LiFePO4 battery charging was designed [23], and a method ensuring fast dynamic response in hybrid SRC-PSFB converters was presented [24], underscoring the adaptability and versatility of these systems.

Despite the breadth of applications covered by existing studies, their modeling and control methods have tended to be complex and scenario-specific, imposing higher demands on digital controllers. Notably, no prior research has addressed the need for a modeling and control approach tailored to MIs that can operate efficiently across wide load ranges, with a simple control logic suitable for commercial deployment. Moreover, PSFB-SRCs exhibit reduced efficiency under light-load conditions and at high input voltages [25]. The commonly employed fundamental harmonic analysis (FHA) is only accurate near the resonant frequency, which, given the broad input voltage and output power ranges in micro-inverters, makes achieving accurate modeling and high-performance control across all operating conditions a significant challenge [26,27].

In this context, to address the existing research gap, this article innovatively develops first- and second-order time-domain equivalent models for PSFB-SRCs across a spectrum of operating conditions, enabling precise derivation of the output gain. Leveraging variable relationships, an advanced control strategy is proposed, utilizing turn-on time as the sole feedback variable and incorporating the phase shift angle and dead time as feedforward variables. This allows for the direct computation of frequency, duty cycle, and phase shift time, ensuring compatibility with digital controllers. This approach supports stable operation over wide load ranges, simplifies the control logic for commercial deployment, and maintains high-efficiency power conversion. Importantly, the control loop remains consistent regardless of varying input voltages and output powers, globally optimizing the MI system's efficiency, stability, and dynamic response, thereby making a significant contribution to PSFB-SRC converters within photovoltaic applications.

In this article, Section 2 provides a comprehensive analysis of the topology and operating modes of PSFB-SRCs, deriving the output gain for major operating conditions based on a second-order time-domain equivalent model. In addition, Section 3 delves into light-load performance through first-order equivalent circuit modeling and optimization, examining the impact of phase shift on current stress and conduction losses. Building on this foundation, Section 4 introduces a three-degree-of-freedom global optimization control strategy that avoids control loop switching, ensuring consistent performance across all operating conditions. To substantiate these theoretical advancements, Section 5 presents experimental results from a prototype, validating the proposed modeling and control strategies. Finally, Section 6 summarizes the key findings and provides a cohesive conclusion to the study.

2. Phase-Shift Full-Bridge Series Resonant Converter

2.1. Converter Topology

Figure 1 illustrates the PSFB-SRC studied in this paper. The PV panel voltage and current are denoted as V_{pv} and I_{pv}, respectively. An input capacitor C_{in} is used to filter out high-frequency ripples. Four MOSFETs (S_1, S_2, S_3, S_4) form a full-bridge circuit, with their parasitic capacitances represented by C_{oss1}, C_{oss2}, C_{oss3}, and C_{oss4}. The drain-to-source voltages of the MOSFETs are denoted as V_{ds1}, V_{ds2}, V_{ds3}, and V_{ds4}.

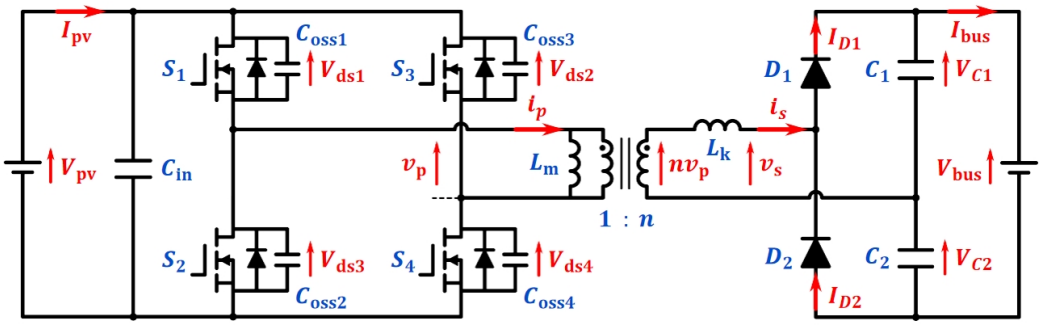

Figure 1. The PSFB-SRC.

The midpoints of the two legs of the full-bridge circuit connect to the primary ends of the high-frequency transformer. The switching states of the MOSFETs, together with V_{pv}, determine the primary-side voltage v_{p} of the transformer. The primary-side current is denoted as i_{p}. The transformer's magnetizing inductance and the equivalent leakage inductance on the secondary side are represented as L_{m} and L_{k}, respectively. Assuming the turns ratio between the primary and secondary sides is $1:n$, the voltage across L_{k} on the secondary side can be approximated as nv_{p}. The voltage difference between the midpoint of capacitors C_1 and C_2 and the midpoint of diodes D_1 and D_2 is denoted as v_{s}.

The voltage doubler constructed from capacitors C_1 and C_2 along with diodes D_1 and D_2 further increases the voltage boost ratio. Additionally, L_{k}, C_1, and C_2 form a series resonant tank that enhances the soft-switching performance and reduces the current stress. The voltage difference $nv_{\mathrm{p}} - v_{\mathrm{s}}$ drives the resonant tank, determining the secondary-side current i_{s}, diode currents I_{D1} and I_{D2}, and capacitor voltages V_{C1} and V_{C2}, thereby controlling the output bus current I_{bus}. In a two-stage grid-tied inverter, the DC bus voltage is typically regulated by the inverter stage, allowing the DC stage's output to be considered a constant voltage source V_{bus}. The reference directions for all voltages and currents used in the subsequent modeling are provided in Figure 1.

2.2. Normal Operation Mode

Figure 2a,b present typical waveforms of the converter operating in SRC mode and PSFB mode, respectively. In SRC mode, the gate signals of S_1 and S_4 are identical, whereas

in PSFB mode, there is a phase shift between the leading bridge leg (constructed with S_1 and S_2) and the lagging bridge leg (constructed with S_3 and S_4).

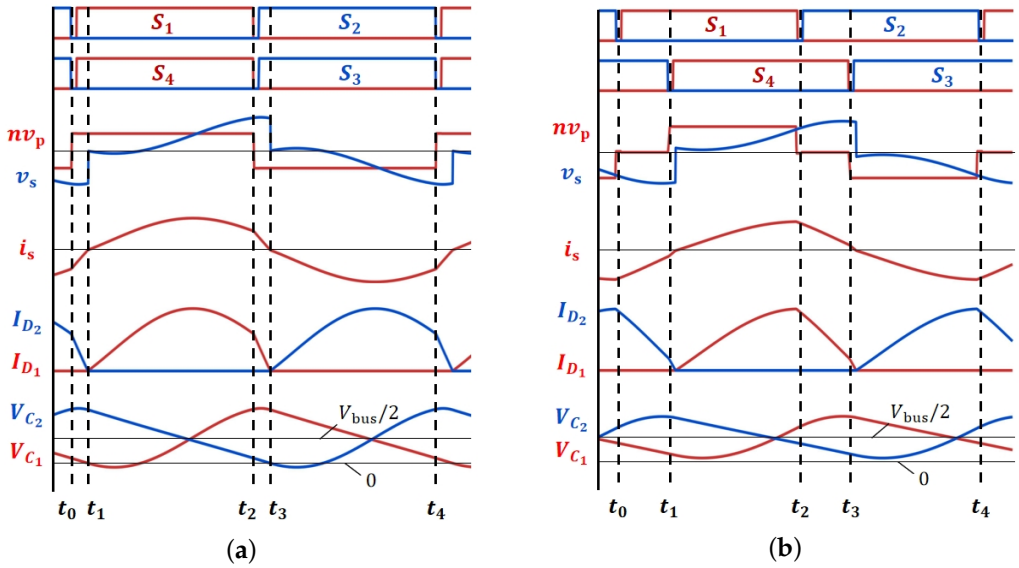

Figure 2. Typical waveforms of the converter in (**a**) SRC mode; (**b**) PSFB mode.

2.2.1. SRC Mode

From t_0 to t_1: The equivalent circuit is shown in Figure 3a, where v_p equals V_{pv}, while v_s is negative. Consequently, the secondary-side current i_s rapidly decreases in reverse. Since D_2 is active, i_s charges capacitor C_2, while discharging capacitor C_1.

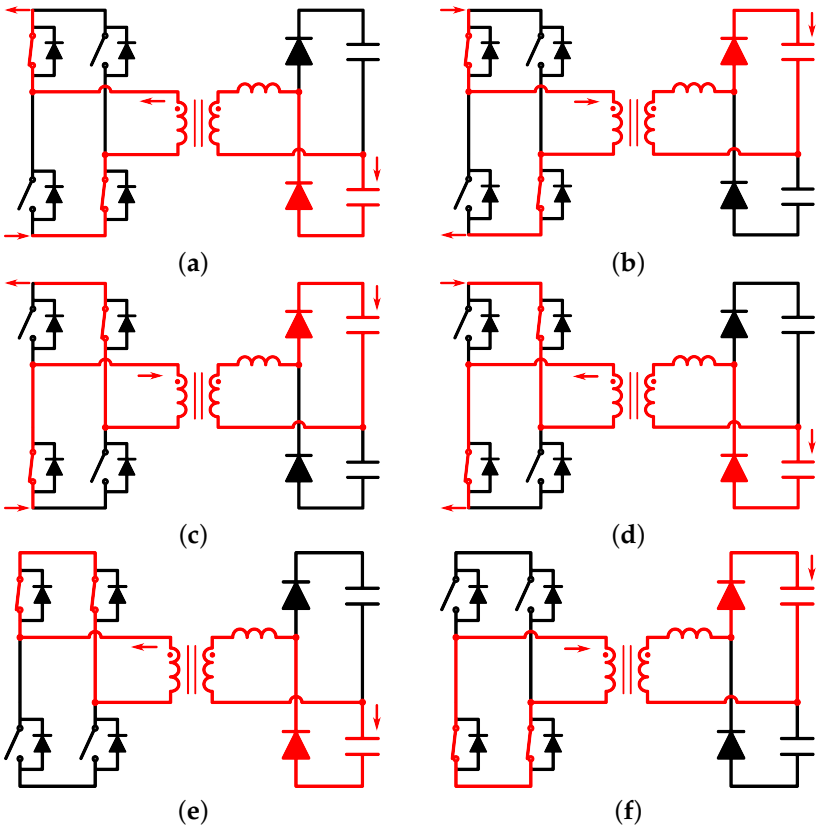

Figure 3. Equivalent circuits: (**a**) SRC Mode $t_0 - t_1$; (**b**) SRC & PSFB Mode $t_1 - t_2$; (**c**) SRC Mode $t_2 - t_3$; (**d**) SRC& PSFB Mode $t_3 - t_4$; (**e**) PSFB Mode $t_0 - t_1$; (**f**) PSFB Mode $t_2 - t_3$.

From t_1 to t_2: The equivalent circuit is shown in Figure 3b, where v_p remains equal to V_{pv}, and i_s begins to increase positively from zero. During this period, D_1 is activated, allowing i_s to charge capacitor C_1, while discharging capacitor C_2. Notably, there is a brief dead time at t_2 to prevent simultaneous conduction of the two MOSFETs in the same bridge leg. During this dead time, before S_2 and S_3 are switched on, i_p discharges the parasitic capacitors C_{oss2} and C_{oss3}. This process facilitates the realization of zero voltage switching (ZVS) for S_2 and S_3, enhancing the efficiency and reliability of the converter.

From t_2 to t_3 and from t_3 to t_4: The equivalent circuits during these intervals are depicted in Figure 3c and Figure 3d, respectively. The waveforms in these periods exhibit symmetry with those observed from t_0 to t_1 and from t_1 to t_2.

2.2.2. PSFB Mode

From t_0 to t_1: The equivalent circuit is shown in Figure 3e, where S_1 and S_3 are switched on, resulting in $v_p = 0$. Free resonance occurs in the equivalent circuit composed of L_k and the parallel capacitance of C_1 and C_2. During this phase, the negative secondary-side current i_s decreases at a moderate rate.

From t_1 to t_2: S_1 and S_4 are switched on simultaneously. The trends in the voltages and currents during this period closely resemble those observed from t_1 to t_2 in the SRC mode. This behavior can be illustrated by the equivalent circuit shown in Figure 3a.

From t_2 to t_3 and from t_3 to t_4: The equivalent circuits during these intervals are depicted in Figure 3f and Figure 3d, respectively.

2.3. Output Gain

The accuracy of FHA diminishes when there is a substantial discrepancy between the switching frequency and the resonant frequency. To address this limitation and provide a more precise description of the converter's dynamics, a time-domain second-order model is utilized. In both SRC mode and PSFB mode, assuming that the magnetic inductance L_m is much larger than the leakage inductance L_k, the primary-side current i_p increases due to the resonance between L_k and the parallel combination of C_1 and C_2 during the interval from t_1 to t_2. Consequently, the secondary-side current i_s can be derived as follows:

$$i_s(t) = \frac{nV_{pv} - V_{c1}(t_1)}{2\pi L_k f_r} \sin[2\pi f_r(t - t_1)], t \in (t_1, t_2) \tag{1}$$

where f_r is the resonant frequency, given by $f_r = 1/(2\pi\sqrt{L_k \cdot C_1//C_2})$. The voltage across capacitor C_1 at t_2, denoted as $V_{c1}(t_2)$, can be calculated based on the average voltage of V_{c1} and V_{c2}, which is equal to $V_{bus}/2$, plus the capacitor voltage deviation Δv_c [25]:

$$V_{c1}(t_2) = \frac{V_{bus} - \Delta v_c}{2} \tag{2}$$

In Figure 2a,b, the time period $t_1 - t_0$ is much shorter than $t_2 - t_1$. This indicates that the majority of power transfer in a half switching cycle occurs during the interval $t_2 - t_1$. Consequently, the instantaneous current from t_1 to t_2 can be used to estimate the average current in the positive half switching cycle [15,25]. Therefore, the average current through diode D_1, denoted as $\overline{I_{D_1}}$, can be described by

$$\overline{I_{D_1}} = \overline{I_{C_1}} + \overline{I_{C_2}} \tag{3}$$

Here, $\overline{I_{C_1}}$ and $\overline{I_{C_2}}$ denote the average currents through capacitors C_1 and C_2, respectively, which are equal to the bus current I_{bus}. Therefore, the following equation holds:

$$\int_{t_1}^{t_2} I_{D_1}(t)\,dt = \int_{t_1}^{t_2} i_s(t)\,dt = \frac{I_{bus}}{f_s} \tag{4}$$

The capacitor voltage deviation Δv_c, as given in Equation (2), can be calculated as follows:

$$\Delta v_c = \frac{\int I_{D_1}(\tau)d\tau}{C_1} = \frac{I_{bus}}{2C_1 f_s} \tag{5}$$

The time period $t_2 - t_1$ can be expressed in terms of the switching frequency f_s and the phase shift angle D_{ps}:

$$t_2 - t_1 = \frac{1 - D_{ps}}{2f_s} \tag{6}$$

By integrating Equations (1), (2), (4), and (6), the expression for the output bus current can be derived as follows:

$$I_{bus} = (2nV_{pv} - V_{bus})(C_1//C_2)f_s \frac{1 - \cos\left[\frac{f_r}{f_s}(1 - D_{ps})\pi\right]}{1 + \cos\left[\frac{f_r}{f_s}(1 - D_{ps})\pi\right]} \tag{7}$$

Figure 4a,b depict the converter's output power as a function of variations in the phase shift angle and switching frequency for input voltages of 30 V and 50 V, respectively, based on Equation (7). At an input voltage of 30 V, the converter successfully transfers power across almost the entire load range through the combined use of frequency and phase shift control. However, when the input voltage rises to 50 V, the preset ranges for switching frequency and phase shift angle become inadequate to support light load operation (below 100 W). This highlights the limitations of the current control strategy under higher input voltage conditions.

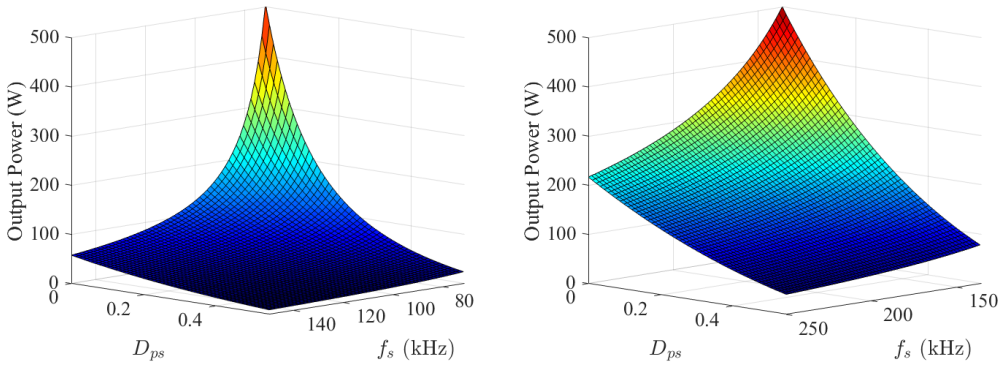

Figure 4. The converter output power versus variations in the phase shift angle and the switching frequency when: (**a**) V_{pv} = 30 V; (**b**) V_{pv} = 50 V.

3. Light Load Performance Optimization

3.1. Typical Waveform and Output Characteristics

For light load conditions, as illustrated in Equation (7) and Figure 4, either a high switching frequency or a large phase shift angle is typically observed. To reduce the power transferred per switching cycle, while maintaining a constant switching frequency and phase shift angle, one potential approach is to extend the ineffective time intervals, often referred to as dead time. This extension is usually realized through duty cycle control, allowing the converter to lower its power output, without altering its fundamental control parameters [28,29].

The typical light load waveforms are illustrated in Figure 5a (with no phase shift) and Figure 5b (with a phase shift applied), respectively. In both cases, the major power transfer occurs from t_0 to t_2 within a half switching cycle.

From t_0 to t_1: The equivalent circuit is identical to that shown in Figure 3b;

From t_1 to t_2 in Figure 5a: The equivalent circuit is depicted in Figure 6a. During this interval, no MOSFETs are actively switched on; instead, the anti-parallel diodes of S_2 and S_3 are activated, resulting in $v_p = -V_{pv}$.

From t_1 to t_2 in Figure 5b: The equivalent circuit is shown in Figure 6b. Here, S_4 and the anti-parallel diode of S_2 are activated, leading to $v_p = 0$.

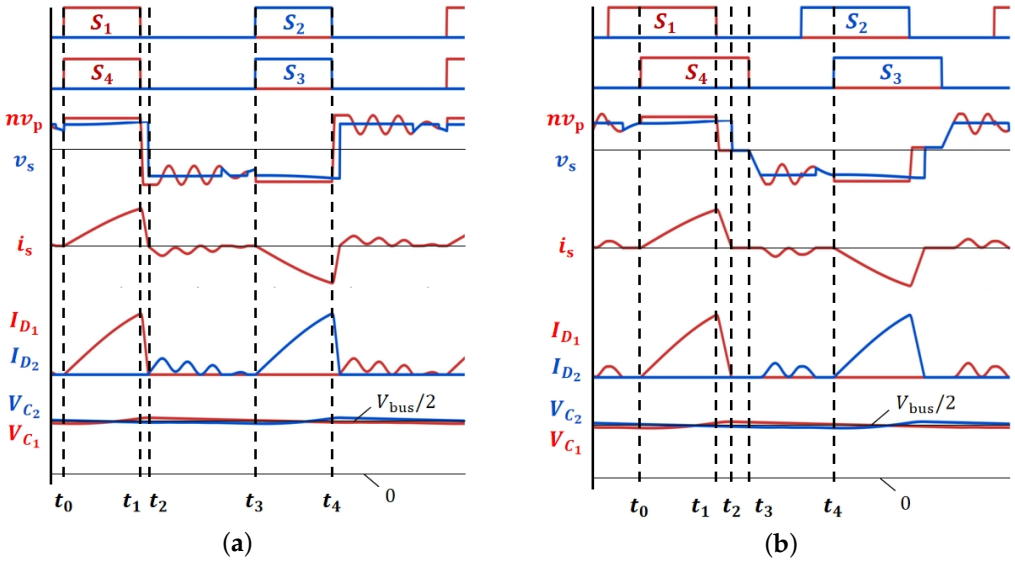

Figure 5. Light load waveforms: (**a**) with no phase shift; (**b**) with phase shift.

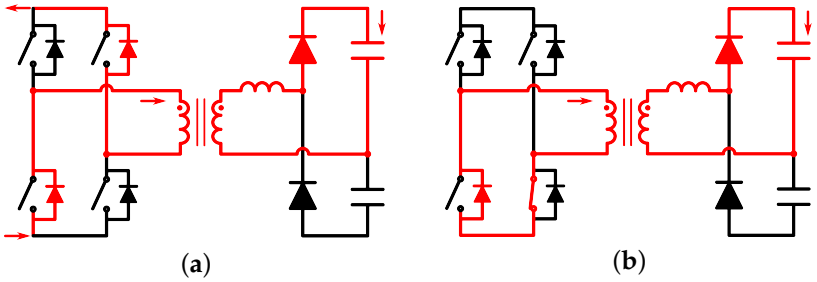

Figure 6. Equivalent circuit at light load corresponding to (**a**) Figure 5a, $t_1 - t_2$; (**b**) Figure 5b, $t_1 - t_2$. Arrows indicate the direction of currents.

During light load conditions, the time interval for power transfer is significantly shorter than the resonant period, leading to negligible fluctuations in the capacitor voltage. Consequently, the capacitor voltage can be approximated as constant, allowing the system to be effectively modeled using a first-order circuit approximation.

3.1.1. Mode with No Phase Shift

For the mode operating without a phase shift, the first-order model is derived based on the waveforms shown in Figure 5a as follows:

$$is(t) = \begin{cases} \dfrac{nV_{pv} - \frac{V_{bus}}{2}}{L_k}(t - t_0), \ t \in [t_0, t_1] \\ i_s(t_1) + \dfrac{-nV_{pv} - \frac{V_{bus}}{2}}{L_k}(t - t_1), \ t \in [t_1, t_2] \end{cases} \tag{8}$$

Define $T_{on1} = t_1 - t_0$ as the on-time interval and $T_{dd1} = t_3 - t_1$ as the dead time interval. Given that $i_s(t_2) = 0$, the values of $i_s(t_1)$ and the duration $t_1 - t_0$ are derived as follows:

$$\begin{cases} i_s(t_1) = I_{pk1} = \dfrac{nV_{pv} - \frac{V_{bus}}{2}}{L_k} T_{on1} \\ t_2 - t_1 = \dfrac{nV_{pv} - \frac{V_{bus}}{2}}{nV_{pv} + \frac{V_{bus}}{2}} T_{on1} \end{cases} \tag{9}$$

where I_{pk1} represents the peak current in this mode. The average current of $i_s(t)$ over a half switching period is equal to the bus current, yielding

$$I_{bus1} = \frac{nV_{pv} \cdot (2nV_{pv} - V_{bus})}{(2nV_{pv} + V_{bus}) \cdot L_k} \cdot \frac{2T_{on1}^2}{T_{on1} + T_{dd1}} \tag{10}$$

3.1.2. Mode with Phase Shift

In the mode with phase shift, as shown in Figure 5b, the first-order model is modified as follows:

$$i_s(t) = \begin{cases} \dfrac{nV_{pv} - \frac{V_{bus}}{2}}{L_k}(t - t_0), \ t \in [t_0, t_1] \\ i_s(t_1) + \dfrac{-\frac{V_{bus}}{2}}{L_k}(t - t_1), \ t \in [t_1, t_2] \end{cases} \tag{11}$$

Define $T_{on2} = t_3 - t_0$ as the on-time interval, $T_{dd2} = t_4 - t_3$ as the dead-time interval, and $T_{ps} = t_3 - t_1 = D_{ps} \cdot T_{on2}$ as the phase shift time interval. The values of $i_s(t_1)(I_{pk2})$ and the duration $t_2 - t_1$ are derived as follows:

$$\begin{cases} i_s(t_1) = I_{pk2} = \dfrac{nV_{pv} - \frac{V_{bus}}{2}}{L_k}(1 - D_{ps}) T_{on2} \\ t_2 - t_1 = \dfrac{nV_{pv} - \frac{V_{bus}}{2}}{nV_{pv} + \frac{V_{bus}}{2}} T_{on2} \end{cases} \tag{12}$$

The phase shift time interval $T_{ps} = t_3 - t_1$ should be sufficiently large to ensure that $t_2 - t_1 \leq T_{ps}$. Therefore, the phase shift angle must satisfy: $D_{ps} \geq 1 - \frac{V_{bus}}{2nV_{pv}}$. As a result, the bus current in the light load mode with phase shift is determined as follows:

$$I_{bus2} = \frac{nV_{pv} \cdot (2nV_{pv} - V_{bus})}{V_{bus} \cdot L_k}(1 - D_{ps})^2 \frac{2T_{on2}^2}{T_{on2} + T_{dd2}} \tag{13}$$

3.2. Impact of the Phase Shift

To accurately assess the impact of the phase shift in the two different light load modes, an analysis is conducted under conditions where both the switching frequency and the output current are kept constant, ensuring a fair comparison. Specifically, (1) the total switching period remains unchanged: $T_{on1} + T_{dd1} = T_{on2} + T_{dd2}$; (2) the output bus current is consistent: $I_{bus1} = I_{bus2}$.

The simplified first-order current model for the two different light load modes is illustrated in Figure 7. Given that the output bus currents are equal, i.e., $I_{bus1} = I_{bus2}$, the on-time interval T_{on2} can be expressed as a function of T_{on1} based on Equations (10) and (13):

$$T_{on2} = \sqrt{\frac{V_{bus}}{2nV_{pv} + V_{bus}}} \cdot \frac{T_{on1}}{1 - D_{ps}} \tag{14}$$

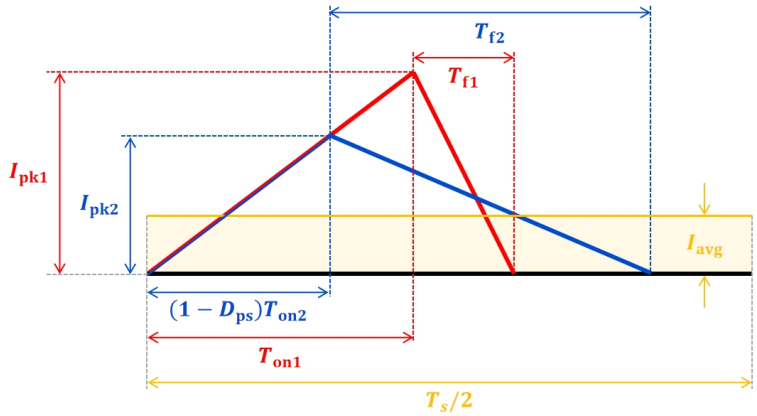

Figure 7. Simplified first-order current model.

Subsequently, I_{pk2} can also be expressed in terms of I_{pk1}. Given the condition $nV_{pv} > \frac{V_{bus}}{2}$, the peak current stress in the mode with phase shift, I_{pk2}, is less than $\sqrt{2}/2$ times the peak current stress in the mode without phase shift, I_{pk1}, as presented in Equation (15):

$$I_{pk2} = \sqrt{\frac{V_{bus}}{2nV_{pv} + V_{bus}}} \cdot I_{pk1} \leq \frac{\sqrt{2}}{2} I_{pk1} \tag{15}$$

According to Figure 7, by expressing the current fall times T_{f1} and T_{f2} in terms of T_{on1} for both operating modes, the following equations hold:

$$\begin{cases} T_{f1} = \dfrac{2nV_{pv} - V_{bus}}{2nV_{pv} + V_{bus}} \cdot T_{on1} \\ T_{f2} = \dfrac{2nV_{pv} - V_{bus}}{\sqrt{V_{bus}(2nV_{pv} + V_{bus})}} \cdot T_{on1} \end{cases} \tag{16}$$

Consequently, the conduction loss in the two different modes, denoted as P_{cond1} and P_{cond2}, can be estimated as follows:

$$\begin{cases} P_{cond1} = f_s \left[\displaystyle\int_0^{T_{on1}} \left(\frac{2nV_{pv} - V_{bus}}{2L_k}\right)^2 t^2 dt + \int_0^{T_{f1}} \left(\frac{2nV_{pv} + V_{bus}}{2L_k}\right)^2 t^2 dt \right] \\ P_{cond2} = f_s \left[\displaystyle\int_0^{(1-D_{ps})T_{on2}} \left(\frac{2nV_{pv} - V_{bus}}{2L_k}\right)^2 t^2 dt + \int_0^{T_{f2}} \left(\frac{V_{bus}}{2L_k}\right)^2 t^2 dt \right] \end{cases} \tag{17}$$

Assuming an identical loop resistance, the ratio of conduction losses between the two different modes, P_{cond2}/P_{cond1}, is expressed as

$$P_{cond2}/P_{cond1} = \frac{1}{2}\sqrt{\frac{V_{bus}}{2nV_{pv} + V_{bus}}} \tag{18}$$

Figure 8 depicts how the conduction loss ratio P_{cond2}/P_{cond1} varies with changes in the PV voltage V_{pv} and bus voltage V_{bus}. In all operating conditions, the conduction losses in the mode with phase shift are notably lower than those in the no phase shift mode. This performance advantage becomes more significant as the PV voltage rises or the bus voltage decreases.

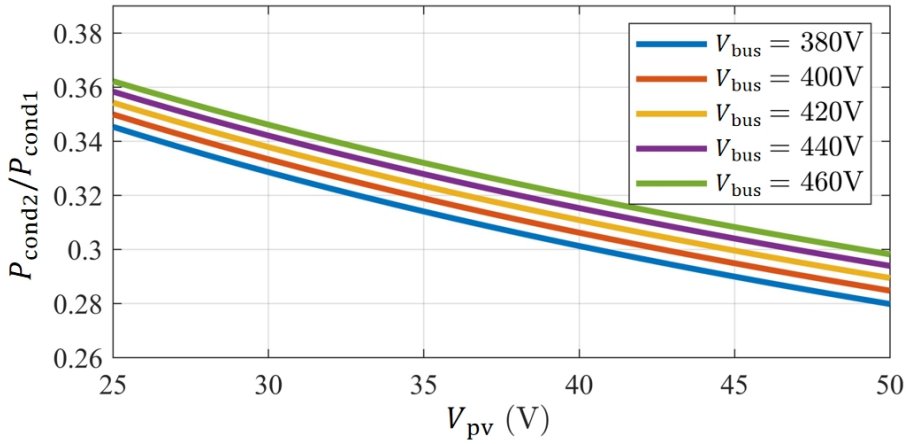

Figure 8. Conduction loss comparison.

In summary, the implementation of phase shift is crucial for reducing both the current stress and conduction losses, rendering it especially beneficial under light load conditions.

4. Full Load Range Control Strategy

According to Equation (7), when V_{pv} is high, the switching frequency increases significantly, and the phase shift angle becomes large under light load conditions. However, the hardware limitations of the MOSFET drive circuit impose an upper limit on the switching frequency. Additionally, a large phase shift angle can lead to hard switching in the MOSFETs of the lagging bridge leg, which reduces efficiency. To enhance the converter efficiency under light load conditions, the converter operates in the light load mode with phase shift as discussed in Section 3. By increasing the dead time, the output power can be reduced, even if both the switching frequency and phase shift angle remain unchanged. Based on Equation (7), a multivariate function $Fcn(I_{pv}, V_{pv}, V_{bus})$ is constructed as follows:

$$Fcn(I_{pv}, V_{pv}, V_{bus}) = \frac{I_{pv}}{2N_{sp}V_{bus} - \frac{V_{bus}^2}{V_{pv}}} \tag{19}$$

The function value is mapped to particular switching frequencies and phase shift angles, establishing a relationship as follows:

$$Fcn(I_{pv}, V_{pv}, V_{bus})\Big|_{D_{ps}=D_{ps0}}^{f_s=f_0} = f_0(C_1//C_2)\frac{1-\cos[\frac{f_r}{f_0}(1-D_{ps0})\pi]}{1+\cos[\frac{f_r}{f_0}(1-D_{ps0})\pi]} \tag{20}$$

The PSFB-SRC manages multiple controlled variables. Considering the real-time variations in operating conditions, switching between different control loops can cause system instability. To mitigate this issue, a single T_{on} feedback control loop is implemented, complemented by T_{dd} and D_{ps} as feedforward variables, as illustrated in Figure 9. T_{on} is calculated using a PI controller that processes the error between the PV current reference I_{ref} and the measured PV current I_{pv}. The feedforward variables are directly determined from the sampled values of PV voltage, PV current, and bus voltage, ensuring both stability and responsiveness in control.

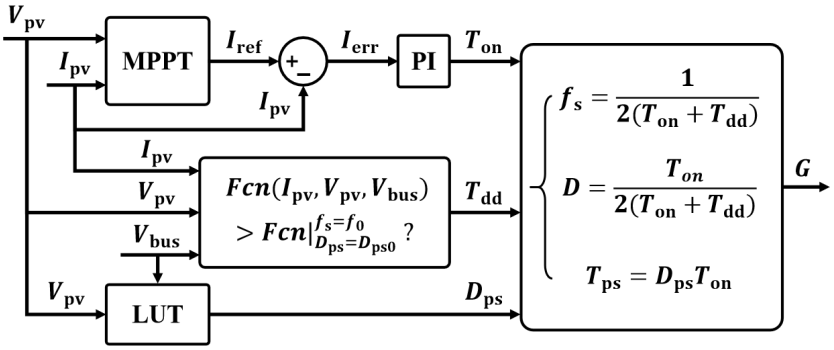

Figure 9. Full load range efficiency optimization control method.

Equations (19) and (20) are used to determine the operation mode, as presented in Figure 9, where a question mark is employed to represent a crucial judgment logic. If the inequality $F(I_{pv}, V_{pv}, V_{bus}) > F|^{f_s=f_0}_{D_{ps}=D_{ps0}}$ holds, the PSFBSRC operates in heavy load mode. In this scenario, T_{dd} is minimized to prevent direct conduction between MOSFETs in the same bridge leg, thus ensuring safe operation. Otherwise, if the inequality does not hold, the PSFBSRC operates in the light load mode, where the output gain is described by Equation (13) and a larger T_{dd} is applied as a feed-forward variable to reduce the switching frequency and switching loss, as the MOSFETs are in hard switching. In both light and heavy load modes, T_{on} is calculated using a simple PI controller, while D_{ps} is obtained from a lookup table based on the PV voltage. Finally, the switching frequency, duty cycle, and phase shift time are determined from T_{on}, T_{dd}, and D_{ps}, and these parameters are applied in digital controllers to optimize the performance.

5. Experimental Results and Analysis

The effectiveness of the proposed modeling and control method is verified by the results of experiments conducted on the hardware platform illustrated in Figure 10. The system parameters used in these experiments are listed in Table 1.

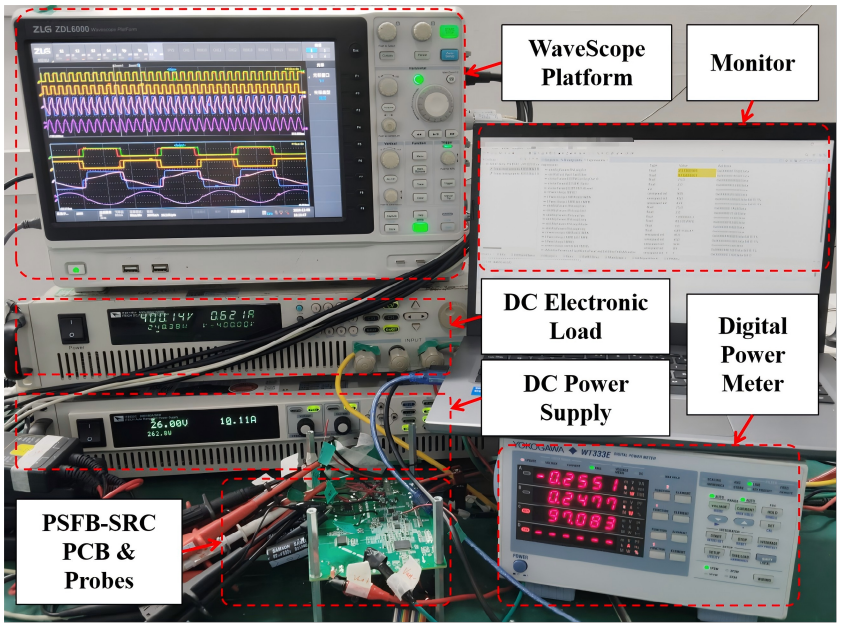

Figure 10. The experiment setup.

Table 1. System parameters.

Parameters	Symbols	Value
Power Rating	P_{ref}	400 W
PV Voltage range	V_{pv}	25–50 V
Output (DC Bus) Voltage	V_{bus}	400 V
Transformer Turn Ratios	N_{sp}	25:3
Leakage Inductance	L_k	210 uH
Resonant Capacitance	C_1, C_2	15 nF
LC Network Resonant Frequency	f_r	63.4 kHz
Switching Frequency Range	f_s	65–250 kHz
Phase shift angle Range	D_{ps}	0–0.8

Figure 11 presents the experimental waveforms of the gate signals (S_1, S_2, S_3, S_4), primary side voltage (v_p), secondary side voltage (v_s), and secondary side current (i_s) under various operating conditions. When V_{pv} = 25 V and I_{pv} = 15 A, the PSFB-SRC operated near its maximum output limitation, with the phase shift angle D_{ps} = 0. The switching frequency was slightly higher or approximately equal to the resonant frequency, as shown in Figure 11a. This condition can also be inferred from the waveform of i_s, which approached a full resonant cycle. Under these specific operating conditions, FHA accurately modeled the system dynamics. Figure 11b illustrates the waveforms when V_{pv} = 35 V, I_{pv} = 2 A, and D_{ps} = 0.3. During the effective power transmission interval, the waveform of i_s was approximately linear, indicating that a time-domain first-order model is suitable for modeling light load conditions. Figure 11c,d present waveforms where V_{pv} and I_{pv} were kept constant, with the only difference being the phase shift angle D_{ps}. Increasing D_{ps} resulted in a reduction of the switching frequency, aligning with the predictions of the time-domain second-order model described by Equation (7).

Zero voltage switching (ZVS) is closely linked to overall power efficiency. The performance under various input voltage and output power conditions is presented in Figure 12, with the specific operating conditions detailed in Table 2. ZVS was achieved in most scenarios, except for certain critical cases: In Figure 12(a3), the MOSFET in the lagging bridge leg experienced hard switching, as highlighted by the red dashed block. This condition arose due to a large phase shift angle. Reducing this angle and correspondingly increasing the switching frequency could significantly improve the efficiency. In Figure 12(c1,c2,c3), both MOSFETs in the bridge legs underwent hard switching, also indicated by the red dashed blocks. These conditions occurred when the PSFB-SRC operated in light load mode. Under the latter conditions, the increased efficiency compared to normal operation mode was primarily attributed to the reduced switching frequency, which minimized the switching losses.

Table 2. ZVS conditions in Figure 12.

I/O	Figure 12	D_{ps}	f_s (kHz)	I/O	Figure 12	D_{ps}	f_s (kHz)	I/O	Figure 12	D_{ps}	f_s (kHz)
30 V, 300 W	(a1)	0	88.9	50 V, 300 W	(b1)	0	158.7	30 V, 60 W	(c1)	0	92.6
	(a2)	0.15	86.6		(b2)	0.15	155.0		(c2)	0.15	87.7
	(a3)	0.25	71.4		(b3)	0.4	134.2		(c3)	0.25	74.6

Figure 13 illustrates the experimental results for the converter efficiency across the entire load range at various PV voltages, employing the proposed control strategy. At an input voltage of 25 V, the PSFB-SRC exhibited its highest efficiency across all load conditions, reaching a peak efficiency of 97.8% at 60% of the rated power. As the input voltage increased, the overall efficiency tended to decrease. Notably, even at an input

voltage of 50 V, the efficiency under extreme light load conditions (10% of the rated power) remained above 90%.

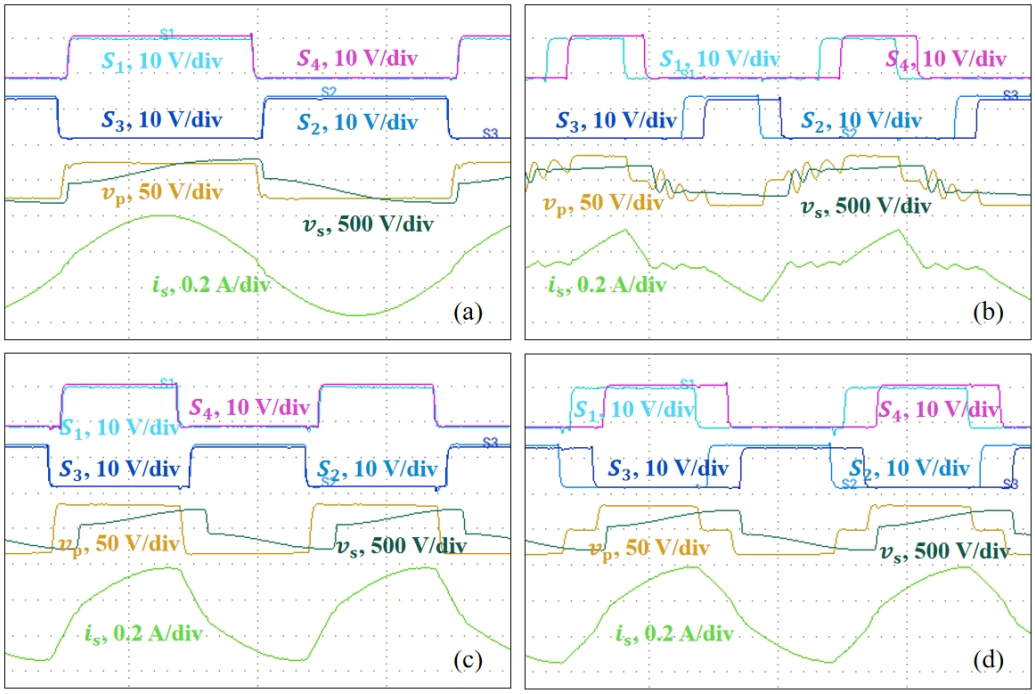

Figure 11. Experimental waveforms under different operating conditions: (**a**) V_{pv} = 25 V, I_{pv} = 15 A, D_{ps} = 0; (**b**) V_{pv} = 35 V, I_{pv} = 2 A, D_{ps} = 0.3; (**c**) V_{pv} = 35 V, I_{pv} = 10 A, D_{ps} = 0; (**d**) V_{pv} = 35 V, I_{pv} = 10 A, D_{ps} = 0.3.

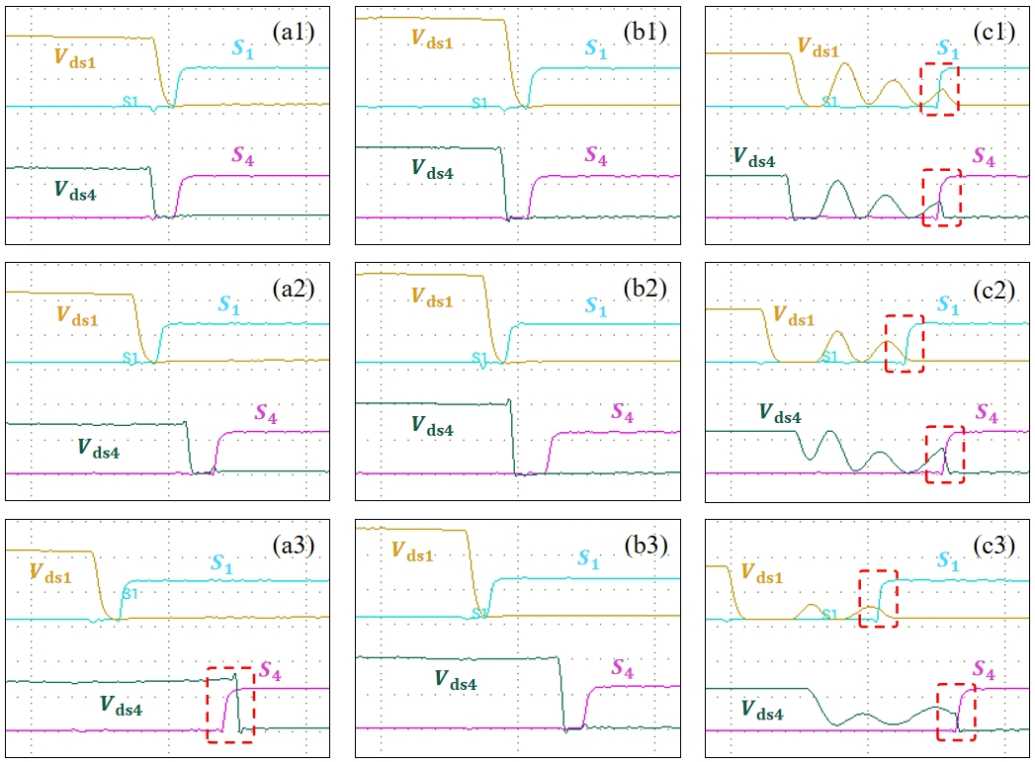

Figure 12. ZVS performances. The specific operating conditions represented by each sub-figures is detailed in Table 2.

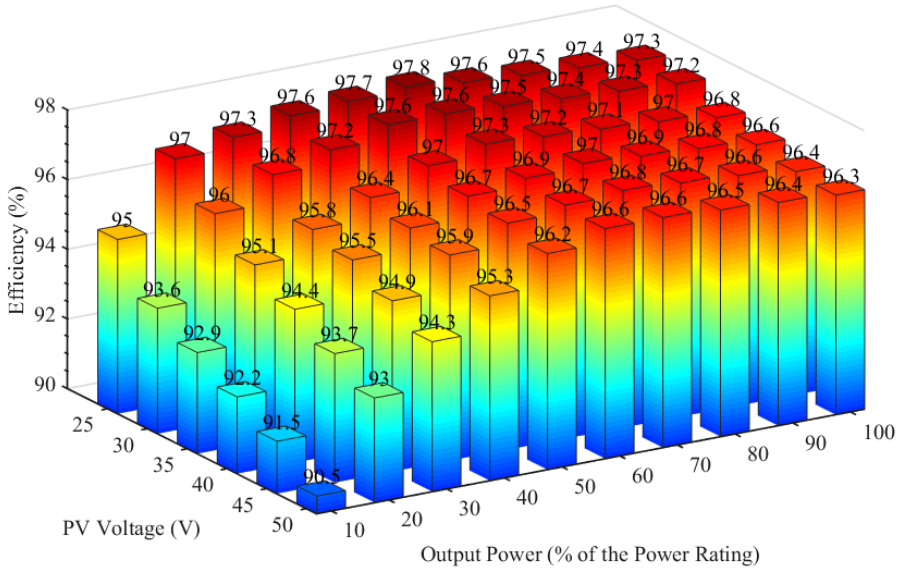

Figure 13. Efficiency across the full output power range at various PV voltages.

Figure 14 shows the experimental efficiency results across the full load range for the proposed method, compared with Baseline1 from [10] and Baseline2 from [15]. At an input voltage of 25 V, the proposed solution exhibited a higher efficiency throughout the entire load range than both baselines. When the input voltage was 50 V, while the proposed approach was slightly less efficient than baseline2 under light loads (below 50% of rated power), it outperformed both baselines in the heavy-load range (50–100% of rated power). Notably, the proposed system's peak efficiency exceeded that of the baselines in [10,15], highlighting its superior performance.

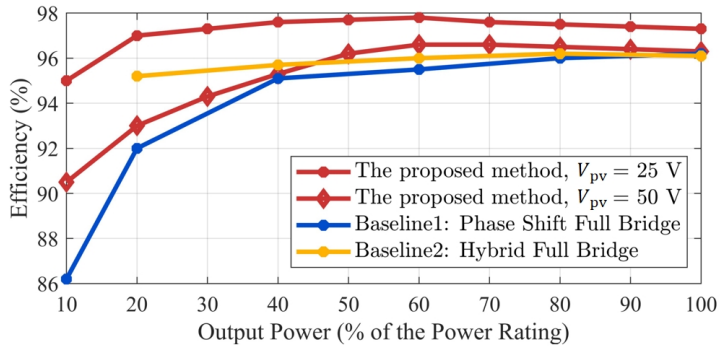

Figure 14. Comparisons of full output power range efficiencies with Baseline1: the phase-shift full bridge studied in [10], and Baseline2: the hybrid full bridge studied in [15].

6. Conclusions

A flowchart of the methodology for addressing challenges in PSFB-SRC for MI applications is presented in Figure 15. In conclusion, this study addressed the modeling and efficiency challenges associated with PSFB-SRCs in MI applications, especially under conditions of a light load and high input voltage. By developing first- and second-order time-domain equivalent models, the limitations of traditional FHA, which is typically constrained to near-resonant frequencies and therefore not suitable for wide-range operation, were overcome. The equivalent models accurately predicted the converter's performance across a broad spectrum of operating conditions, leading to precise determination of the output gain.

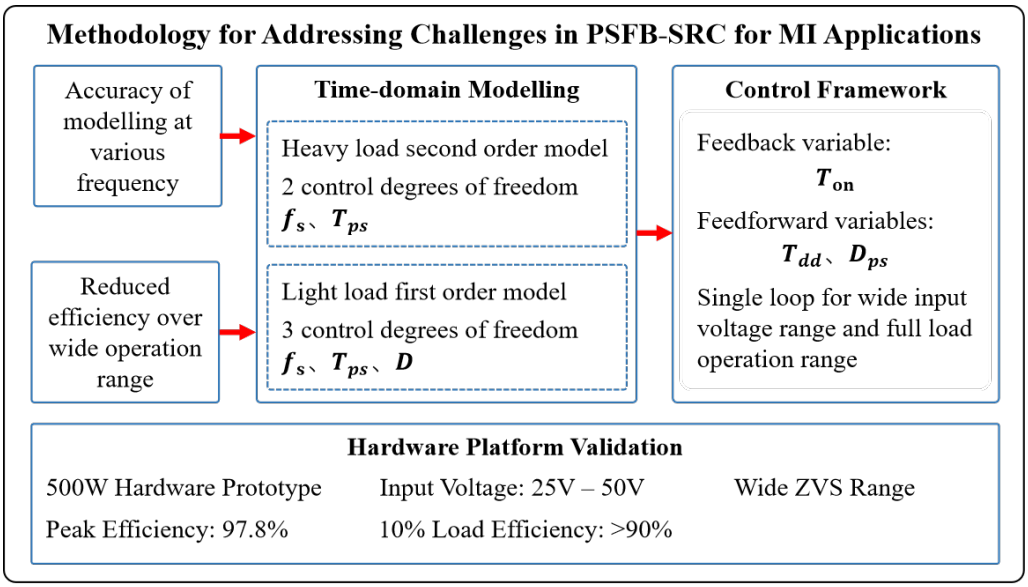

Figure 15. Flowchart of methodology.

Furthermore, an advanced control strategy was introduced that utilizes turn-on time as the feedback variable, complemented by phase shift angle and dead time as feedforward variables. This innovative approach enables direct computation of key operational parameters such as frequency, duty cycle, and phase shift time, thereby enhancing compatibility with digital controllers. The proposed control method simplifies the system architecture, while simultaneously improving efficiency, stability, and dynamic response, all without necessitating complex control loop switching mechanisms.

The experimental validation demonstrated consistent improvements in efficiency and overall system performance across different conditions. The success of the prototype indicates promising prospects for commercial adoption in PV systems.

Future work will integrate adaptive machine learning algorithms, such as reinforcement learning and neural networks, into PSFB-SRC control to predict optimal parameters like the switching frequency and phase shift angle, optimizing performance in real time. Additionally, the models and control strategies could be applied for application in wind power generation and hybrid energy systems, aiming to improve energy conversion efficiency and system stability. These advancements will broaden the scope of this research, contributing to more versatile and sustainable renewable energy solutions.

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Conflicts of Interest: G.Q., H.M. and J.L. has been involved as a consultant and expert witness in Shenzhen Poweroak Newener Co., Ltd. C.H. is affiliated with Shenzhen Poweroak Newener Co., Ltd. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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