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Magnetic Integrated Multi-Trap Filters Using Mutual Inductance to Mitigate Current Harmonics in Grid-Connected Power Electronics Converters

Maged Al-Barashi [1], Aicheng Zou [1,*], Yongjun Wang [1], Wei Luo [1], Nan Shao [1], Zeyu Tang [1] and Bing Lu [2]

[1] School of Aeronautics and Astronautics, Guilin University of Aerospace Technology, Guilin 541004, China; dr_albarashi@yahoo.com (M.A.-B.); dongwang@guat.edu.cn (Y.W.); glluowei@163.com (W.L.); shaonan@guat.edu.cn (N.S.); 2023044@guat.edu.cn (Z.T.)

[2] School of Electrical Engineering, Southwest Jiaotong University, Chengdu 611700, China; lbj_swjtu@163.com

* Correspondence: zouaicheng@guat.edu.cn; Tel.: +86-18977366018

Abstract: This paper introduces magnetic integrated high-order trap–trap–inductor (*TTL*) and inductor–trap–trap (*LTT*) filters featuring two *LC*-traps designed for grid-tied inverters, aimed at reducing the size of output-power multi-trap filters. The proposed filters exhibit excellent harmonic absorption capabilities alongside a compact design. Building on the conventional integrated inductor–capacitor–inductor (*LCL*) filter, the approach involves connecting a small capacitor in parallel with either the inverter-side or grid-side inductors to create an *LC* trap. Additionally, a second *LC* trap can be achieved by integrating the filter capacitor in series with the equivalent trap inductance, established by the magnetic coupling between the grid-side inductor and inverter-side one. This paper thoroughly analyzes the characteristics of the proposed filters. Moreover, a design method is presented to further minimize the size of the output filter components. Finally, validation through simulations and hardware-in-the-loop (HIL) experiments confirms the proposed approach's effectiveness and feasibility. The integrated designs achieve a size reduction of 35.4% in comparison with the discrete windings. Moreover, these designed filters comply with IEEE standards, maintaining a grid-side current total harmonic distortion (THD) of less than 0.9%, with all current harmonics below 0.3% of the fundamental current.

Keywords: harmonic distortion; *LC*-trap passive filters; magnetic integration; multi-trap filters; switching harmonics

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1. Introduction

The increasing demand for energy has driven rapid advancements in power electronics for renewable generation and microgrid systems [1,2]. Grid-tied converters have been widely implemented to facilitate the seamless integration of renewable energy sources and energy storage systems into modern electrical networks [3–6]. However, these converters introduce a significant level of harmonic distortion due to pulse width modulation (PWM). According to the IEEE standard 519-2014 [7], grid current harmonics above the 35th harmonic must be limited to less than 0.3% of the fundamental current to comply with grid codes. To mitigate these harmonics, low-pass power filters are typically employed to connect the converters to the power grid and reduce high-frequency PWM harmonics to acceptable levels [8].

Traditionally, high-frequency PWM harmonics have been attenuated using *L* filters [9]. Nevertheless, achieving the desired harmonic effectiveness with such simple filters necessitates a large inductor, leading to bulky and costly power converters. Consequently,

this larger inductor can restrict grid current dynamics. To address this issue, the inductor–capacitor–inductor (*LCL*) filter has been proposed, which offers a reduction in size while enhancing performance [10–17]. As the price of copper rises, the cost of inductors increases as well. To achieve improved harmonic attenuation and minimize overall inductance, output filters utilizing trap filters have been developed based on the *LCL* filter. These include *LTL* [18–21], *LTCL* [22–25], *SPRLCL* [26], $L(LCL)_2$ [27], and *PDTLCL* [28] filters, where the letter "T" signifies one or more LC traps. Each of these modified filters incorporates at least one *LC* trap designed to bypass or block specific harmonics. Generally, the switching frequency and its multiples are the positions where most switching harmonics are concentrated. When these frequencies align with the resonance frequencies of the *LC* traps, PWM harmonics are dramatically diminished. Additionally, trap inductors can be designed to have small inductances as the resonance frequency of the *LC* traps is generally equal to or greater than the switching frequency, greatly lowering the total inductance. Filters with smaller inductances also greatly reduce the switching harmonics of multilevel inverters [29]. However, high-order output filters are preferred in low-voltage applications.

LTL filters, categorized as high-order trap filters, have garnered considerable attention. The inclusion of parallel *LC* traps enhances harmonics suppression, although it can increase the trap inductances within the filters. In practical implementations, employing double-trap filters is advantageous, as the significant harmonics are typically at the switching and double switching frequencies. Nevertheless, minimizing the output filter remains challenging since they need two extra inductors in comparison with the *LCL* ones, where they account for much of the filter's size. Size is a critical consideration in filter design, as it directly impacts performance and overall effectiveness. Designers often strive to achieve the optimal performance with the minimum size of the filter due to factors like expenses, spatial limitations, power density, and weight.

Much of the previous research has focused on reducing the overall inductance of power filters to decrease both their cost and size. The magnetic cores are a primary factor contributing to the filters' size. Additional magnetic cores are introduced with high-order trap filters, which significantly increase the system size, even with a notable reduction in total inductance. Magnetic integration is a common solution, where several discrete inductors are combined on one magnetic core [30–38]. The use of EIE cores to integrate the *LCL* filter was suggested in [39,40] to improve the efficiency of converters, aiming to minimize the core size. Three-phase *LCL* filters have been presented in [41], utilizing delta-yoke cores, which are approximately 10% smaller than EIE ones. While these approaches were feasible, they often led to magnetic coupling, which affects the harmonic suppression efficiency of the filters. Coupling inductance is introduced in the branch of the filter capacitor by this magnetic coupling. An I core with high permeability was employed in the case of EIE cores [39,40] to mitigate the effects of magnetic coupling.

Conversely, by utilizing inductance produced through magnetic coupling, [42–45] developed *LLCL* filters. However, to achieve the desired trap inductance, a specific air gap is required in the common flux path of the EE core. This requirement restricts the flexibility of the design and complicates parameter adjustments post-fabrication. The filters presented in [42–45] achieved only one *LC* trap, resulting in limited harmonic suppression capabilities. In [46], an integrated double-trap *LTL* filter was introduced. Yet, this design, alongside the side limbs' air gaps, necessitated additional inductance between the *LC* traps, making the overall design more intricate.

To address these challenges, this paper introduces new output filters named trap–trap–inductor (*TTL*) and inductor–trap–trap (*LTT*) filters. In these proposed filters, the magnetic coupling of the grid-side inductor and inverter-side inductor creates an equivalent trap inductance. This inductance is connected serially with the filter capacitance to

form one *LC* trap. A small capacitor is connected in parallel to either the inverter-side or grid-side inductors to form another *LC* trap. The distinction between the two filters lies in the placement of the small trap capacitor: in *TTL*, it is positioned on the inverter side, while in *LTT*, it is on the grid side. However, both filters can be designed similarly and utilized for the same applications. Each filter is composed of two traps: one exhibiting zero impedance at the resonance frequency and the other presenting high impedance at that frequency, along with either the grid-side or inverter-side inductance. These traps effectively reduce harmonics around the switching frequency and its first multiple, where they are predominant in the current harmonics. Consequently, the required inductors of filters are minimized by addressing lower harmonics at high multiples of switching frequencies.

To validate the feasibility of the presented filters and demonstrate the efficiency of the integrated components, they are compared with conventional filters, particularly their equivalent *SPRLCL* filter. Moreover, the presented approach will be contrasted with the selective harmonics elimination (SHE) approach [47,48], which employs the controller to suppress exact harmonics without requiring resonance traps. Nevertheless, it is confined to offline calculations and requires large lookup tables in lower fundamental frequencies, often leading to the amplification of high harmonics in an attempt to suppress low harmonics [29,49–51]. The presented approach is more straightforward, providing a similar performance for low-order harmonics, while reducing switching losses and enhancing output waveforms. Furthermore, the coupling effect between the *LCL* filter capacitance and inductance generates a trap without additional components, and employing a single core to the two inductors leads to a more compact design and reduced expenses.

This paper's contributions are summarized as follows:

1. Integrated multi-trap filters are developed and verified.
2. A comprehensive investigation into magnetic integration for various inductors is provided.
3. The harmonic reduction and size minimization validate the proposed methodology.
4. The proposed filters are applicable in a range of electrical power systems, including industrial systems, renewable energies, transportation, etc.

Section 2 covers the fundamental theoretical and operational specifications of the presented *TTL* and *LTT* filters. Section 3 introduces the magnetic integration approach for double-trap *TTL* and *LTT* filters, followed by an optimal design method aimed at reducing filter inductances. Section 4 presents the simulation results and findings from hardware-in-the-loop (HIL) experiments utilizing the proposed approach. Finally, the paper concludes in Section 5.

2. System Structure and Modeling of *TTL* and *LTT* Filters

Figure 1 illustrates an H-bridge single-phase inverter connected to the grid, incorporating both *TTL* and *LTT* filters. The currents i_g and i_i represent the grid-side and inverter-side currents, respectively. The voltages v_{gg}, v_{in}, and V_{dc} correspond to the grid voltage, inverter input voltage, and DC-link voltage. With switches S_1, S_2, S_3, and S_4 operating at the switching frequency f_{sw}, the inverter input voltage v_{in} is rectified into V_{dc}, containing harmonics centered around twice the switching frequency $2f_{sw}$ and its multiples, due to the unipolar effect [52]. The harmonics primarily cluster around $2f_{sw}$ when employing unipolar sinusoidal PWM (SPWM). Therefore, $2f_{sw}$ effectively becomes the primary switching frequency. The harmonics around both $2f_{sw}$ and $4f_{sw}$ are considerably pronounced compared to the harmonics around higher frequencies, where they predominantly contribute to the harmonics of the output current. Thus, the focus on reducing the harmonics at $2f_{sw}$ and $4f_{sw}$ is crucial for effectively minimizing total harmonic distortion. In practical applications,

the use of double *LC* traps is preferred because of the reduced cost and weight, which the current study further explores.

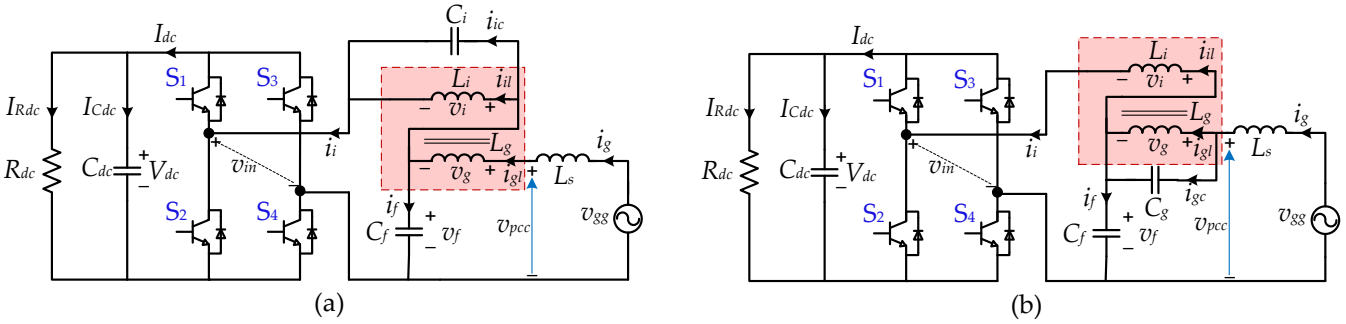


Figure 1. H-bridge single-phase grid-connected converter with a (**a**) *TTL* filter; (**b**) *LTT* filter.

Additionally, the DC-link capacitor and load are represented as C_{dc} and R_{dc}, respectively, with I_{Rdc} and I_{Cdc} indicating their currents. The inductors on the grid and inverter sides, denoted as L_g and L_i, are connected in series, with voltages v_g and v_i across them and currents i_{gl} and i_{il} flowing through. The currents passing the capacitors C_i and C_g are represented as i_{ic} and i_{gc}. Meanwhile, the DC bus current, grid-side current, and inverter-side current are denoted by I_{dc}, i_g, and i_i, respectively. Furthermore, L_s represents the grid inductance. The filter capacitor C_f is placed at the junction of L_g and L_i, with a voltage labeled v_f and the current flowing through it represented as i_f. Additionally, v_{pcc} indicates the voltage at the point of common coupling.

Figure 2 shows the circuit configuration of *TTL* and *LTT* filters, each comprising either the grid-side inductance L_g or the inverter-side inductance L_i, along with two *LC* traps (a trap involving $M_{ig}C_f$ and a trap involving L_iC_i or L_gC_i). Both traps are tuned at $2f_{sw}$ and $4f_{sw}$, with M_{ig} representing the mutual inductance between L_i and L_g. As depicted, the mutual inductance M_{ig} can be utilized in both *TTL* and *LTT* filters to form a resonance tank with C_f. Conversely, either L_i or L_g contributes to the creation of another resonance tank with C_i or C_g to dampen switching harmonics. The feasibility of magnetic integration has been explored in prior studies [30–36,53]. This work highlights the advantages of integrated *TTL* and *LTT* filters, detailing the potential for magnetic integration in multi-trap filter designs. As illustrated in Figure 2, the configuration allows for the elimination of a series resonance inductor previously suggested in [26], thereby reducing the size of the passive filter. The resonance tanks are effective in eliminating exact harmonics from the output current, while the overall filter attenuates the remaining harmonics. An approach for designing *TTL* and *LTT* filters by adjusting the series resonance frequency at $2f_{sw}$ and the parallel resonance frequency at $4f_{sw}$ is proposed in this paper.

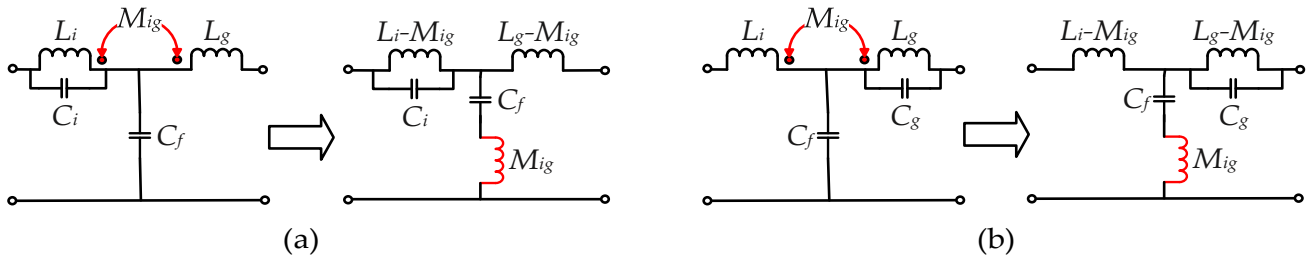


Figure 2. Circuit configuration of a (**a**) *TTL* filter; (**b**) *LTT* filter.

The *LC*-trap configurations in the proposed filters are designed to resonate at specific harmonic frequencies, particularly at the dominant switching frequencies ($2f_{sw}$ and $4f_{sw}$). Each *LC* trap consists of an inductor and capacitor arranged to create a resonance

circuit that provides either high impedance (parallel *LC* trap) or low impedance (series *LC* trap) at the targeted frequencies. At the resonance frequency, the series *LC* trap acts as a short circuit, effectively bypassing harmonic currents, while the parallel *LC* trap creates a high-impedance path, blocking harmonic currents from propagating further. These traps significantly reduce the magnitude of the dominant harmonic components in the current spectrum, as shown in the experimental and simulation results. By incorporating multiple *LC* traps tuned to different harmonic frequencies, the proposed filters achieve enhanced harmonic suppression across a wider frequency range, ensuring compliance with IEEE 519-2014 standards.

Additionally, the block diagrams for the presented output filters are displayed in Figure 3. The transfer function $G_{TTL}(s)$ for the *TTL* filter, which describes the relationship from v_{in} to i_g, can be expressed in Equation (1).

$$G_{TTL}(s) = \frac{i_g(s)}{v_{in}(s)} = \frac{a_4 s^4 + a_2 s^2 + 1}{b_5 s^5 + b_3 s^3 + b_1 s} \tag{1}$$

where

$$a_4 = C_f C_i M_{ig}(L_i - M_{ig})$$
$$a_2 = C_f M_{ig} + C_i(L_i - M_{ig})$$
$$b_5 = C_f C_i M_{ig}(L_i - M_{ig})(L_g - M_{ig} + L_s)$$
$$b_3 = (C_f + C_i)(L_i - M_{ig})(L_g - M_{ig} + L_s) + C_f M_{ig}(L_i + L_g - 2M_{ig} + L_s)$$
$$b_1 = L_i + L_g - 2M_{ig} + L_s$$

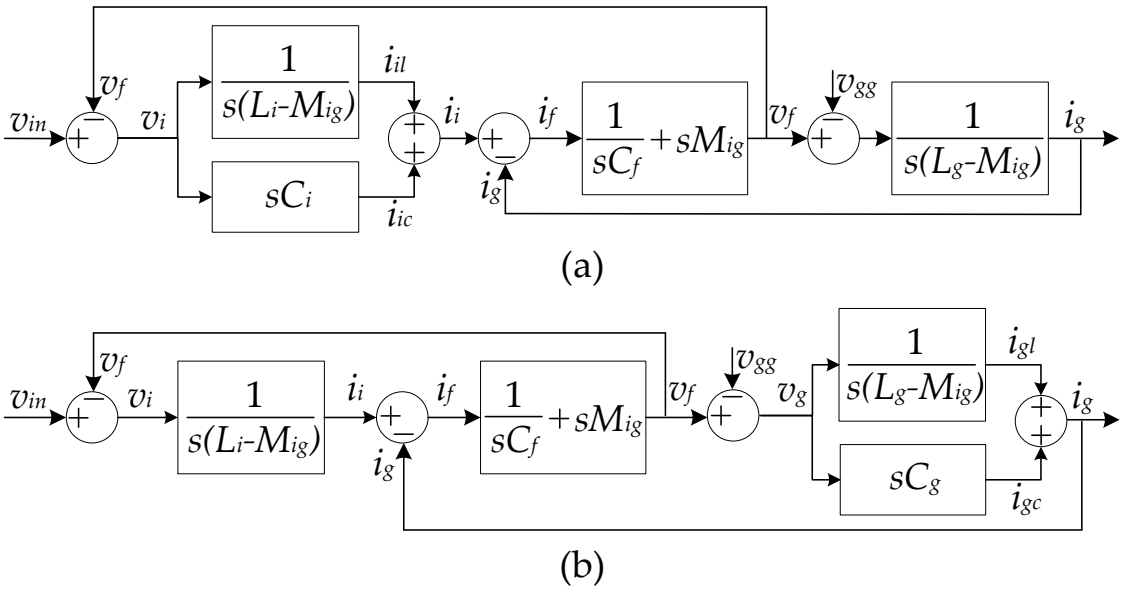


Figure 3. Block diagrams of a (**a**) *TTL* filter; (**b**) *LTT* filter.

Similarly, the transfer function $G_{LTT}(s)$ for the *LTT* filter, relating v_{in} to i_g, is given by Equation (2) [26].

$$G_{LTT}(s) = \frac{i_g(s)}{v_{in}(s)} = \frac{a_4 s^4 + a_2 s^2 + 1}{b_5 s^5 + b_3 s^3 + b_1 s} \tag{2}$$

where

$$a_4 = C_f C_g M_{ig}(L_g - M_{ig})$$
$$a_2 = C_f M_{ig} + C_g(L_g - M_{ig})$$

$$b_5 = C_f C_g (L_g - M_{ig})(L_i M_{ig} - M_{ig}^2 + L_i L_s)$$

$$b_3 = C_f M_{ig}(L_i + L_g - 2M_{ig} + L_s) + C_g(L_g - M_{ig})(L_i - M_{ig} + L_s) + C_f(L_i - M_{ig})(L_g - M_{ig} + L_s)$$

$$b_1 = L_i + L_g - 2M_{ig} + L_s$$

The Bode plots for $i_g(s)/v_i(s)$ of the *TTL*, *LTT*, and *SPRLCL* filters are presented in Figure 4, utilizing the parameters outlined in Table 1, with detailed parameter development steps provided in Section 3. The *TTL* and *LTT* filters preserve the characteristics of the *SPRLCL* filter while achieving significant harmonic suppression at both $2f_{sw}$ and $4f_{sw}$.

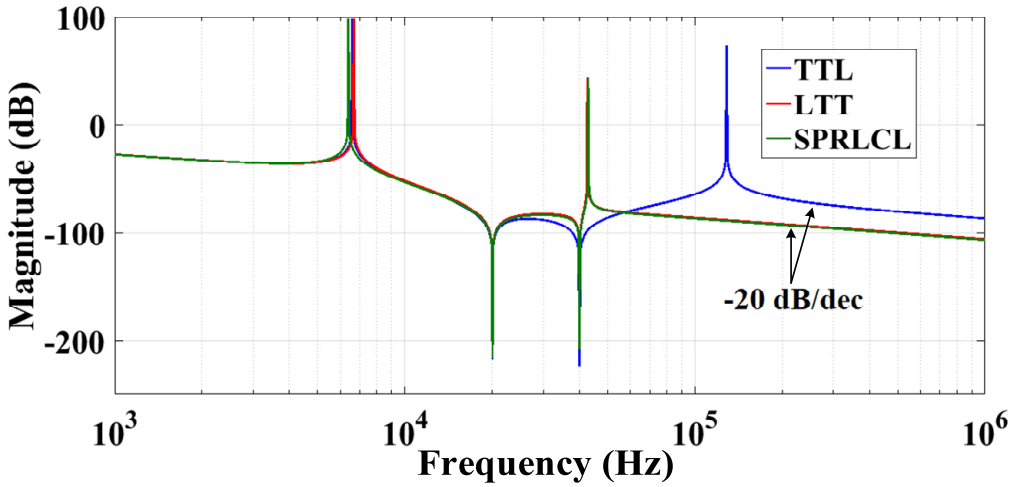


Figure 4. Bode diagrams of *TTL*, *LTT*, and *SPRLCL* filters.

Table 1. Filters' parameter values.

Filter Type	*TTL*	*LTT*	*SPRLCL*
L_i (mH)	0.45	0.45	0.45
C_f (μF)	1.4	1.4	1.4
L_g (mH)	0.45	0.45	0.45
L_s (mH)	3	3	3
C_g (nF)	-	39.09	35.18
C_i (nF)	39.09	-	-
L_f (μH)	-	-	45
M_{ig} (μH)	45	45	-
k_{Mig}	0.1	0.1	-

From Equations (1) and (2), it is evident that $G_{TTL}(s)$ and $G_{LTT}(s)$ each possess two zeros at $\omega_{t1\_TTL} = \omega_{t1\_LTT} = \omega_{t1} = (1/(M_{ig}C_f))^{1/2}$ while $\omega_{t2\_TTL} = (1/(L_iC_i))^{1/2}$ or $\omega_{t2\_LTT} = (1/(L_gC_g))^{1/2}$. Here, ω_{t1}, ω_{t2_TTL}, and ω_{t2_LTT} denote the trap angular frequencies. Figure 4 illustrates that these two frequencies correspond to two magnitude traps. By aligning these frequencies with the dominant switching frequency, the switching harmonics can be efficiently suppressed [26,46], as outlined in Equations (3) and (4), where f_{t1}, f_{t2_TTL}, and f_{t2_LTT} are the respective trap frequencies. Furthermore, the efficiency of the proposed *TTL* and *LTT* filters in minimizing harmonics is demonstrated by the simulations and HIL experiments.

$$f_{t1} = 2f_{sw} = \frac{1}{2\pi}\sqrt{\frac{1}{C_f M_{ig}}} \tag{3}$$

$$\begin{cases} f_{t2_{TTL}} = 4f_{sw} = \frac{1}{2\pi}\sqrt{\frac{1}{C_i(L_i - M_{ig})}} \\ f_{t2_{LTT}} = 4f_{sw} = \frac{1}{2\pi}\sqrt{\frac{1}{C_g(L_g - M_{ig})}} \end{cases} \tag{4}$$

Furthermore, Figure 4 indicates that the magnitude–frequency characteristics of $G_{TTL}(s)$ and $G_{LTT}(s)$ exhibit two resonance peaks, attributable to the denominator's order, which is five. The resonance peaks can be derived by setting the denominators of $G_{TTL}(s)$ and $G_{LTT}(s)$ to zero and replacing s with $j\omega$. The initial resonance frequencies of *TTL* and *LTT* filters are nearly identical, which can be approximated as shown in Equation (5) [42,43], where f_{res1} and ω_{res1} denote the resonance and resonance angular frequencies.

$$\omega_{res1} = 2\pi f_{res1} \approx \sqrt{\frac{L_i + (L_g + L_s) - 2M_{ig}}{C_f(L_g + L_s)L_i - C_f M_{ig}^2}} \tag{5}$$

Figure 4 illustrates that both the *LTT* and *SPRLCL* filters offer superior harmonic suppression for the inverter-side current, marked by a lower second resonance peak and a steeper roll-off in the high-frequency domain. It is critical to position the resonance frequency away from the multiples of the switching frequency to prevent harmonic amplification [22,30], ideally around 43 kHz, as shown in Figure 4. Additionally, the second resonance peak of the *TTL* filter is observed at a higher frequency. Beyond the second resonance frequency, both the *TTL* and *LTT* filters achieve harmonic suppression at a rate of -20 dB/dec.

These resonance peaks could pose stability challenges for the system. Various damping strategies, including passive damping [54–56] and active damping [57–61], have been suggested to enhance system stability. Passive damping effects may be significantly more pronounced in real implementations due to the typical increase in equivalent series resistance (ESR) of passive components at high frequencies. Employing a single-current loop controller with inherent delay can also stabilize the system by appropriately configuring the filter resonance frequency [62–64]. The design of a resonance frequency above the Nyquist frequency [43,65] is advantageous due to extra losses associated with passive damping techniques and the high costs of active damping techniques. Additionally, parasitic resistances in the filter may provide effective damping to improve system stability and performance. Extensive stability analyses have been conducted in earlier works [43,65]; thus, this paper focuses on the magnetic integration aspects of *TTL* and *LTT* filters without replicating that analysis.

3. Magnetic Integration Approach and Design of *TTL* and *LTT* Filters

This section provides a comprehensive method for designing the magnetic integration technique and selecting the parameters for the *TTL* and *LTT* filters. To highlight the advantages of the proposed integrated filters, a size comparison with the discrete *SPRLCL* filter will also be conducted.

3.1. Magnetic Integration Approach

The concept of designing passive filter inductors has been widely examined in the relevant literature. Typically, in the *LCL* filter, both the inverter side and grid side require a separate inductor, meaning two inductors need to be manufactured. For *SPRLCL* [26], *TTL*, and *LTT* filters—where two *LC* traps are used, as depicted in Figure 2—an additional inductor and capacitor are required, adding to the inverter-side and grid-side inductances. As a result, these filters remain relatively large and costly due to the need for extra capacitors and magnetic cores for trap inductors, despite their reduced total inductance compared to standard *LCL* filters. Magnetic integration, a proven technique for *LCL* [39,40] and *LLCL* [42,43] filters, is suggested here to enhanced power density and cost savings.

Using the magnetic integration from *LLCL* filters as a foundation, Figure 5a shows the integrated magnetic design for *TTL* and *LTT* filters. One air gap is inserted into the central

limb and two gaps in the side limbs of the magnetic circuit, which consists of EE magnetic cores, to prevent magnetic saturation. For the same purpose, the side limbs' cross-sectional area is half that of the central limb. Such E cores are often produced for industrial use. The core size, material, turn number for each inductor (N_g and N_i), and air gap lengths (l_{gs} for the side limbs and l_{gc} for the central limb) are essential parameters in building these filter inductors. Air gaps help prevent saturation but decrease magnetic permeability, requiring more turns to achieve the desired inductors. Figure 5b shows the magnetic circuit, which simplifies calculations by ignoring reluctances in the yokes and limbs since air-gap reluctances are significantly higher. Thus, the three limbs' magnetic resistances (R_i, R_m, and R_g) are mainly defined by air-gap reluctances. The flux density should be evaluated to design the magnetic core of integrated filter inductors. The circuit's electrical connections are shown in Figure 2, where inductors L_i and L_g wound on the side limbs are negatively coupled due to opposing flux directions. This negative coupling helps to minimize the filter size, with magnetic coupling between L_g and L_i creating "active trap inductance".

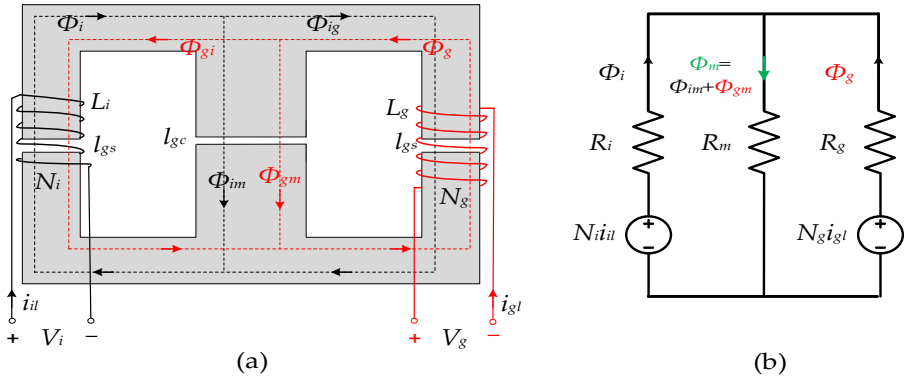


Figure 5. Proposed magnetic integration of *TTL* and *LTT* filters: (**a**) integrated inductor core structure of L_i and L_g; (**b**) simplified magnetic circuit.

Conversely, the second trap can be created by pairing the capacitor (C_i) with the L_i for the *TTL* filter or C_g with the L_g windings for the *LTT* filter. Coupling inductance of one *LC* trap is formed via the integration of L_g and L_i. As depicted in Figure 5b, L_i winding generates the flux Φ_i, while Φ_{ig} and Φ_{im} are fluxes from L_i that flow through the L_g winding and central limb, as shown in Equation (6), with magnetic resistances R_i, R_m, and R_g of the three limbs given by [30,31,43,46].

Similarly, the flux Φ_g is generated by the L_g winding, while Φ_{gi} and Φ_{gm} represent the fluxes from L_g that flow through the L_i winding and central limb, as described in Equation (7) [30,31,43,46].

Each inductor winding's total flux is the sum of self-flux and mutual flux. Therefore, V_i and V_g are defined in Equation (8) [43,46] and further expressed using Equations (6)–(8) in Equation (9) [31,43]. Here, the mutual inductances M_{ig} and M_{gi} and self-inductances L_i and L_g are depicted in Equation (10) [30,31,42,43].

$$\begin{cases} \Phi_i = \dfrac{N_i i_{il}}{R_i + R_m \| R_g} = \dfrac{N_i i_{il}\left(R_m + R_g\right)}{R_i R_m + R_i R_g + R_m R_g}, \\ \Phi_{im} = \dfrac{N_i i_{il}\left(R_m + R_g\right)}{R_i R_m + R_i R_g + R_m R_g} \dfrac{R_g}{R_m + R_g} = \dfrac{N_i i_{il} R_g}{R_i R_m + R_i R_g + R_m R_g}, \\ \Phi_{ig} = \dfrac{N_i i_{il}\left(R_m + R_g\right)}{R_i R_m + R_i R_g + R_m R_g} \dfrac{R_m}{R_m + R_g} = \dfrac{N_i i_{il} R_m}{R_i R_m + R_i R_g + R_m R_g}. \end{cases} \quad (6)$$

$$\begin{cases} \Phi_g = \frac{N_g i_{gl}(R_m+R_i)}{R_iR_m+R_iR_g+R_mR_g}, \\ \Phi_{gm} = \frac{N_g i_{gl} R_i}{R_iR_m+R_iR_g+R_mR_g}, \\ \Phi_{gi} = \frac{N_g i_{gl} R_m}{R_iR_m+R_iR_g+R_mR_g}. \end{cases} \tag{7}$$

$$\begin{cases} V_i = N_i \frac{d}{dt}(\Phi_i - \Phi_{gi}), \\ V_g = N_g \frac{d}{dt}(\Phi_g - \Phi_{ig}). \end{cases} \tag{8}$$

$$\begin{pmatrix} V_i \\ V_g \end{pmatrix} = \begin{pmatrix} L_i & -M_{ig} \\ -M_{ig} & L_g \end{pmatrix} \begin{pmatrix} \frac{di_{il}}{dt} \\ \frac{di_{gl}}{dt} \end{pmatrix}, \tag{9}$$

$$\begin{cases} M_{ig} = M_{gi} = \frac{N_i N_g R_m}{R_iR_m+R_iR_g+R_mR_g}, \\ L_i = \frac{N_i^2(R_m+R_g)}{R_iR_m+R_iR_g+R_mR_g}, \\ L_g = \frac{N_g^2(R_m+R_i)}{R_iR_m+R_iR_g+R_mR_g}. \end{cases} \tag{10}$$

Since M_{ig} and M_{gi} are identical, both can be written as M_{ig}. The coupling between the two inductors follows Equations (9) and (10). Additionally, Equation (11) represents V_i and V_g [42,43] based on Equation (9).

$$\begin{cases} V_i = V_{in} - V_f = L_i \frac{di_{il}}{dt} - M_{ig} \frac{di_{gl}}{dt}, \\ V_g = V_f - V_{pcc} = L_g \frac{di_{gl}}{dt} - M_{ig} \frac{di_{il}}{dt}. \end{cases} \tag{11}$$

Using Equation (10), the magnetic resistances define self and mutual inductances, as shown in Equation (12). In this equation, A_C and A_S are the central and side limb cross-sectional areas, where $A_C = 2A_S$, and the permeability of air is $\mu_0 = 4\pi \times 10^{-7}$ N/A^2 [30,31,42,43,46].

$$\begin{cases} R_i = R_g = \frac{l_{gs}}{A_S \mu_0}, \\ R_m = \frac{l_{gc}}{A_C \mu_0}. \end{cases} \tag{12}$$

Finally, substituting Equation (12) into Equation (10) allows for the calculation of self and mutual inductances, shown in Equation (13) [30,31,43].

$$\begin{cases} L_i = \frac{N_i^2 \mu_0 (l_{gc} A_S + l_{gs} A_C)}{2 l_{gs} (l_{gc} + l_{gs})}, \\ L_g = \frac{N_g^2 \mu_0 (l_{gc} A_S + l_{gs} A_C)}{2 l_{gs} (l_{gc} + l_{gs})}, \\ M_{ig} = \frac{N_i N_g \mu_0 l_{gc} A_S}{2 l_{gs} (l_{gc} + l_{gs})}. \end{cases} \tag{13}$$

Equation (14) illustrates the coupling coefficient k_{Mig}, which measures the mutual inductance between two circuits, calculated as in [30,31,43]. Adjusting l_{gc} and l_{gs}, or their ratio l_{gc}/l_{gs}, allows for fine-tuning of the coupling coefficient.

$$k_{Mig} = \frac{M_{ig}}{\sqrt{L_i L_g}} = \frac{1}{1 + 2 l_{gs}/l_{gc}}. \tag{14}$$

Utilizing the magnetic coupling, as shown in Figure 2, the proposed approach can form an equivalent trap inductor, eliminating the need for multiple magnetic cores and reducing the size and cost of *TTL* and *LTT* filters. Unlike the *SPRLCL* filter, this configuration does not require additional components.

Prior research, such as [42,43], designed *LLCL* filters with magnetic coupling but required a specific air gap in the shared flux path of an EE-type core, limiting design flexibility and complicating adjustments after manufacturing. Since only one *LC* trap was achieved, these designs offered limited harmonic suppression. The integrated *LTL* filter with two traps, presented in [46], necessitated additional inductance between the traps and featured a complex design with side limbs' air gaps. The proposed approach, however, only requires a small additional capacitor, creating a second *LC* trap for enhanced harmonic suppression.

3.2. Design of the Proposed Magnetic Integrated Filters

In this study, the AC grid is considered weak, with a grid inductance of L_s = 3 mH. To design parameters for magnetic integrated *TTL* and *LTT* filters, the system parameters outlined in Table 2 are applied, with an inverter-side current ripple ΔI_{Li} of less than 40% and harmonic suppression compliant with IEEE 519-2014 [7]. Based on the DC-link resistor R_{dc}, the converter functions as a rectifier. The design of L_i, based on methods for *LCL* and *LLCL* filters [43,65], is calculated in Equation (15) for a single-phase unipolar SPWM H-bridge rectifier with $\Delta I_{Li} \leq 40\%$, ensuring protection against IGBT saturation.

$$L_i = \frac{0.5 \times 0.5 \times V_{dc}}{2 f_s \Delta I_{Li}} \approx 0.45 \text{ mH}. \tag{15}$$

Table 2. System parameters.

Description	Symbol	Value
Rated power	P_o	1 kW
Network voltage (RMS)	V_{gg}	110 V
Dc-link voltage	V_{dc}	200 V
Dc-link capacitor	C_{dc}	1000 µF
Dc-link resistor	R_{dc}	40 Ω
Fundamental frequency	f_o	50 Hz
Switching frequency	f_{sw}	10 kHz

Given that this setup achieves the lowest resonance frequency for optimal inductance usage, the design for L_g mirrors that for L_i [33,43]. The total inductance $L_{total} = L_i + L_g$ needs controlling to keep the AC voltage drop across inductors below 10% of the RMS grid voltage v_{gg} [26]. The maximum value for L_{total} is shown in Equation (16), where I_{ref} is the RMS of the reference current $I_{ref} = P_o / v_{gg}$ = 9.09 A for output power P_o. Calculated at 0.9 mH, L_{total} is within acceptable limits for $L_i + L_g$.

$$L_i + L_g \leq \frac{0.1 \times V_{gg}}{2\pi f_o I_{ref}} = 3.85 \text{ mH}. \tag{16}$$

In addition, C_f and M_{ig} are selected according to Equations (3) and (5), where the resonance frequency f_{res1} of the magnetic integrated *TTL* and *LTT* filters is set between half the switching frequency $1/2f_{sw}$ and five-sixths of it $5/6f_{sw}$, while f_{t1} equals $2f_{sw}$ (i.e., f_{t1} = 20 kHz). To further enhance system stability and counteract inductance reduction with a rising current, a midpoint resonance frequency of $f_{res1} = 2/3f_{sw}$ = 6.67 kHz is used [43,65]. With this approach, C_f and M_{ig} are calculated to be 1.4 µF and 45 µH, respectively.

Additionally, based on Equation (14), the coupling coefficient k_{Mig} is optimized to be 0.1 (or 1/10). This results in a calculated l_{gs}/l_{gc} ratio of 4.5, indicating that the values of L_i and L_g primarily depend on l_{gs}.

The additional capacitor (C_i for the *TTL* filter or C_g for the *LTT* filter) is derived using Equation (4) and found to be approximately 39.09 nF. However, the total capacitance C_{total} needs limiting based on the rated reactive power consumption to satisfy power factor requirements [46], which can be expressed as shown in Equation (17). This sets C_{total} at 1.439 µF, comfortably below the maximum limit specified in Equation (17).

$$C_{total} = C_f + C_i = C_f + C_g \leq \frac{0.05 \times P_o}{2\pi f_o V_{gg}^2} = 13.15\ \mu\text{F}. \tag{17}$$

Power loss in the integrated inductors can be reduced by employing Litz wire with a cross-sectional area of 0.5π mm^2 (S_ω) and low ESR. The design criteria for magnetic integration are based on the inductances calculated earlier. The selection process begins with choosing an EE-type magnetic core, taking into account the core size, material, relative permeability μ_r, resistivity, saturation flux density B_{sat}, and cost. High values of B_{sat} or μ_r reduce the inductor's required turns, leading to a smaller, lighter design. Meanwhile, higher resistivity helps to decrease eddy current losses. A balanced selection of these factors ensures cost-effectiveness in producing an efficient inductor. The proposed multi-trap filters utilize ferrite cores due to their availability, cost-effectiveness, and adequate performance in medium-power applications. However, recent advancements in soft magnetic materials, such as Fe-based nanocrystalline materials, present an opportunity for further performance improvements. These materials, as discussed in [66,67], exhibit high permeability, low losses, and excellent frequency responses, making them ideal for high-frequency and high-power applications. Incorporating Fe-based nanocrystalline cores in the multi-trap filter design could significantly enhance its EMI filtering capabilities and harmonic suppression. The high permeability of these materials allows for smaller core sizes while maintaining inductance values, contributing to a more compact filter design. Additionally, their low coercivity minimizes core losses, thereby improving overall efficiency. Future work could explore the integration of nanocrystalline materials into the proposed filter topology, potentially achieving even better harmonic suppression and power density.

The well-known area-product method [68] is used to determine the dimensions of the magnetic core. Given that $L_{\text{i}} = L_{\text{g}}$, the area-product ($A_P$) for the window area A_W and core's cross-sectional area A_S for L_{i} or L_{g} is used to select appropriate cores of integrated inductors. The EE core type is chosen based on this method [68], with $L_{\text{i}} = 0.45$ mH, maximum current $I_{il\text{max}} = 20$ A, and core saturation flux density $B_{\text{max}} = 0.35$ T, where B_{max} is set as λB_{sat} with $0 < \lambda < 1$, and B_{sat} is 0.49 T at 25 °C. The margin λ is set at 0.714 to ensure a 30% safety margin. The A_P is calculated as 8.08×10^{-8} m^4, as shown in Equation (18), where $k_u = 0.5$ is the utilization factor.

$$A_P = \frac{L_i I_{il-\text{max}} S_\omega}{k_u B_{\text{max}}}. \tag{18}$$

According to the TDK product catalog [69], one pair of E 70/33/32 cores is selected, with $A_W = 0.55 \times 10^{-3}$ m^2 and $A_S = 0.35 \times 10^{-3}$ m^2, yielding an area-product of approximately 19.2×10^{-8} m^4 $\approx 2A_P$, providing an ample size margin. The inverter-side inductor winding turns N_i are carefully calculated to prevent saturation of the central limb, as illustrated in Figure 5a. The number of winding turns is determined by Equation (19), with the optimal power loss achieved at 70 turns after accounting for certain parameters, as a high turn count and layers increase skin and proximity losses [70–72].

$$N_i = N_g = \frac{L_i I_{il-\text{max}}}{A_S B_{\text{max}}}. \tag{19}$$

In the proposed design, the flux through the right-side limb, wound by the grid-side windings, remains lower than the maximum flux $\Phi_{\text{max}} = B_{\text{max}} A_s$, where B_{max} is set at

0.742 times B_{sat}, ensuring no saturation. Assuming that magnetic resistance primarily arises from the side-limb air gaps, inserting $l_{gs} = 4.5l_{gc}$ and $A_C = A_S$ into Equation (13) results in Equation (20), where $l_{gc} = 0.97$ mm and $l_{gs} = 4.35$ mm are calculated. For experimental purposes, the air-gap length in the central limb can be adjusted by placing a small I-core within it, allowing for minor modifications to the mutual inductance.

$$l_{gc} = \frac{N_i^2 \mu_0 A_S}{4.95 L_i}. \tag{20}$$

Assuming that L_i and L_g are equivalent to those in the proposed filters, the *SPRLCL* filter is designed in similar steps. Here, C_f is set to meet Equation (5) with $M_{ig} = 0$, placing the f_{res1} of *SPRLCL* between $1/2f_{sw}$ and $5/6f_{sw}$. The midpoint $2/3f_{sw} = 6.67$ kHz is selected to maintain consistency with the proposed filters. As a result, C_f is calculated at 1.43 µF, the same value chosen for C_f in the proposed filters, to enable a fair comparison. The additional inductance L_f is derived by substituting L_f with M_{ig} in Equation (3), and it can be selected as 45 µH. Thus, L_{total} is calculated as 0.945 mH, below the upper threshold of $L_i + L_g + L_f$ as determined in Equation (16). The additional capacitor C_g, calculated by Equation (4) with $M_{ig} = 0$, is 35.18 nF, resulting in a total capacitance C_{total} of 1.435 µF, safely below the limit for $C_f + C_g$ in Equation (17).

After completing the design steps, the parameters for the integrated *TTL*, *LTT*, and *SPRLCL* filters are as outlined in Table 1. Additionally, Figure 6 illustrates the overall design flowchart for the proposed filters as a general guide, where any unmet condition prompts a return to the initial step. The inductance value from Equation (15) and other parameter values serve as examples to validate the proposed design. Verification results confirm that all conditions are met, so revisiting the initial steps is unnecessary. The parameter values are finalized after fine-tuning. The same controller used for [31,43] is suitable for a grid-tied converter with these presented filters, though it is not covered in this paper. Verification results will be presented in Section 4 to demonstrate the design's effectiveness.

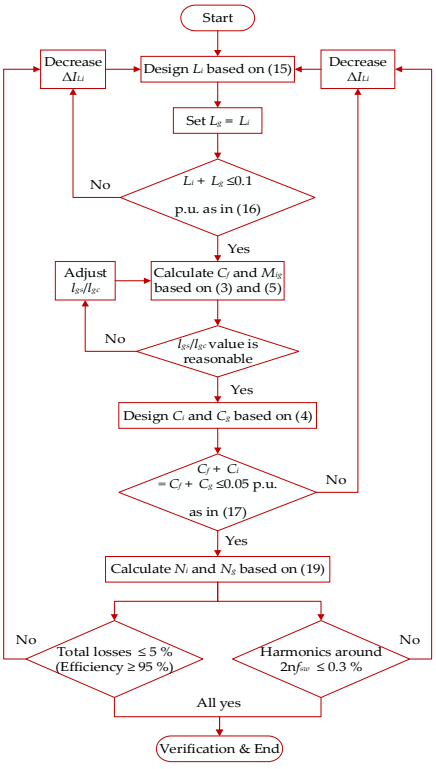


Figure 6. Flowchart of the presented *TTL* and *LTT* filters' design method.

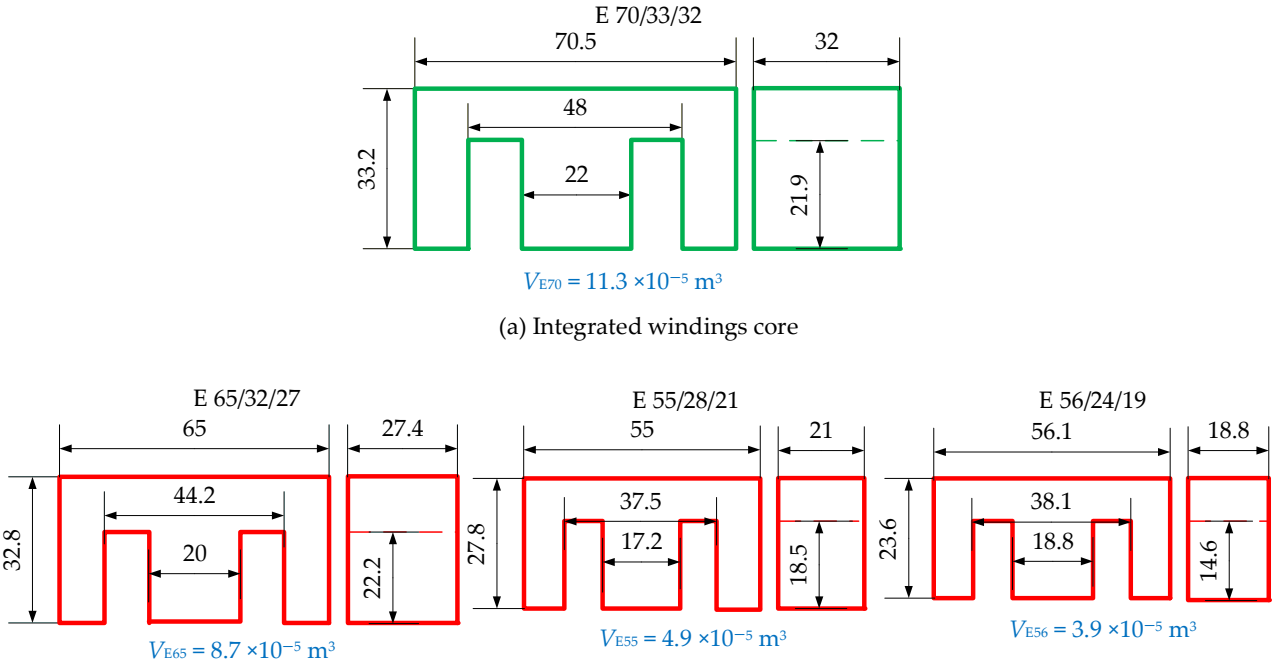
3.3. Comparison of Integrated and Discrete Inductor Sizes

As previously discussed, the integrated multi-trap filters eliminate the need for an extra inductor and components, saving both core space and cost. Since both L_g and L_i are wound onto a single core's side limbs, this integration replaces the three cores needed for filters such as *SPRLCL* or similar designs, like *LCL-LC* and *LTCL* ones.

Comparing the size of integrated and discrete inductors is crucial. The *SPRLCL* filter's discrete inductors can be wound onto the central limbs of three EE core pairs, where the central limbs have a cross-sectional area twice that of the side limbs, making saturation less likely. This configuration allows for the use of smaller cores for discrete inductors. However, the total core size must be compared between discrete and integrated setups to ensure a fair assessment.

Without magnetic integration, the area-product requirements for discrete L_{i} and L_f are calculated as 8.08×10^{-8} m^4 and 6.06×10^{-8} m^4, respectively. Suitable EE cores (EE 65/32/27 and EE 56/24/19) from the TDK catalog [69] offer area-products of 29.4×10^{-8} m^4 and 9.55×10^{-8} m^4. By removing ripple currents, the grid-side inductor's area-product requirement is reduced by 40% to 4.85×10^{-8} m^4. Hence, a single E 55/28/21 core with an area-product of 13.6×10^{-8} m^4 meets these requirements.

Using the area-product method [68], the integrated winding core size is $V_{\mathrm{E70}} = 11.3 \times 10^{-5}$ m^3, while the discrete setup requires $V_{\mathrm{E65}} + V_{\mathrm{E55}} + V_{\mathrm{E56}} = (8.7 + 4.9 + 3.9) \times 10^{-5} = 17.5 \times 10^{-5}$ m^3. As shown in Figure 7, integrated windings enable a 35.4% size reduction compared to discrete designs.



(a) Integrated windings core

(b) Discrete windings cores

Figure 7. Dimensions of (**a**) integrated *TTL* and *LTT* windings' core; (**b**) discrete *SPRLCL* windings' cores.

4. Simulation and HIL Experimental Results

To assess the effectiveness of the presented output filters and their design approach, simulations were conducted by MATLAB/Simulink R2023b, alongside the HIL experimental platform, for a 1 kW grid-connected inverter. The efficacy of *TTL* and *LTT* filters was evaluated in comparison with the discrete *SPRLCL* filter. Tables 1 and 2 outline the primary system parameters adopted to construct the verifying models according to the configuration shown in Figure 1. A thorough analysis was performed, examining various passive

filters' strengths, weaknesses, durability, complexity, and size. The harmonic suppression capabilities and transient behavior of the three filters were evaluated through simulation and HIL testing. The performance metrics obtained are presented in Table 3.

Table 3. Filter performance indexes.

Index	*TTL*	*LTT*	*SPRLCL*
Harmonics at $2f_{sw}$ (% I_{ref})	0.25	0.15	0.00
Harmonics at $4f_{sw}$ (% I_{ref})	0.02	0.00	0.00
Harmonics at $6f_{sw}$ (% I_{ref})	0.01	0.00	0.01
THD of i_g (%)	0.90	0.85	0.83
Core size ($\times 10^{-5}$ m^3)	11.3	11.3	17.5

4.1. Simulation Results

To provide a clearer understanding of the simulation setup and its execution, Figure 8 shows the Simulink model used for the *TTL* and *LTT* filters' simulation. The model comprises key components such as the grid, inverter, control system, and filter design. This representation highlights the interconnections and the functionality of the integrated *TTL* and *LTT* filters, offering an improved understanding of the results. Each subsystem within the Simulink model is appropriately configured to simulate steady-state and transient responses under varying operating conditions.

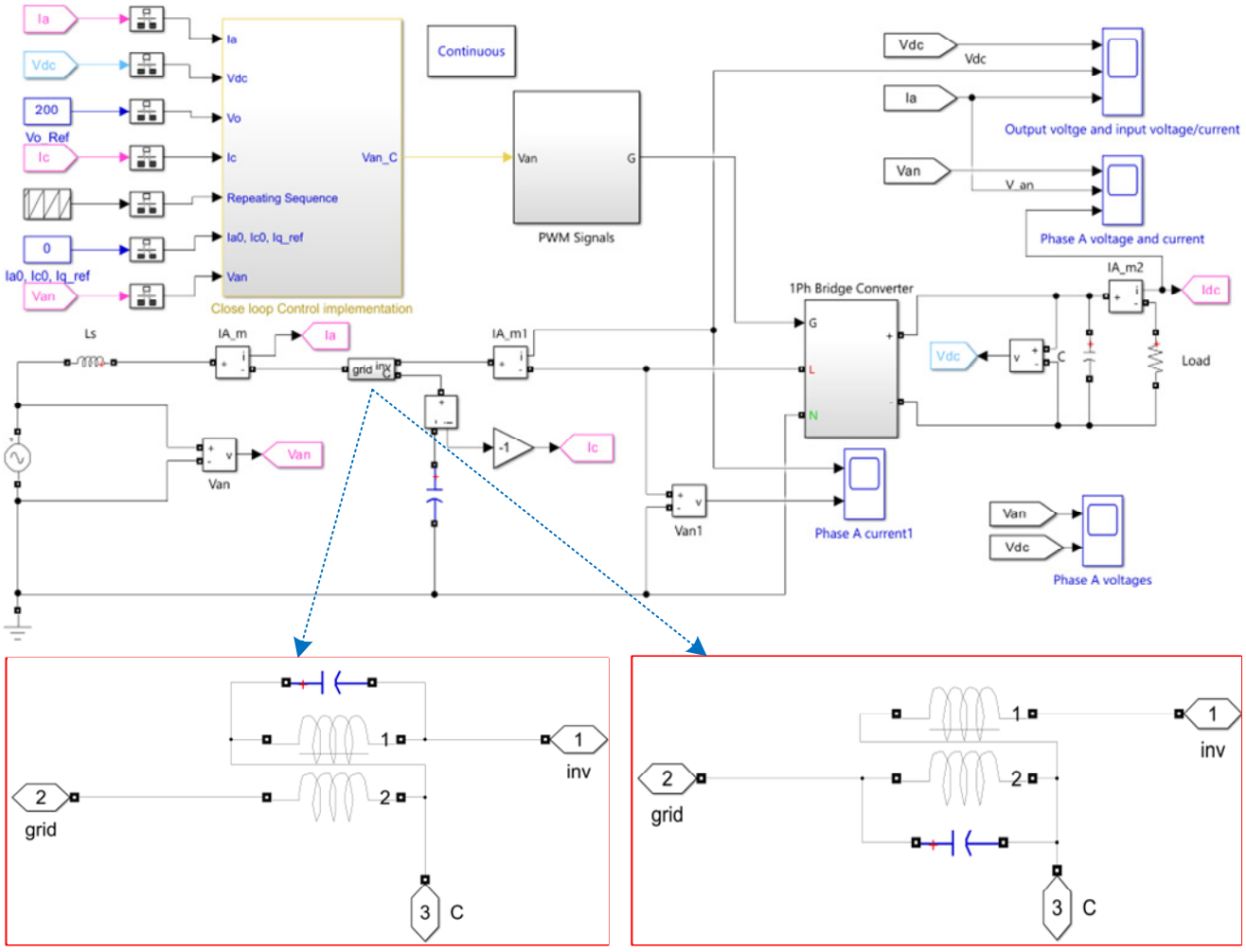


Figure 8. Simulink model of the proposed *TTL* and *TTL* filter system.

Figure 9a illustrates the waveforms for inverter-side current i_i, grid-side current i_g, network voltage v_{gg}, and DC bus voltage V_{dc} for the integrated *TTL* filter in the steady state. As shown, V_{dc} stabilizes close to 200 V, with a small error of 8 V (4%) due to the control system's voltage loop. The current spectrum of i_g is displayed in Figure 9b, showing that low-order harmonics meet IEEE standard 519-2014 [7] requirements, with switching frequency harmonics kept well below the 0.3% threshold, and a total harmonic distortion (THD) of i_g at 0.90%. Thanks to the placement of two *LC* traps, the double and quadruple switching-frequency harmonics are reduced to 0.25% and 0.02%, respectively. Additionally, harmonics in i_g at frequencies above the quadruple switching frequency are effectively suppressed, with sixfold harmonics kept to 0.01% of the fundamental current, safely within the allowable limits. Table 3 provides a detailed breakdown of the current harmonics, all of which comply with IEEE 519-2014.

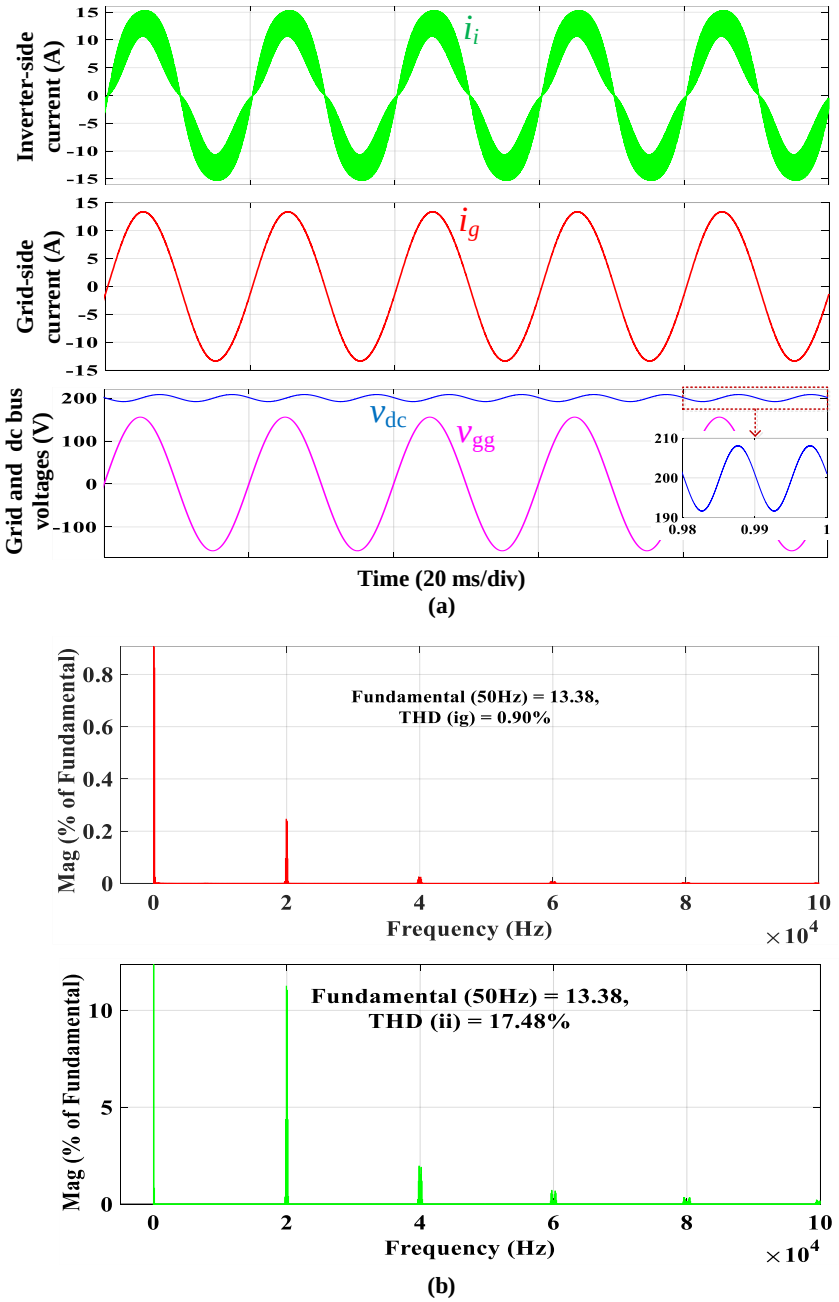


Figure 9. Simulation results of the proposed *TTL* filter: (**a**) waveforms of currents and voltages; (**b**) grid-side and inverter-side currents' spectra.

In Figure 10a, the same waveforms for the *LTT* filter in the steady state are shown. Similar to the *TTL* filter, V_{dc} stabilizes near 200 V, with an error of only 8 V (4%). Moreover, the grid current i_g appears well-filtered and sinusoidal in the steady state. As shown in Figure 10b, the THD of i_g is a low 0.85%, primarily due to the *LTT* filter's strong attenuation of low-order harmonics, which achieves harmonic reductions of 0.15% and 0.00% at the double and quadruple switching frequencies, respectively. High-frequency harmonics are also well suppressed, with sixfold harmonics maintained at 0.00% of the fundamental current. This setup ensures all harmonic currents remain below the 0.3% threshold, meeting IEEE 519-2014 standards. Table 3 further outlines the detailed harmonic components.

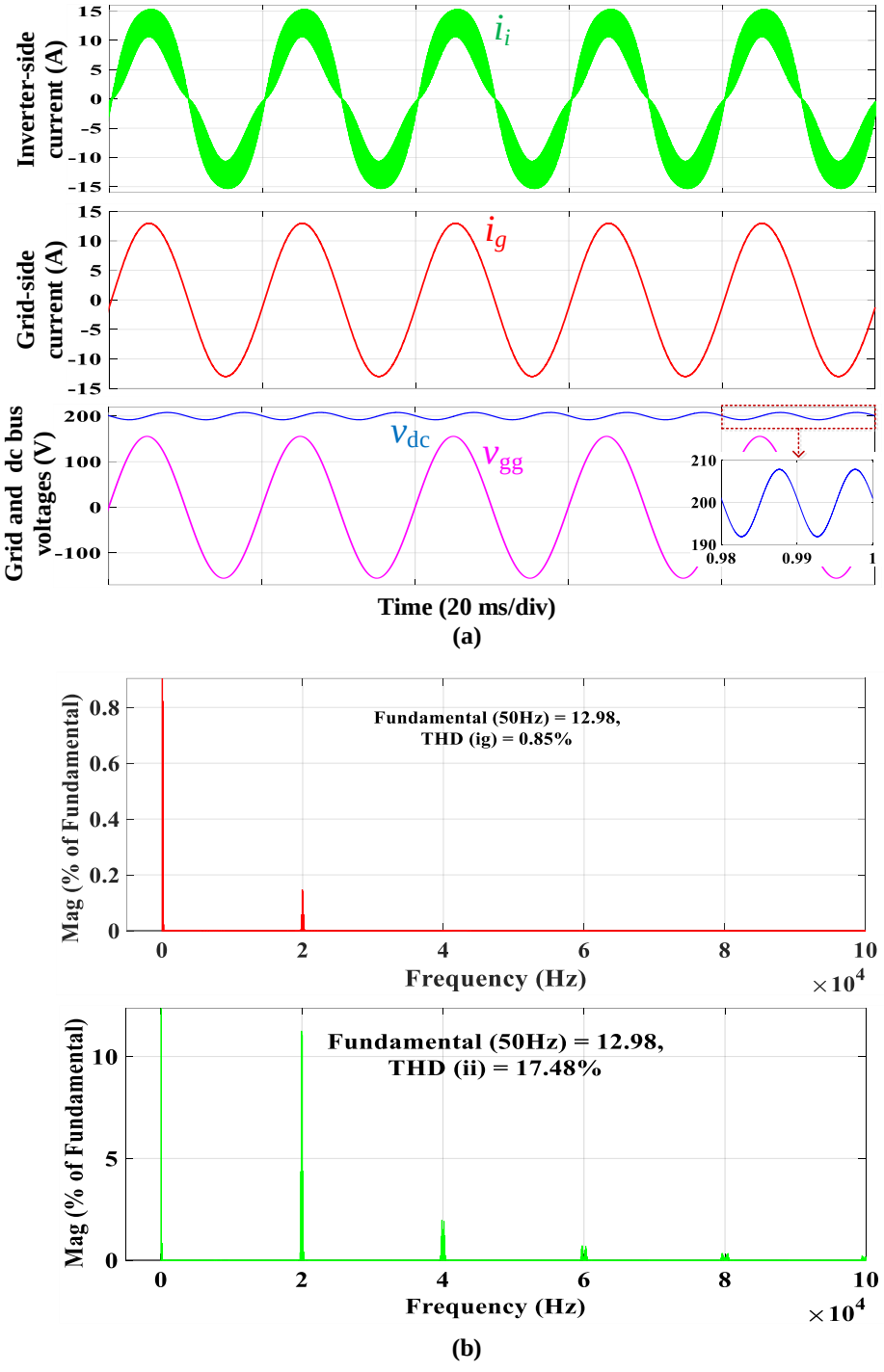


Figure 10. Simulation results of the proposed *LTT* filter: (**a**) waveforms of currents and voltages; (**b**) grid-side and inverter-side currents' spectra.

For comparison, Figure 11a illustrates the waveforms when using an *SPRLCL* filter. This segment conducts a performance comparison for the presented filters and existing ones [26]. The *SPRLCL* filter, commonly used in the literature with two traps, was subjected to similar testing for a performance comparison with the *TTL* and *LTT* filters, as shown in Figures 9–11. When the *SPRLCL* filter replaces the *TTL* and *LTT* filters, the waveform of i_g remains sinusoidal, demonstrating that low-order harmonics are effectively managed. Figure 11b shows that harmonics at double and quadruple switching frequencies are also reduced. The harmonics at frequencies beyond four times the switching frequency are efficiently suppressed, with sixfold harmonics limited to 0.01% of the fundamental component. As shown in Table 3, the *SPRLCL* filter achieves a THD of i_g equal to 0.83%, meeting IEEE standards, albeit with larger filter components. Overall, the proposed filters perform similarly to the *SPRLCL* filter, validating their compact and effective design.

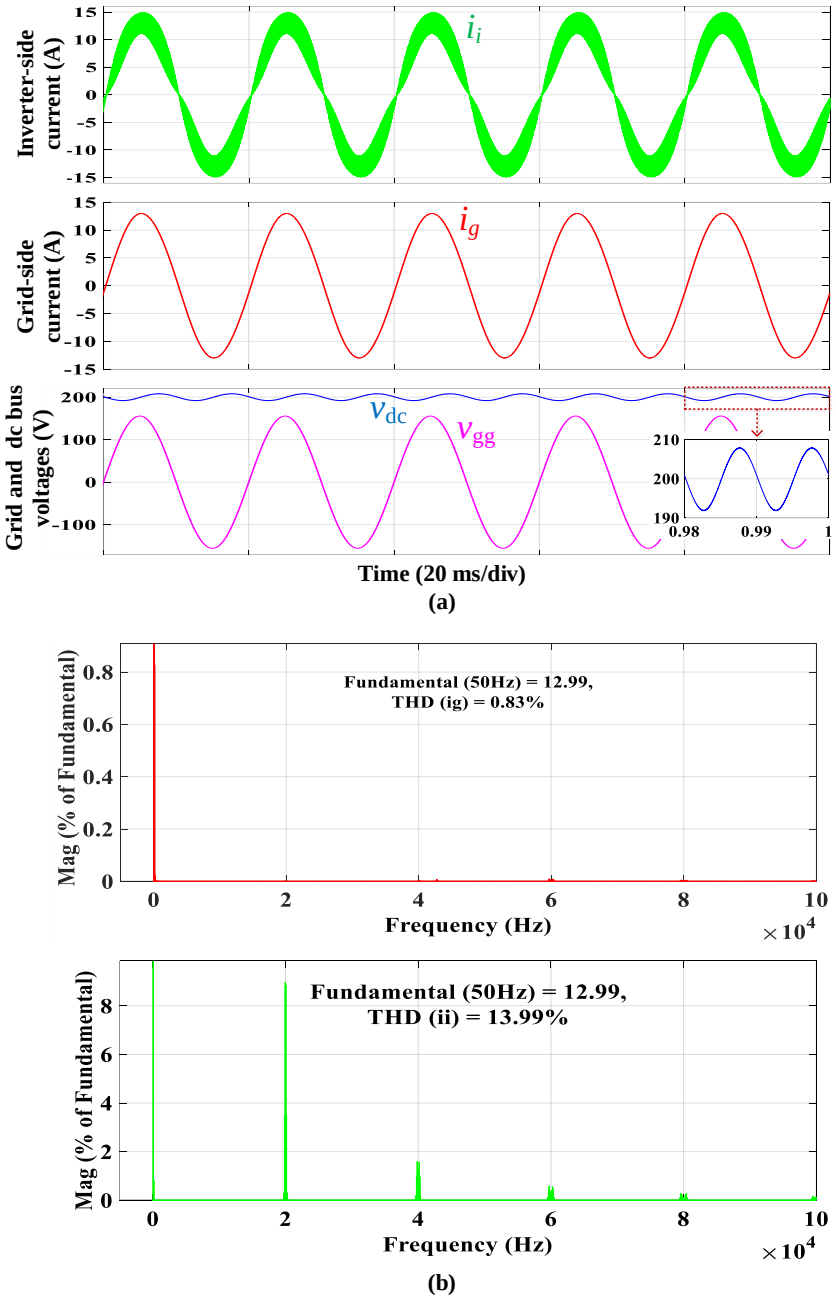


Figure 11. Simulation results of the discrete *SPRLCL* filter: (**a**) waveforms of currents and voltages; (**b**) grid-side and inverter-side currents' spectra.

The effectiveness of the proposed filters in mitigating current harmonics is further demonstrated through detailed FFT analysis. Figure 9b illustrates the harmonic spectra of the current before and after the implementation of the *TTL* filter. The results show significant attenuation at the dominant switching frequencies, $2f_{sw}$ and $4f_{sw}$, where the harmonics are reduced from 11.14% and 1.93% to 0.25% and 0.02%, respectively. Similarly, Figure 10b presents the harmonic spectra for the *LTT* filter, highlighting reductions at $2f_{sw}$ and $4f_{sw}$ to 0.15% and 0.00%, respectively. High-frequency harmonics beyond $4f_{sw}$ are also effectively suppressed, with components at $6f_{sw}$ reduced to negligible levels. These results validate the strong harmonic attenuation capabilities of the proposed filters. A comparison of the FFT results for both filters is provided in Table 3, showcasing their performance relative to the discrete *SPRLCL* filter. This expanded analysis provides a more detailed understanding of the harmonic suppression achieved by the proposed filters, reinforcing their compliance with IEEE 519-2014 standards and their suitability for practical applications.

Though all three filters achieve a THD below 5%, the required inductance varies. Moreover, the switching current harmonics at *LC*-trap frequencies are comparable across the three methods, affirming the effectiveness of the proposed approaches. Additionally, the *TTL* and *LTT* filters save two cores in comparison with the *SPRLCL* one, which translates to cost and size reductions. As shown in Table 3, the *SPRLCL* filter occupies a volume of 17.5×10^{-5} m^3, compared to the compact 11.3×10^{-5} m^3 size of each integrated filter. Furthermore, as can be seen in Figures 9b and 10b, the *LTT* filter slightly outperforms the *TTL* filter in harmonic suppression due to lower ripple on the grid-side inductance, resulting in marginally lower THD.

Dynamic testing was executed for the *TTL* filter, with the results shown in Figure 12. The load is reduced by 75% (from 40 Ω to 30 Ω) at t = 0.50 s. The *TTL* filter maintains stability despite the 25% load variation during the dynamic period. The DC-link voltage drop remained below 12 V, with a total transient duration of 0.06 s, then smoothly returned to its setpoint, demonstrating the robust design.

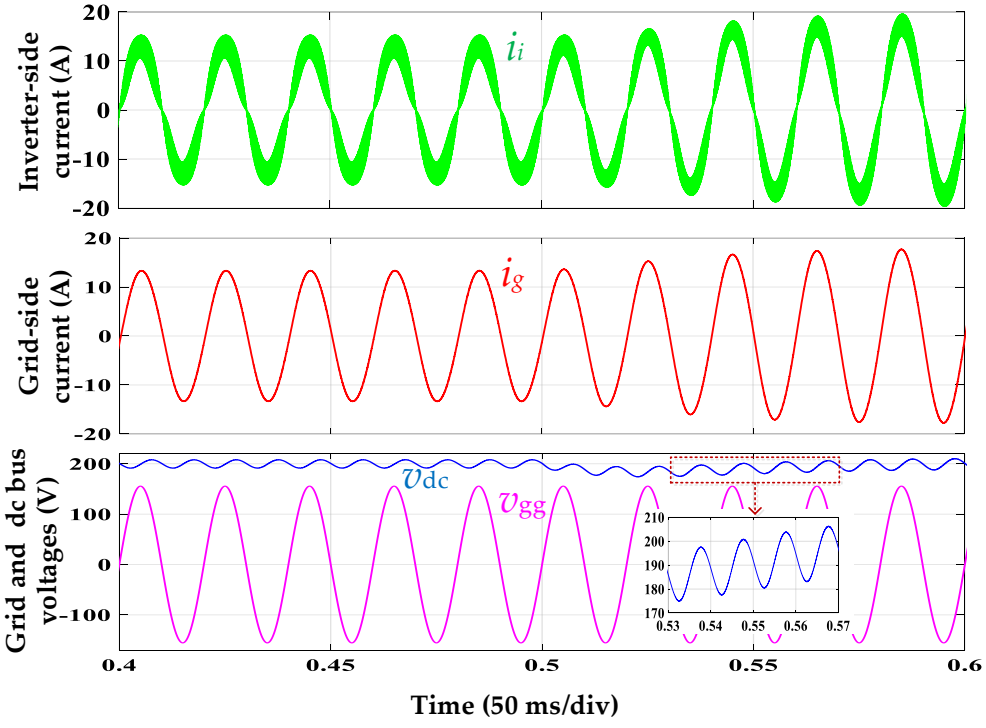


Figure 12. Simulation dynamic waveforms with a 10 Ω load step-down using the proposed integrated *TTL* filter.

The *LTT* filter was also subjected to dynamic testing, with load variation waveforms shown in Figure 13. At t = 0.50 s, the load was stepped down from 40 Ω to 30 Ω, assessing the filter's ability to follow command changes. Similar to Figure 12, the dynamic behavior was consistent, as the current controller was designed similarly. The instability suppression of the filter, i.e., to return to its setpoint, is the essential requirement in dynamic states. The *LTT* filter effectively maintains stability during load changes, with the DC-link voltage briefly decreasing before gradually returning to the setpoint.

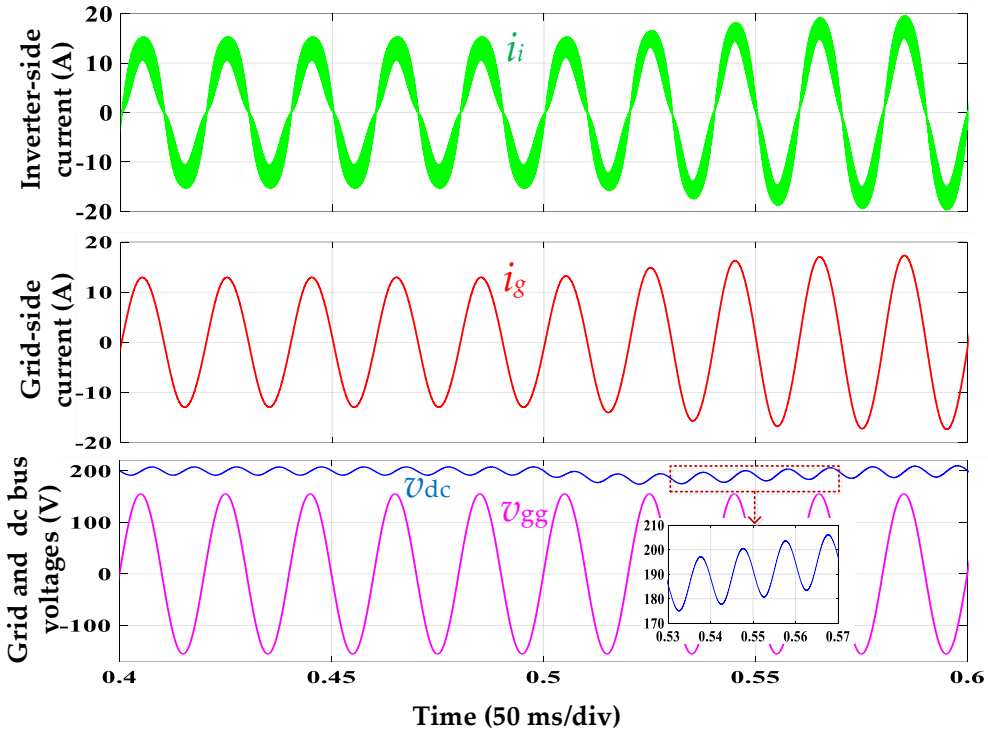


Figure 13. Simulation dynamic waveforms with a 10 Ω load step-down using the proposed integrated *LTT* filter.

Section 3.2 indicates that the integrated inductors were designed with a sufficient margin to prevent current saturation. The maximum current in this example is 20 A, or $I_{il\max} = I_{gl\max}$ = 20 A. System transients were examined by applying a step change in DC voltage to assess current saturation at this maximum. A 40 V step-up in V_{dc} (from 200 V to 240 V) was applied at t = 0.50 s to evaluate the transient response and current saturation using the integrated *TTL* filter. The results, shown in Figure 14, demonstrate that the *TTL* filter maintains stability, with the system operating normally during transients even at the peak current. The filter encountered minor transients before returning smoothly to the setpoint without oscillations, indicating robust switching harmonic suppression.

Figure 15 illustrates the transient simulation results for the integrated *LTT* filter when the DC-link voltage V_{dc} is increased by 40 V (from 200 V to 240 V) at t = 0.5 s. The gains for the current controller are similar to those used in the previous test with the *TTL* filter. As shown, the resulting waveforms closely resemble those in Figure 14, confirming the filter's stability and its ability to attenuate switching harmonics. Although the filter experiences brief transients, it quickly returns to the setpoint without fluctuations. The system's transient response takes a short time to stabilize before the current starts following its reference, with the entire transient phase lasting only around 60 ms.

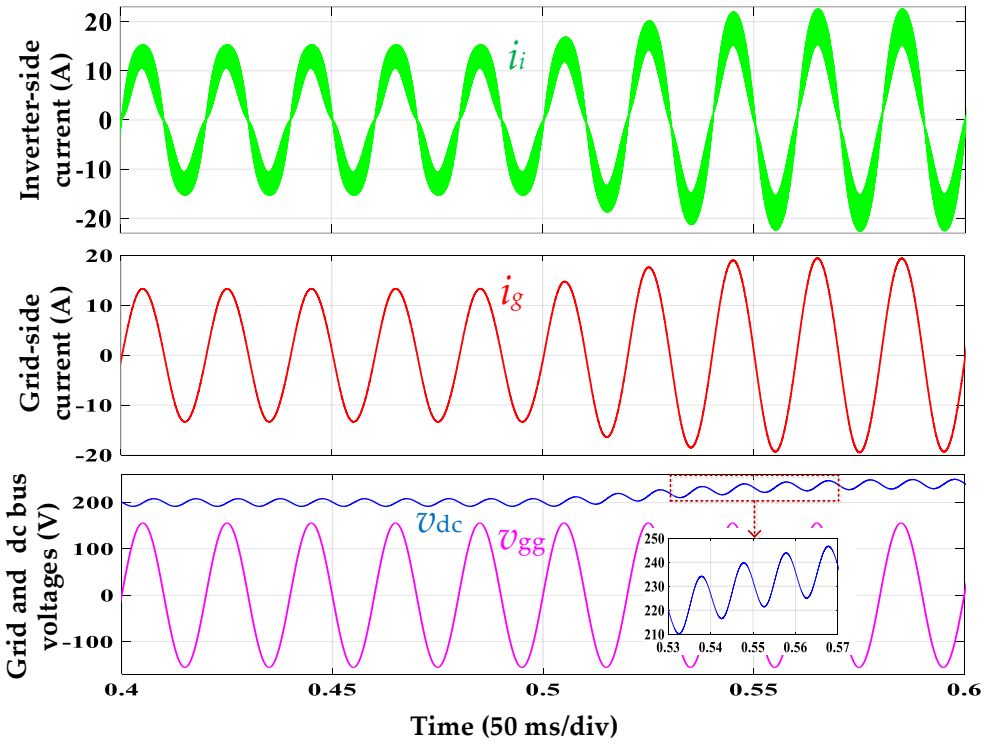


Figure 14. Transient simulation waveforms with a 40 V step-up in the DC-link voltage using the integrated *TTL* filter.

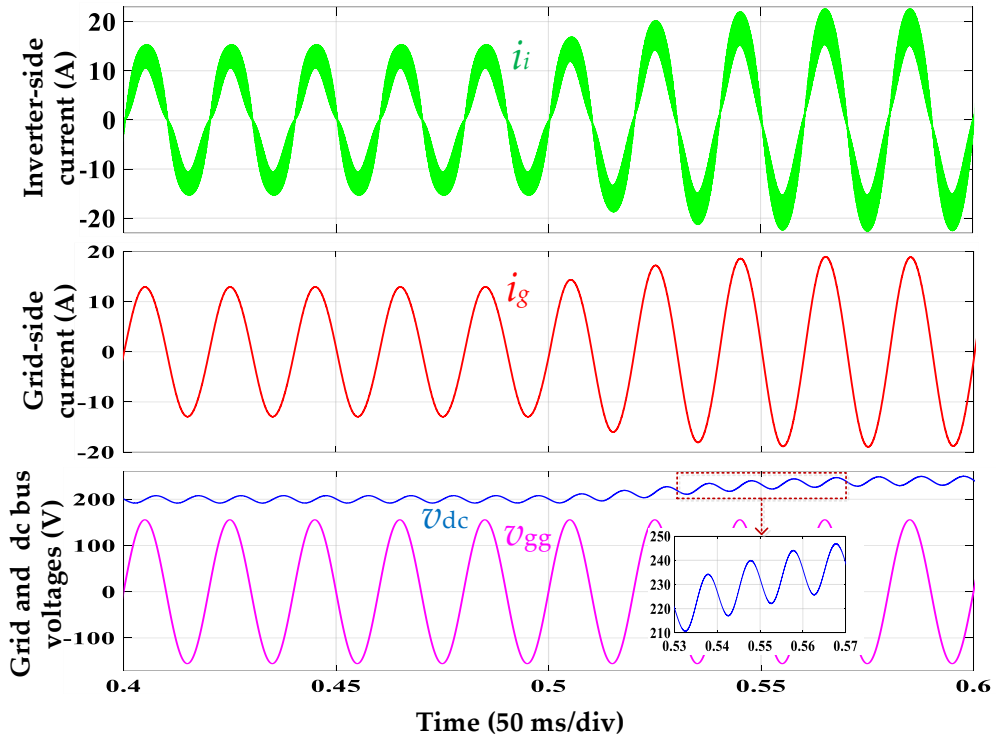


Figure 15. Transient simulation waveforms with a 40 V step-up in the DC-link voltage using the integrated *LTT* filter.

According to earlier studies [43,65], the resonance poles of the *TTL* and *LTT* filters can be further dampened by L_s. As can be seen in Figures 12–15, this added damping minimizes ringing in the grid-side current. However, the system's overall dynamic response takes

longer to stabilize, as it requires more time for the current to align with the reference, resulting in a slightly extended dynamic period.

4.2. HIL Experimental Results

An HIL testing platform was developed to assess and validate the proposed filters' performance. A primary benefit of the HIL experiment setup is its ability to evaluate the prototype without requiring physical components, as depicted in Figure 16 [73]. HIL provides additional benefits, allowing designers to bypass environmental constraints and natural testing. Since HIL simulations can emulate plant models, this approach is cost-effective. HIL testing reduces both the cost and time associated with physical validations, as well as the development time for modifications across various scenarios [74,75]. Moreover, HIL tests enable quick identification and reconfiguration of barriers, accelerating real-time testing compared to traditional methods. HIL's precision, affordability, and flexible scheduling make it advantageous over physical tests.

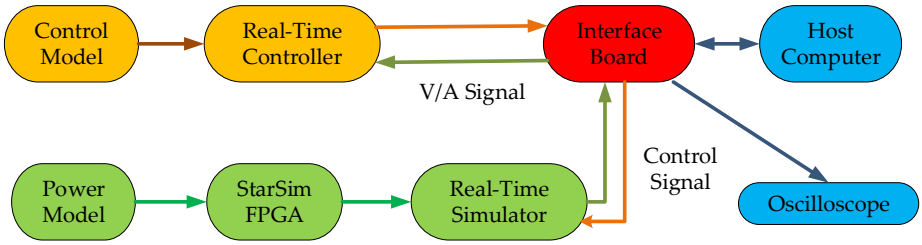


Figure 16. Diagram of HIL experiment platform.

This testing method holds significant potential in both industrial and academic settings, because of HIL's capability of providing a secure, rapid prototyping environment for research and development [31,38,43,73–97]. For large, complex systems, HIL creates a safe testing environment. HIL is particularly effective for assessing design methodologies in systems with complex, independent models, fast dynamics, or high switching frequencies [74,81,85,86,89–91,94–97]. As a modern technique, HIL is frequently used to test and validate power electronic systems [73,75,82–84,92]. HIL has proven valuable for evaluating network-tied converters with passive filters, addressing the challenges of complexity, cost, and stability requirements [31,36,38,43,82,83,85].

It should be noted that the presented filters are still in the research phase. Using the HIL platform for testing and evaluation is more cost-effective at this stage compared to developing physical prototypes, which may follow in later phases. It serves as a valuable verification approach for new design methods, allowing the assessment of system accuracy and efficiency without the expense of real implementation [36,74,81,85,86,88–91,93]. This study uses the standard HIL approach to represent the proposed filters. Based on previous work [31,36,38,43,82,83,85], it is believed that HIL testing provides results that closely match actual physical tests. The HIL setup includes the components illustrated in Figure 17. Furthermore, it conforms to OXI-5 PXI hardware standards, offering enhanced synchronization and high reliability, minimizing repair times [75].

MATLAB/Simulink was used to program the control system, utilizing a fixed-step solver. The HIL testing was performed using StarSim (https://www.modeling-tech.com/en/products/144.html, accessed on 13 December 2024), a real-time simulation system software developed by ModelingTech (Shanghai, China). Models for the control circuit and grid-tied inverter with filters were included in the StarSim environment. The closed loop is formed when these models are executed on the RTC and RTS, respectively. The parameters here are like those adopted in the simulation stage. Voltage and current

waveforms were monitored using a scope, with experimental waveforms later analyzed in MATLAB/Simulink using the Powergui FFT Analysis Tool.

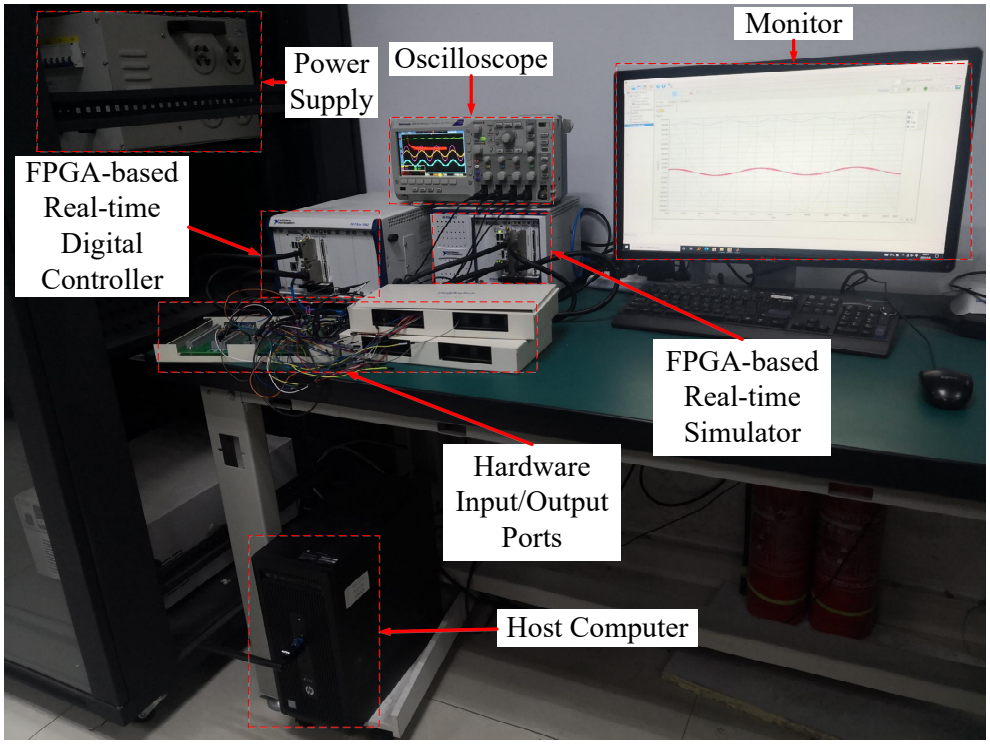


Figure 17. Setting of HIL experiments.

Only the *LTT* filter's performance in this experiment is presented, as its waveforms were similar to those obtained from the *TTL* filter. Figure 18 shows the experimental waveforms and harmonic spectrum of i_g for the *LTT* filter. The control system maintains V_{dc} close to 200 V, with an error of just 8 V (4%). The i_g is well-filtered, exhibiting a highly sinusoidal waveform. By tuning the two traps to 20 kHz and 40 kHz, current-switching harmonics are significantly minimized. As the current harmonics fall below the 0.3% criterion, this filter adheres to IEEE 519-2014 requirements.

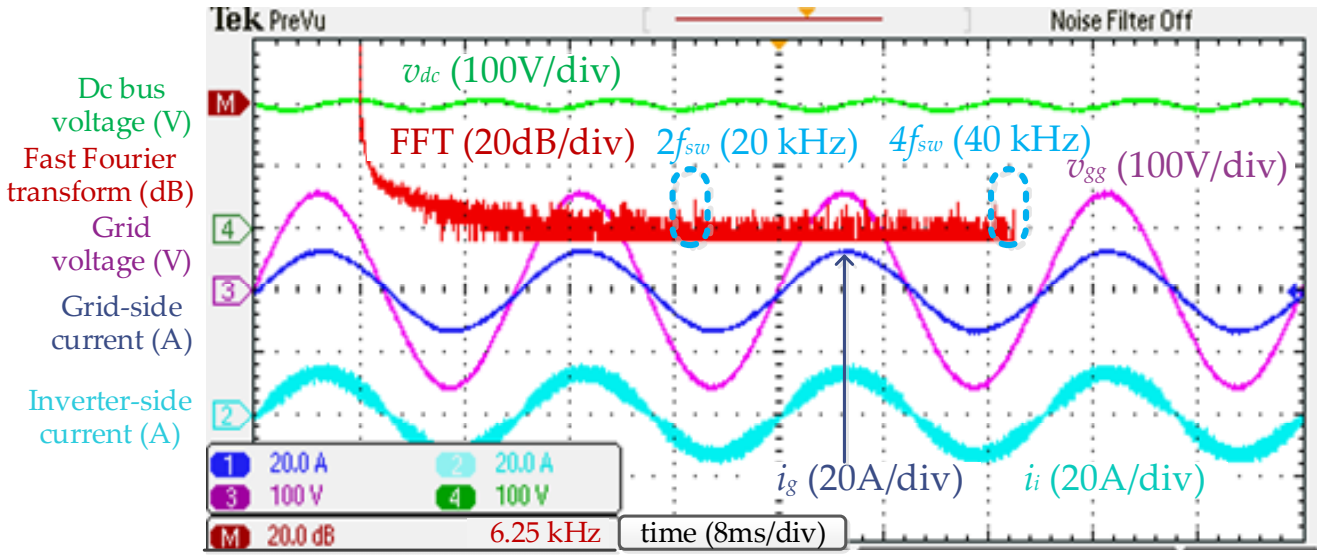


Figure 18. Experimental waveforms and grid-side current spectrum for the integrated *LTT* filter.

For a comparison, Figure 19 shows the experimental results with the *SPRLCL* filter replacing the *LTT* filter. The i_g waveform remains sinusoidal, confirming that low-order harmonic mitigation is maintained. The double- and quadruple-switching frequencies' harmonics are also effectively reduced. When compared with Figure 18, the proposed filters exhibit a comparable performance to the discrete *SPRLCL* filter, highlighting their effectiveness despite their smaller size.

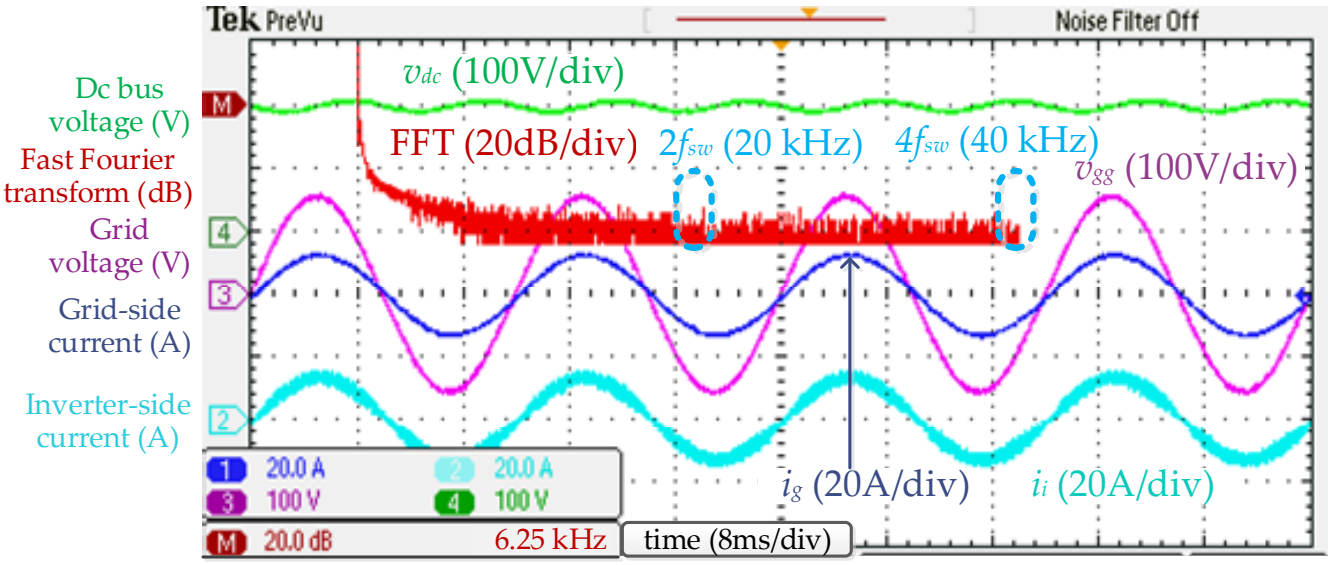


Figure 19. Experimental waveforms and grid-side current spectrum for the discrete *SPRLCL* filter.

Even though the proposed magnetic integrated *TTL* and *LTT* filters have the advantage of lower weight and size than the discrete *SPRLCL* filter, the power losses of their inductors must also be examined for a fair comparative analysis. The direct measurement or calculation of the inductors' power losses is difficult because of the vast quantities of switching harmonics in the inverter-side output voltage v_{in} and current i_i. Thus, the system efficiency is calculated under the same conditions to compare the inductors' power losses of the three selected filters. The system efficiency is calculated by P_o/P_{in}, where P_{in} is the active input power calculated by $P_{in} = V_{gg}I_{g\text{rms}}$ in unity factor working conditions, and P_o is the dc side output power calculated by $P_o = V_{\text{dc}}I_{dc}$. V_{gg} and $I_{g\text{rms}}$ are the RMS values of v_{gg} and i_g, respectively, while V_{dc} and I_{dc} are the average values of v_{dc} and i_{dc}, respectively, which can indeed be measured or calculated directly. The losses are calculated by subtracting P_o from P_{in}. When subjected to circumstances corresponding to a full load, the system efficiencies of the integrated *TTL* and *LTT* and discrete *SPRLCL* filters are 94.36%, 97.25%, and 97.23%, respectively, indicating that these three filters have losses of 59.77 w, 28.28 w, and 28.49 w, respectively. As can be seen, except for the integrated *TTL* filter, the efficiency is roughly the same and greater than 97.2%, indicating low system power losses. As can be observed, the efficiency with the proposed integrated *TTL* filter is slightly less than that with the other two filters because the ripple is large on the inverter-side inductance.

To test the dynamic response of the integrated *LTT* filter, a step change in the DC load resistance from 40 Ω to 30 Ω was introduced at t = 0.5 s. Figure 20 shows the dynamic performance, indicating that the system handles load changes well, similar to the simulation results shown in Figure 13. The primary requirement during dynamic conditions is the capability of the filter to maintain stability, measured by returning to its setpoint. The *LTT* filter remains stable under load changes, with the DC-link voltage dipping before gradually returning to its setpoint.

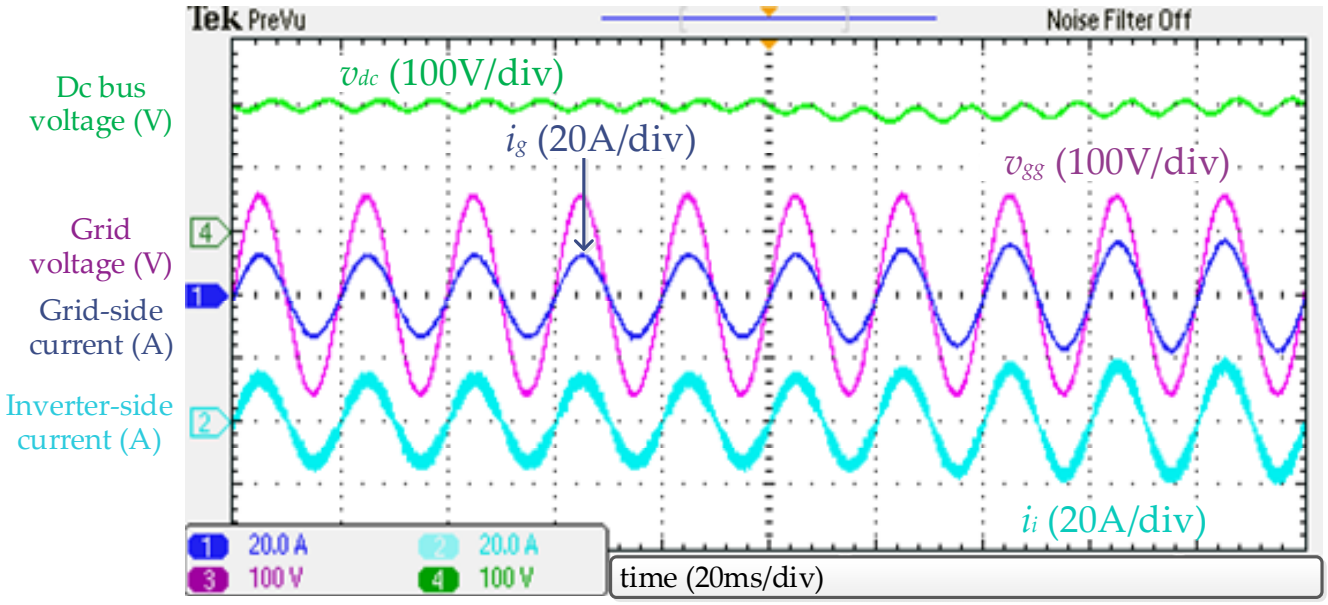


Figure 20. Experimental dynamic waveforms with a 10 Ω load step-down using the integrated *LTT* filter.

A transient test was also conducted on the *LTT* filter, where a 40 V step-up variation in V_{dc} was applied. The experimental results, shown in Figure 21, are consistent with the simulated results in Figure 15, verifying that the filter maintains stability while attenuating switching harmonics. The *LTT* filter experiences minor transients before returning to the setpoint, which demonstrates the system's resilience. Despite the transient phase lasting only around 60 ms, the system quickly stabilizes as the current begins to follow the reference.

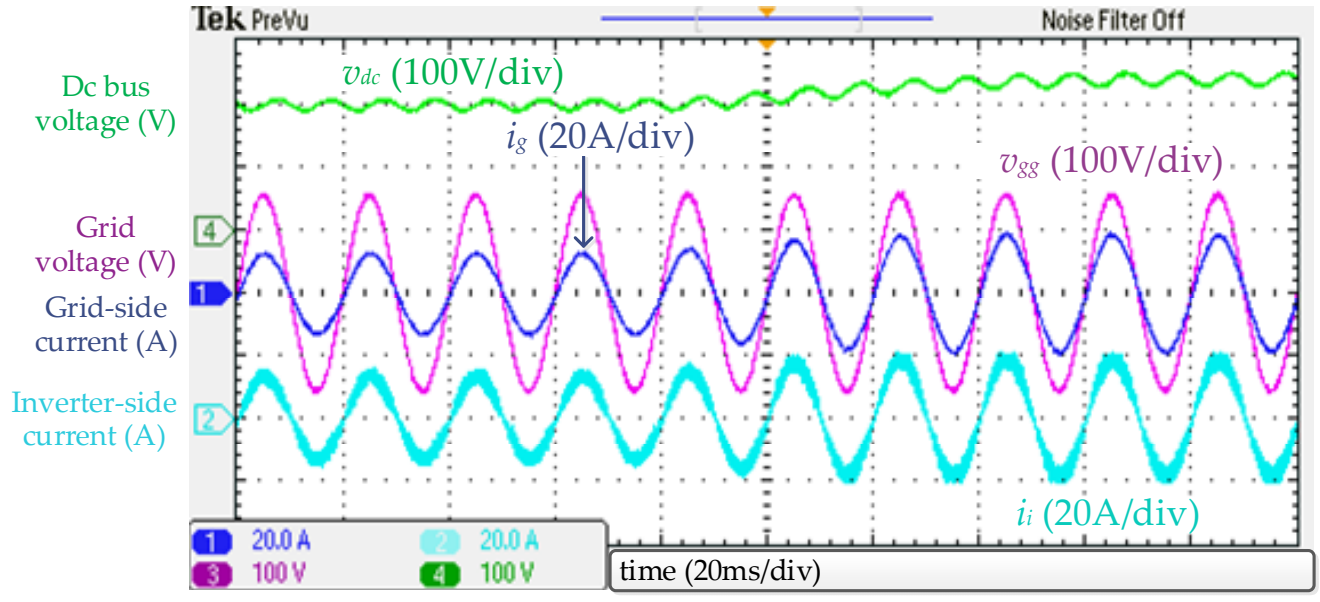


Figure 21. Experimental transient waveforms with a 40 V step-up in DC-link voltage using the integrated *LTT* filter.

The comparison between the proposed *TTL* and *LTT* filters is summarized here to identify the most suitable topology for practical applications. Both filters achieve similar steady-state harmonic suppression, with THD levels of 0.90% and 0.85%, respectively, meeting IEEE 519-2014 standards. Additionally, both designs successfully attenuate har-

monics around the dominant switching frequencies ($2f_{sw}$ and $4f_{sw}$), demonstrating strong trapping capabilities. However, a closer evaluation reveals notable differences. The *LTT* filter exhibits better efficiency (97.25%) than the *TTL* filter (94.36%) due to reduced ripple on the inverter-side inductance. Furthermore, the *LTT* filter demonstrates a slightly better performance in dynamic scenarios, with faster stabilization times and lower transient voltage fluctuations. On the other hand, the *TTL* filter has a simpler design, making it easier to implement and more cost-effective for applications where these factors are prioritized. Considering the performance indices and practical requirements, the *LTT* filter emerges as the more suitable option for applications where efficiency, power quality, and dynamic performance are critical. The *TTL* filter, however, remains a viable alternative for systems with lower complexity and cost constraints.

In general, the experimental results align closely with the simulation data and theoretical analyses presented earlier. The performance of the proposed *TTL* and *LTT* filters was evaluated in this study against existing solutions, such as the *SPRLCL* filter, as described in this section. Both the simulations and experiments confirm the theoretical accuracy, validating that the proposed integrated *TTL* and *LTT* filters retain the benefits of the *SPRLCL* filter while addressing its limitations. These results demonstrate the performance similarity of the proposed filters and the *SPRLCL* filter, validating the designing robustness. While achieving comparable harmonic suppression (THD levels of 0.90% and 0.85%, respectively, versus 0.83% for the *SPRLCL* filter), the proposed filters offer significant size reductions, with core volumes reduced by approximately 35%. This compact design eliminates the need for additional magnetic cores, simplifying configurations and reducing costs compared to traditional solutions like *LTCL* and *LCL-LC* filters. In addition, the integration of magnetic components in the proposed filters improves efficiency by minimizing core losses and parasitic elements. Moreover, the integrated *TTL* and *LTT* filters exhibit flexibility and stability across different operating conditions.

Furthermore, incorporating planar transformers with PCB trace windings offers a potential pathway for further reducing filter size and improving performance. These designs are particularly advantageous for their compactness, reduced leakage inductance, and excellent thermal characteristics. However, challenges such as parasitic capacitances, thermal dissipation, and manufacturing complexity need to be addressed for high-power applications. Future work can explore optimized designs based on the insights provided in recent studies, such as [98], which demonstrate significant improvements in reducing parasitic capacitance and enhancing efficiency in high-frequency converters.

5. Conclusions

This paper presents magnetic integrated multi-trap filters, designated as *TTL* and *LTT*, developed for grid-connected inverters to reduce the size and weight of inductors while effectively suppressing the primary switching harmonics in the current. Built upon traditional *LCL* filters, the proposed design incorporates small trap capacitors in parallel with both the inverter-side and grid-side inductors to form one trap. A second trap was achieved by incorporating the coupling inductor, generated through magnetic coupling between the grid-side and inverter-side inductors, into the filter capacitor branch. By following a step-by-step design approach, these two *LC* traps can be tuned to target specific harmonic frequencies. The proposed filters deliver harmonic suppression comparable to discrete multi-trap configurations, like the *SPRLCL* filter, while saving the two cores of trap inductances. Moreover, these filters have a magnetic core structure resembling that of integrated *LCL* filters but with an enhanced harmonic suppression performance. For this design, the resonance frequency was fixed above the Nyquist frequency. A comprehensive, step-by-step design method is provided to facilitate parameter selection. Additionally,

these filters are robust enough to accommodate variations in grid impedance. Following MATLAB/Simulink simulations and HIL experimental models, the verification results confirm that the integrated *TTL* and *LTT* filters offer several advantages:

1. The proposed filters contain significantly fewer discrete passive components than discrete filter designs, achieving a size reduction of 35.4%.
2. They provide efficient harmonic suppression, achieving a grid-side current THD below 0.90%.
3. The approach enables the creation of adaptable filters with effective inductor integration.
4. The design demonstrates strong reliability and stability under dynamic and transient conditions.

However, passive-filtered converters must maintain stable grid connectivity and support fault ride-through during grid faults to prevent system instability. Addressing this issue and developing a solution will be essential areas for future research.

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