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HIL-Based Fault-Tolerant Vector Space Decomposition Control for a Six-Phase PMSM Fed by a Five-Level CHB Converter

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Abstract: The growing demand for higher reliability and efficiency in modern electric drives, coupled with the increasing adoption of multi-phase machines, has necessitated advancements in fault-tolerant control strategies. This paper presents a fault tolerance analysis for a six-phase permanent magnet synchronous machine (PMSM) connected to a five-level cascaded H-bridge converter, employing a level-shift pulse width modulation (LSPWM) technique. Unlike existing strategies, this work integrates a unique combination of three key innovations: first, a fault detection mechanism capable of identifying faults in both machine phases and inverter legs with high precision; second, an open-circuit fault compensation strategy that dynamically reconfigures the faulty inverter phase leg into a two-level topology to reduce losses and preserve healthy switches; and third, a modified closed-loop control method designed specifically to mitigate the adverse effects of short-circuit faults while maintaining system stability. The proposed approach is validated through rigorous simulations in Simulink and Hardware-in-the-Loop (HIL) tests, demonstrating its robustness and applicability in high-reliability applications.

Keywords: cascade H-bridge (CHB); multi-level inverter (MLI); fault tolerance; level-shifted pulse width modulation (LSPWM); multi-phase PMSM

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1. Introduction

In recent years, significant advancements in the renewable energy sector, particularly in offshore energy systems (e.g., wind and tidal turbines) and electric vehicles, have driven the demand for high-efficiency and high-reliability electric drives. This has intensified interest in advanced systems, including multi-phase machines, multi-level inverters, and sophisticated fault-tolerant control techniques. Among these, multi-phase permanent magnet synchronous machines (PMSMs) have emerged as a promising solution in renewable energy applications due to their numerous advantages. In particular, PMSMs are widely used in the transportation sector due to their efficiency, high power density, and advanced control capabilities, which align with the focus of this research on fault-tolerant strategies [1,2]. These include high power density, a superior torque-to-current ratio, cost-effectiveness, versatility across operating speeds, the elimination of gearboxes, and reduced excitation power losses thanks to the absence of an excitation current requirement [3,4].

The six-phase PMSM, particularly with a symmetrical configuration and a 60° phase shift between two winding sets, offers further advantages such as reduced harmonic distortion, enhanced operational reliability, and improved fault tolerance and power quality. These features make six-phase PMSMs especially suitable for applications requiring high

fault tolerance and smooth operation, such as renewable energy systems and electric vehicles, where system robustness and efficiency are paramount [5–7]. In parallel, the adoption of multi-level inverters (MLIs) continues to rise, driven by their superior reliability and efficiency. MLIs are cost-effective solutions that improve power quality by reducing Total Harmonic Distortion (THD) and minimizing voltage stress on components. This makes them ideal for medium- and high-power applications, where power quality is critical [8–11]. Various topologies of MLIs have been extensively studied, including diode-clamped (neutral-point-clamped), cascaded H-bridge, flying capacitors, and hybrid inverters [12–15]. Among these, the cascaded H-bridge (CHB) topology stands out for its modular nature, scalability, and fault tolerance, making it widely used in grid interface applications [16,17]. The integration of CHB inverters with six-phase electric machines has garnered significant attention due to their modularity, scalability, and the high reliability they offer in fault-tolerant operation. Fault tolerance is essential for maintaining uninterrupted operation in critical applications such as renewable energy systems, electric vehicles, and marine propulsion [18–20]. Effective fault tolerance begins with timely fault detection and accurate diagnosis, which are essential to avoid system failure. Fault tolerances generally fall into several main categories, each contributing to improved system resilience [21–43]. These methods can be broadly categorized into four main approaches, each contributing to improved system resilience: (1) model-based fault diagnosis, (2) signal processing techniques, (3) hardware redundancy and (4) advanced modulation strategies. Model-based fault diagnosis plays a crucial role by enabling real-time comparisons between measured system data and expected behavior derived from mathematical models. Deviations detected through this approach allow for the identification and localization of faults, facilitating timely mitigation measures [21–25]. Complementing this, signal processing techniques such as wavelet transforms, Fast Fourier Transforms (FFTs) and machine learning algorithms analyze system signals to detect fault-specific features, proving particularly effective in isolating faults in multi-phase machines [26–32]. Additionally, hardware redundancy, which involves incorporating redundant modules or components such as additional H-bridge cells in CHB inverters, ensures continuous operation despite component failures. This strategy often works in conjunction with control algorithms that dynamically reconfigure the system to bypass faulty elements [33–37]. Advanced modulation strategies further enhance fault tolerance. Techniques like level-shifted pulse width modulation (LSPWM) and Space Vector Modulation achieve this by dynamically redistributing power and maintaining system stability during faults [38–43]. For instance, LSPWM is particularly effective in minimizing harmonic distortion and switching losses, which are critical under fault conditions. Based on the previous analysis, the comparisons of different fault tolerance methods are listed in Table 1.

Table 1. Comparison of fault tolerance methodologies.

References	Fault Tolerance Method	Description	Key Advantages
[21–25]	Model-Based Fault Diagnosis	Uses mathematical models to detect faults by comparing actual system behavior with expected behavior.	Real-time fault detection and localization; effective for multi-phase systems.
[26–32]	Signal Processing Techniques	Employs methods like FFT, wavelet transforms, and machine learning for fault feature extraction.	Accurate isolation of fault features; versatile for electrical and mechanical faults.
[33–37]	Hardware Redundancy	Incorporates extra components (e.g., additional H-bridge cells) to maintain operation during component failures.	High reliability; ensures continuous operation by bypassing faulty modules.

Table 1. *Cont.*

References	Fault Tolerance Method	Description	Key Advantages
[38–43]	Advanced Modulation Strategies	Implements modulation techniques like level-shifted PWM (LSPWM) to redistribute power and maintain stability during faults.	Reduces harmonic distortion, minimizes switching losses, and enhances power quality during fault conditions.

Integrating fault-tolerant strategies is especially vital in multi-level inverters, where fault propagation can compromise overall system performance. CHB inverters, in combination with six-phase PMSMs, are highly suited for fault-tolerant applications due to their modularity and ability to isolate faults effectively. Research demonstrates that reconfiguring a five-level CHB inverter into a two-level topology during a fault maintains operational stability while minimizing power loss [44,45]. The current fault-tolerant approaches for six-phase PMSM with a five-level CHB inverter have some limitations, such as the accurate detection rate and localization of faults on both machine phases and the inverter. This constraint may postpone fault isolation and decrease the system's reliability in crucial tasks. Moreover, classical fault compensation techniques are not sufficient for dealing with open- or short-circuit faults in modular structures such as the five-level CHB. These disadvantages lead to higher power losses and unbalanced phase currents, as well as lower efficiency in general. Moreover, previous methods typically suffer from a lack of robustness under critical fault conditions, especially when multiple faults occur at the same time or affect critical parts of the system. It is worth noticing that many fault-tolerant algorithms are computationally expensive and their resource consumption limits their ability to be employed in real-time applications, particularly in high-velocity or resource-constrained environments.

Despite advanced modulation strategies like level-shifted pulse width modulation (LSPWM) being used to improve system performance, there is a gap in their integration in fault-tolerant structures dedicated to five-level CHB inverters, which are still underexplored and underdeveloped. Furthermore, conventional approaches typically employ fault tolerance mechanisms in isolated layers and are concerned only with fault detection, compensation, or adaptation of control, extending the functions into distinct layers without a unified framework. These limitations highlight the need for a broader and more cohesive approach to fault tolerance. The latter requires that concerns related to fault detection, compensation and control adaptation be treated in a coordinated way and that the specific benefits of both the six-phase PMSM and the five-level CHB topology be exploited to increase reliability and efficiency.

This research focuses on a five-level CHB inverter integrated into a six-phase PMSM drive. The level-shifted pulse width modulation (LSPWM) technique, recognized for its ability to reduce THD and switching losses, improves power quality and efficiency by distributing switching signals across voltage levels. This approach also introduces fault-tolerant operation capabilities [33–43]. A five-level inverter strikes an optimal balance between performance and complexity, offering sufficient harmonic suppression without the excessive control challenges of higher-level inverters [44]. In particular, the proposed paper integrates various fault tolerance approaches to improve system reliability and robustness, such as model-based fault diagnosis, hardware redundancy and advanced modulation strategies. The five-level CHB topology used in this study consists of two H-bridge modules per phase, each with an isolated DC supply, resulting in a total of 12 H-bridge modules and 48 switches for a six-phase PMSM drive. The phase voltage is formed by summing the outputs of the two H-bridge modules to achieve a five-level voltage profile. A Vector Space Decomposition (VSD) fault-tolerant control method is applied to ensure balanced operation and minimize harmonic distortion. In this work, VSD has been modified to further enhance

fault tolerance. The proposed approach introduces additional proportional–integral (PI) controllers to the auxiliary subspaces, designed to suppress harmonics and mitigate the effects of open-circuit and short-circuit faults. The transformation matrices used in VSD are dynamically adjusted upon detecting a fault, ensuring that the remaining healthy phases maintain orthogonality and balanced operation. This tailored adaptation allows the system to transition seamlessly from normal operation to fault-tolerant modes, minimizing performance degradation and maintaining reliability.

By integrating these modifications, the proposed system demonstrates significant improvements in fault detection, isolation, and compensation, as validated through simulation and Hardware-in-the-Loop (HIL) experiments. These innovations establish the framework as a robust solution for high-reliability applications, addressing the growing demand for efficient and resilient electric drive systems.

The paper is structured as follows: Section 2 presents the mathematical model of the six-phase PMSM. Section 3 details the multi-level cascaded H-bridge inverter (MCI) topology. Section 4 introduces the fault-tolerant control strategy. Simulation results and Hardware-in-the-Loop (HIL) experimental tests are provided in Sections 5 and 6, respectively. Conclusions are summarized in Section 7.

2. Mathematical Model of the System

A symmetrical six-phase permanent magnet synchronous machine (PMSM) topology, consisting of two sets of three-phase windings with a 60° electrical phase shift and a common neutral point, is depicted in Figure 1. The application of this model is beneficial due to its ability to significantly reduce harmonics of magnetic force (MMF) and improve overall power quality [45]. The six-phase arrangement also enhances operational performance by minimizing torque ripples, which is essential for smooth and stable operation. Additionally, this configuration improves fault tolerance, making it an ideal choice for applications where reliability is paramount. For instance, offshore energy systems or electric vehicles can greatly benefit from this design due to its robustness in adverse conditions. Moreover, the symmetrical setup simplifies the control strategies, reducing the complexity of the control algorithms required for the system's operation. This ease of control makes it an attractive solution for practical implementation in high-performance and safety-critical applications [29]. Other alternative configurations are asymmetrical six-phase PMSM or concentrated winding. These options can also achieve fault tolerance, but they are generally not as efficient as the current model for high harmonic content and increased control complexity, rendering them non-ideal for the higher reliability applications targeted in this work. The assumptions underlying this analysis are as follows: the three-phase output with 60° phase differences is perfectly balanced, the normal operation of the orthogonal subspaces remains unaffected, and the magnetic properties of the PMSM are assumed to be linear, with no saturation effects. While simplifying the analysis, these assumptions come with limitations. In actual applications, windings may be asymmetric, or saturation effects could cause slight differences in the performance of a system measured against an ideal case. Future studies might include these non-idealities for further accurate modeling.

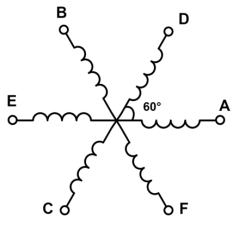


Figure 1. Configuration of a symmetrical six-phase (A–F) PMSM.

The dynamic model of the PMSM can be expressed in (1) and (2), where V_s, i_s, Ψ_s, Ψ_{PM} and Ls are, respectively, the stator voltage, current, flux linkage, permanent magnet's flux linkage and the synchronous inductance. In (2), $F(\vartheta)$ represents a function of the phase angle between the two sets of windings defined in (3). The electromagnetic machine torque τ_e can be expressed by (4), where n_p is the pole-pair number. The resistance R_s and inductance L_s matrix are defined in Equations (5)–(7).

$$V_s^{abcdef} = R_s^{abcdef} \cdot i_s^{abcdef} + \frac{d\Psi_s^{abcdef}}{dt}, \tag{1}$$

$$\Psi_s^{abcdef} = L_s^{abcdef} \cdot i_s^{abcdef} + \Psi_{PM}^{abcdef} \cdot F(\vartheta), \tag{2}$$

$$F(\vartheta) = [cos(\vartheta), cos(\vartheta - 60), cos(\vartheta - 120), cos(\vartheta - 180), cos(\vartheta - 240), cos(\vartheta - 300)]^T \tag{3}$$

$$\tau_e = \frac{1}{2} n_p \frac{\partial}{\partial \theta_m} \left(i_s^{abcdef} \cdot \Psi_s^{abcdef} \right) \tag{4}$$

$$R_s^{abcdef} = R_s \cdot I_6, (\text{where } \mathrm{I_6} \text{ is an identity } 6 \times 6 \text{ matrix}) \tag{5}$$

$$L_s^{abcdef} = \begin{bmatrix} L_s & M_s & M_s & M_m & M_m & M_m \\ M_s & L_s & M_s & M_m & M_m & M_m \\ M_s & M_s & L_s & M_m & M_m & M_m \\ M_m & M_m & M_m & L_s & M_s & M_s \\ M_m & M_m & M_m & M_s & L_s & M_s \\ M_m & M_m & M_m & M_s & M_s & L_s \end{bmatrix} \tag{6}$$

$$L_s = L_{ls} + L_{lm} + L_m \tag{7}$$

$$M_m = \begin{bmatrix} M_1 & M_2 & M_3 \\ M_3 & M_1 & M_2 \\ M_2 & M_3 & M_1 \end{bmatrix} \tag{8}$$

$$M_s = cos\frac{2\pi}{3} \cdot L_m \tag{9}$$

$$M_i = cos\left(\frac{\pi}{3} + (i-1)\frac{2\pi}{3}\right) \cdot \left(\frac{2}{3} L_{lm} + L_m\right), \mathrm{i} = \{1, 2, 3\} \tag{10}$$

where L_{ls} is the leakage inductance, L_{lm} is the mutual leakage inductance and L_m is the magnetizing inductance. The mutual inductances M_s and M_i, which depend on the angular displacement between the different phases, are defined as (8)–(10). The VSD control strategy in Section 4 is based on this mathematical model, which provides the framework for current decoupling of the transformation matrix to control the torque and flux independently through *dq* subspaces.

3. Topology of MCI

The cascaded H-bridge multi-level inverter (CHB MCI) consists of several H-bridge modules connected in series to achieve a desired voltage level. The number of H-bridge modules required to reach a specific voltage level can be determined using the formula $(m-1)/2$, where 'm' represents the desired number of levels [14]. For example, to achieve a five-level inverter, two H-bridge modules are needed for each phase. Figure 2 illustrates the topology of the six-phase five-level cascaded H-bridge inverter (5LCHBI) used in this study. Compared to lower-level inverters such as the three-level inverter, the 5LCHBI offers several advantages, including reduced Total Harmonic Distortion (THD), improved fault tolerance, and reduced stress on the switches. These benefits arise because the total voltage is divided into multiple levels, making the system more efficient and reliable [32,46]. While

a nine-level inverter may offer even better results in terms of THD reduction and voltage quality, it introduces significant challenges. The increased complexity of the control system and the higher cost make nine-level inverters less practical for many applications [47]. In contrast, the five-level inverter strikes a balance between performance and practicality, offering a robust solution for various applications. The modular structure of the CHB topology also enhances fault tolerance. If a fault occurs, such as an open- or short-circuit fault of the switch located in the module, the inverter can bypass the faulty module and continue to operate at a reduced voltage level, utilizing the remaining healthy inverter legs [35]. Figure 3 provides an example of this fault-tolerant operation.

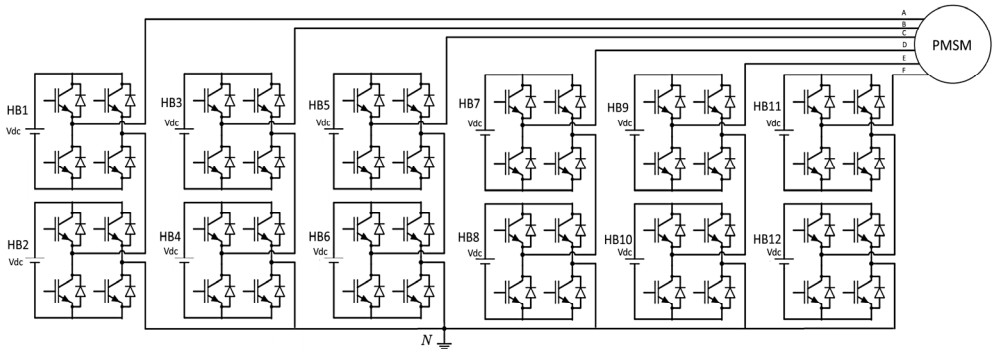


Figure 2. Topology of a six-phase (A–F), five-level cascade H-bridge inverter.

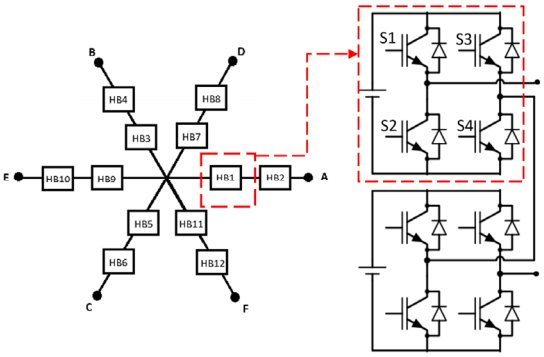


Figure 3. Fault in MCI CHB modules in 6 phase inverter (A–F).

In the case of an open-circuit fault in switch S_3 of module HB1 in phase A, the control strategy deactivates the upper switches (S_1, S_3) and activates the lower switches (S_4, S_2). As a result, the faulty phase operates as a three-level inverter instead of a five-level inverter, but with minimal power reduction. Specifically, the voltage of phase A, denoted V'_A, after the fault is equal to the voltage from the second module (11). Although the phase voltage is slightly imbalanced, the impact on overall system performance is limited due to the fault-tolerant strategy, which is discussed further in Section 4.

$$V_A = V_{HB1} + V_{HB2}, \quad V'_A = V_{HB2} \tag{11}$$

The inverter utilizes level-shifted pulse width modulation (LSPWM) for controlling the switches, which offers several benefits, particularly in multi-level converters. In this method, the carrier signals are amplitude-shifted, leading to lower power losses [38]. This makes LSPWM a suitable and efficient technique for controlling multi-level converters, as it simplifies the control process while effectively balancing the capacitor voltages across the H-bridge cells. In a five-level cascaded H-bridge inverter (CHB), the LSPWM method uses four carrier signals to cover the amplitude of the main reference wave. Each carrier has an amplitude offset of 0.5, ranging from -1 to 1. By comparing the reference waveform with

these carrier signals, the switching signals are generated to control the two CHB modules in each of the six phases. This approach ensures that the voltage levels are modulated correctly, allowing for effective voltage control and minimizing switching losses, which is crucial for the efficiency of multi-level inverters. Overall, LSPWM is advantageous in this context due to its simplicity, its effectiveness in balancing the capacitor voltages, and its ability to reduce switching losses, all of which contribute to the overall efficiency and reliability of the inverter system.

4. VSD Fault-Tolerant Control Strategy

Although the application of the multi-phase PMSM, CHB MCIs and improved modulation techniques such as LSPWM provide better fault-tolerant performance, applying a fault-tolerant control strategy ensures operation in critical maintenance projects, which need high-reliability power conversion systems such as offshore renewable energy units. The common open-circuit and short-circuit faults in power modules mostly lead to system failure, reduced performance, and increased maintenance costs. To overcome such challenges, a Vector Space Decomposition (VSD) fault-tolerant strategy is developed to identify, isolate, and compensate for the fault in critical systems. In standard vector control, to avoid the nonlinear effect of rotor position on the flux during the control of the phase and the amplitude of the stator current, the stator phase currents are transferred to a synchronous rotating frame [48]. Vector Space Decomposition uses Clarke and Park transformation for a six-phase PMSM to decouple the six-phase currents into six orthogonal subspaces including, d, q, x, y, z_1 and z_2, through the C_6 transformation matrix (13), which is derived from the Clarke transformation adjusted for a six-phase machine with 60° displacement between the windings and the coordination of the rotating frame, as shown in Figure 4. The dq subspaces participate in the production of flux and torque, while xy subspaces contain harmonic components. Zero sequences, which, in symmetrical operation, are normally 0, should be controlled when a fault happens to avoid imbalance [15,40]. The $\alpha\beta$ subspace components can be calculated through the transformation in (12):

$$\begin{bmatrix} u\alpha & u\beta & ux & uy & uz1 & uz2 \end{bmatrix}^T = \frac{1}{3} C_6 \cdot \begin{bmatrix} uA & uD & uB & uE & uC & uF \end{bmatrix}^T \quad (12)$$

where the matrix C_6 is defined in (13) [49,50]:

$$C_6 = \begin{bmatrix} \cos 0 & \cos\frac{\pi}{3} & \cos\frac{2\pi}{3} & \cos\pi & \cos\frac{4\pi}{3} & \cos\frac{5\pi}{3} \\ \sin 0 & \sin\frac{\pi}{3} & \sin\frac{2\pi}{3} & \sin\pi & \sin\frac{4\pi}{3} & \sin\frac{5\pi}{3} \\ \cos 0 & \cos\frac{2\pi}{3} & \cos\frac{4\pi}{3} & \cos 0 & \cos\frac{2\pi}{3} & \cos\frac{4\pi}{3} \\ \sin 0 & \sin\frac{2\pi}{3} & \sin\frac{4\pi}{3} & \sin 0 & \sin\frac{2\pi}{3} & \sin\frac{4\pi}{3} \\ \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \\ \frac{\sqrt{2}}{2} & \frac{-\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{-\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{-\sqrt{2}}{2} \end{bmatrix} = \begin{bmatrix} 1 & \frac{1}{2} & \frac{-1}{2} & -1 & \frac{-1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & 0 & \frac{-\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \\ 1 & \frac{-1}{2} & \frac{-1}{2} & 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} & 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \\ \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \\ \frac{\sqrt{2}}{2} & \frac{-\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{-\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{-\sqrt{2}}{2} \end{bmatrix} \quad (13)$$

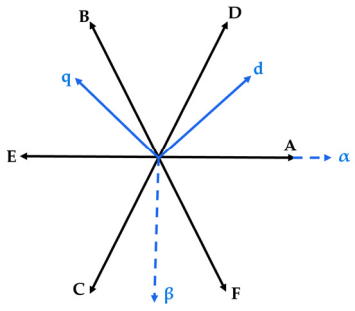


Figure 4. Coordinate of six-phase (A–F) PMSM in rotating frame.

This transformation matrix decouples the six-phase currents uA, uB, uC, uD, uE and uF into orthogonal subspaces. A main feature of this approach is the ability to decouple harmonic components in the x-y subspaces, which improves their control. Moreover, it provides the possibility for fault detection and fault compensation, especially in open-circuit or short-circuit situations for z_1 and z_2 subspaces by the dedication of PI controllers and direct control of these subspaces. However, the dq components are defined based on Park transformation (14), as follows, and the rotation frame coordinate is depicted in Figure 4. When an open-circuit or a short-circuit fault happens in the system, the fault-tolerant strategy is used to suppress the harmonics and balance power flow by controlling the decoupled subspaces and isolating the zero sequence currents, thus preventing the fault-induced currents from affecting the torque production in the d-q subspaces [37]. This approach decreases the adverse effects of faults and adjusts the control system for operating with the remaining healthy phases. By decoupling and controlling each subspace independently through VSD, and in combination with the bypass method for the faulty switches in the inverter, the strategy provides more robust performance in the presence of open-circuit or short-circuit faults in one or more phases. If a short-circuit happens in one or two phases, the consequences vary from damage to power electronic devices to high torque ripple, power surges, mechanical stress and heat stress, which may damage the electrical machine [23].

$$\begin{bmatrix} ud \\ uq \\ ux \\ uy \\ uz1 \\ uz2 \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 0 \\ -\sin\theta & \cos\theta & 0 \\ 0 & 0 & I_4 \end{bmatrix} \cdot \begin{bmatrix} u\alpha \\ u\beta \\ ux \\ uy \\ uz1 \\ uz2 \end{bmatrix}, \ (\mathrm{I}_4 \text{ is a } 4 \times 4 \text{ identical matrix}) \tag{14}$$

Thus, the measuring sensors should detect the faulty phase and disconnect before damaging any vital part of the system. After a phase disconnects, the control system will use the same strategy of an open-phase fault to compensate for the torque through the remaining phases. The current observers can transfer the fault signal to the control system to disconnect the relevant switch for the faulty phase.

For instance, if a phase failure happens in phase A, the matrix vectors are no longer orthogonal. Thus, we need to reconstruct the matrix in a way that keeps the system balanced. Therefore, the following conditions (15) for the matrix components should be satisfied [49]:

$$\begin{cases} \alpha^T \times \beta = 0 \\ \alpha^T \times x = \beta^T \times x = 0 \\ \alpha^T \times y = \beta^T \times y = x^T \times y = 0 \\ \alpha^T \times z = \beta^T \times z = x^T \times z = y^T \times z = 0 \end{cases} \tag{15}$$

The components of the transformation matrix which are related to the faulty phase would be omitted due to the isolation of the fault. Consequently, the $\alpha\beta$ subspaces would be the first two rows of the matrix. On the other hand, the z subspace should be in balance first ($z = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 \end{bmatrix}$) due to the neutral point. The rest of the subspaces (x and y) should be reconfigured to keep the sequences orthogonal [42]. The subspaces of α, β, x, y and z after the fault are calculated through (16), while the transformation matrix is introduced in (17). By the Park transformation matrix (18), the rotating frames of dq are calculated.

$$\begin{bmatrix} u\alpha & u\beta & ux & uy & uz \end{bmatrix}^T = \frac{1}{3} C_5 \cdot \begin{bmatrix} uD & uB & uE & uC & uF \end{bmatrix}^T \tag{16}$$

$$C_5 = \begin{bmatrix} -0.2333 & 0.1 & 0.2667 & 0.1 & -0.2333 \\ -0.2887 & -0.2887 & 0 & 0.2887 & 0.2887 \\ -0.111 & 0.3333 & -0.4443 & 0.3333 & -0.111 \\ 0.2887 & -0.2887 & 0 & 0.2887 & -0.2887 \\ 0.3333 & 0.3333 & 0.3333 & 0.3333 & 0.3333 \end{bmatrix} \quad (17)$$

$$\begin{bmatrix} ud \\ uq \\ ux \\ uy \\ uz \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 0 \\ -\sin\theta & \cos\theta & 0 \\ 0 & 0 & I_3 \end{bmatrix} \cdot \begin{bmatrix} u\alpha \\ u\beta \\ ux \\ uy \\ uz \end{bmatrix}, \ (\mathrm{I}_3 \text{ is a } 3 \times 3 \text{ identical matrix}) \quad (18)$$

The transformation matrix in cases of the fault occurring in the other phases is calculated with the same method and is discussed in detail in [50]. Figure 5 illustrates the control structure for a six-phase permanent magnet synchronous machine (PMSM) driven by a five-level cascaded H-bridge (CHB) inverter using level-shifted pulse width modulation (LSPWM). The LSPWM technique enables the CHB topology to provide a symmetrical AC voltage from a set of asymmetrical time-variant input DC-source voltages [38]. The control system is designed to regulate the machine's speed and torque while ensuring fault tolerance. The speed of the machine is provided directly by the machine model block within the Simulink environment, while, in the HIL tests, the speed is generated by the HIL model and acquired through an ADC channel of the control board. In this picture, it is possible to recognize different parts, such as (1) the speed Control Loop: The machine's speed is measured and compared to a reference speed.

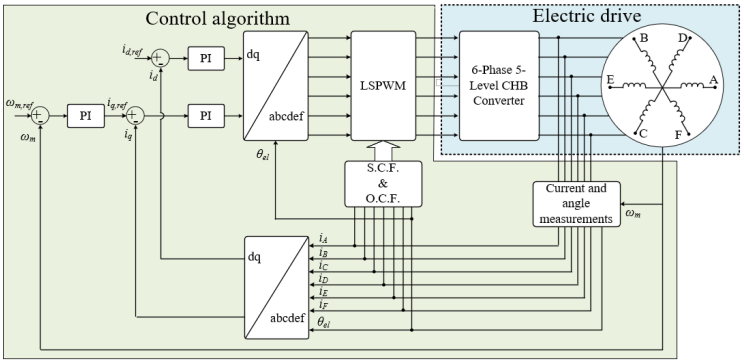


Figure 5. Control structure of the six-phase (A–F) PMSM with a five-level CHB inverter.

The error is processed by a proportional–integral (PI) controller to generate the reference current for the torque-producing component (i_q). Another part is (2) the current Control Loop: the reference currents for the d-axis (i_d) and q-axis (i_q) are regulated by two PI controllers. The id component is set to zero to achieve a high power factor, while the i_q component controls the torque. (3) Fault Tolerance: in the event of a fault, such as an open-circuit or short-circuit fault, the control system adjusts the modulation strategy to maintain balanced operation. The unbalanced subspaces are regulated through additional PI controllers designed to suppress harmonic components. (4) Modulation Strategy: the LSPWM technique is used to control the switches of the CHB inverter. This method reduces switching losses and ensures effective voltage control across the H-bridge cells. LSPWM is the most used technique for the implementation of VSD in a multi-level inverter, while LSPWM disperses the switching of signals onto multi-voltage levels to minimize the harmonic distortion and switching losses, allowing for the precise voltage control that is necessary for effective VSD operation. Additionally, the VSD control strategy outputs are later employed as input references for the LSPWM modulation to produce desired

voltage waveforms, for protection against control stability with respect to system faults. (5) Transformation Blocks: Clarke and Park transformations are applied to decouple the six-phase currents into orthogonal subspaces (d, q, x, y, z_1, z_2). This simplifies the control of the machine and enhances fault tolerance. Overall, Figure 5 demonstrates a robust control strategy that ensures the efficient and reliable operation of the six-phase PMSM, even under fault conditions. During normal operation, xy and zero subspaces are in balance. When a fault happens, the unbalanced subspaces are regulated through three PIs, which are designed to suppress the main harmonic orders [25]. These controllers are used as a solution for the xy and zero sequence subspaces to ensure harmonic components produced after the fault do not contribute to the generation of torque or flux. Indeed, the reference value for these subspaces is considered to be zero. In the fault detection process, the current of every phase is constantly monitored through the current and angle measurement block to check any unusual detection that may indicate open-circuit or short-circuit problems. Current observers of the proposed system measure phase currents and compare them with reference values and thresholds. For open-circuit faults, the current magnitudes in one or more phases are very close to zero, although there is an expected reference current demand; for short-circuit faults, the current spikes well above the safe operating limits. Fault type can also be identified as the magnitude and rate of change on the waveform. Referencing conditions of open-circuit faults are characterized by steadily low currents, flattened waveforms and the absence of harmonics, while short-circuit faults feature rapid current surges and harmonic distortion. Using a threshold-based algorithm, this detection technique samples with high speed to quickly isolate faulty phases, applying compensation behaviors to maintain the stability of the system. As soon as a fault is detected, the control system immediately enables a fault-tolerant operation block (S.F.C and O.C.F), which receives the error signals and modifies the transformation matrix to delete the faulty phase. By using this modified transformation matrix, the five subspaces thus defined remain orthogonal after the failure process, which prevents the non-failed healthy phases from being affected. This transformation matrix allows the system to be adjusted to the new configuration (fault occurrence which leads to isolation of faulty phase and load redistribution on the healthy phases). The PI controllers control the decoupled currents in the subspaces to suppress harmonics and maintain system balance. Then, these regulated currents are passed back through the inverse park transformation to the phase current. The six-phase five-level CHB inverter produces switch control signals from the outputs of the resulting phase currents in the LSPWM block. By dynamically adapting the control strategy to fault conditions and isolating any fault, this approach allows the system to maintain reliable operation and prevent additional damage, even in the event of a failure.

5. Simulation Results

A Simulink/Matlab (version 2023b) model has been implemented to validate the fault-tolerant modulation strategy. Each DC-link voltage source has been set equal to 200 V and the converter's switching frequency is 10 kHz. The power converter is connected to a permanent magnet synchronous machine (PMSM) with the characteristics reported in Table 2. During normal operation, the phase-to-neutral switching voltage at the output of the HB converter shows five voltage levels, as illustrated in Figure 6.

As can be seen from Figure 6, the line-to-line switching voltages exhibit seven voltage levels and the six-phase currents are perfectly sinusoidal waveforms. The THD of the current is close to 1%, and the torque ripple is close to 1 Nm. In this condition, mechanical speed tracking has a reference value equal to 2000 rpm, as illustrated in Figure 7. In the same figure, the dq and $\alpha\beta$ current transformations and the electrical angle (ϑ) are shown. In the following section, the open-circuit and the short-circuit faults are analyzed.

Table 2. Operating parameters of the electrical drive.

PMSM	
Rated phase current [A]	30
Rated torque [Nm]	49.5
PM machine rated speed [rpm]	3000
Number of pole-pairs	10
PM machine-rated phase back ElectroMotive Force (EMF) [V_{rms}]	240
Magnetic flux [Wb]	0.11
PM machine inductance [µH]	420
Operating point of the converter	
DC-bus voltage [V]	400
Switching frequency [kHz]	10
Dead time [µs]	1

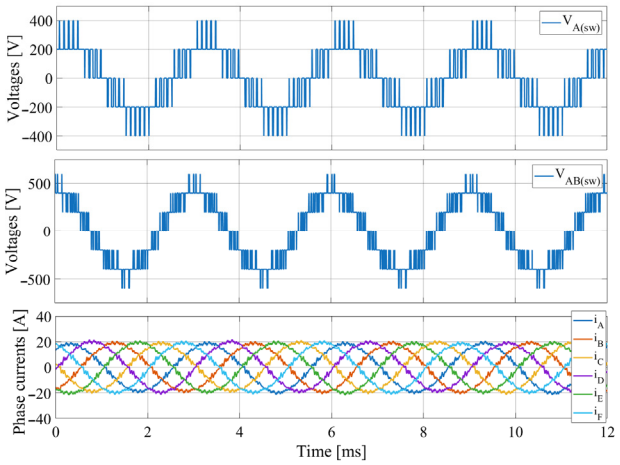


Figure 6. Waveforms at a steady state, from top to bottom: phase-to-neutral switching voltage A, line-to-line switching voltage AB, and six-phase (A–F) currents.

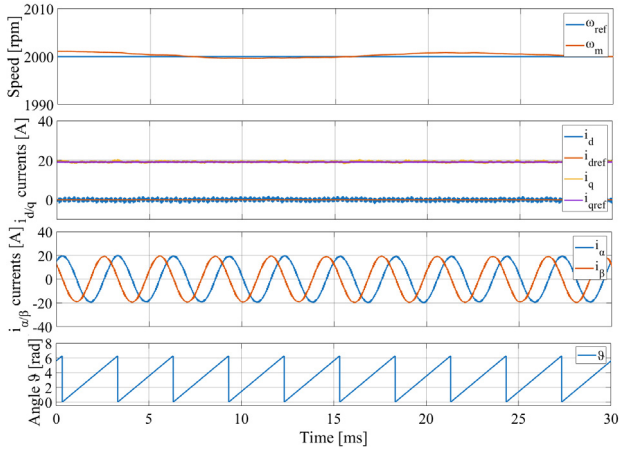


Figure 7. Waveforms at a steady state, from top to bottom: mechanical speed, *id* and *iq* currents, *iα* and *iβ* currents, and electrical angle.

A. Open-circuit faults

In cases of a short-circuit fault in one switch, the converter can work by using only one CHB converter in the faulty phase. Let us assume that the switch S_1 placed in the HB1 is broken in an open-circuit fault, as illustrated in Figure 8.

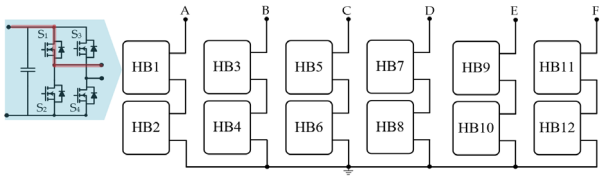


Figure 8. Equivalent circuit of the converter under fault of S_1 in the HB1 in phase A.

In this condition, the switches S_2 and S_4 are always closed and phase A is powered by the HB2. The waveforms at steady state under this fault are shown in Figures 9 and 10. As can be seen, the phase-to-neutral switching voltage of phase A works with three levels and the phase currents are not perfectly symmetrical. However, the mechanical speed of the machine follows its reference, as well as the d-axis and q-axis currents, as can be seen from Figure 10. Similarly, if the fault occurs at switch S_3 (or at switches S_2 or S_4), the control algorithm is able to open the faulty HB and operate with only one HB. Furthermore, the THD of the current is close to 2.1%, the torque ripple is close to 2.8 Nm, and the unbalanced current, calculated with respect to the maximum peak and minimum peak current, is approximately 9.2 A.

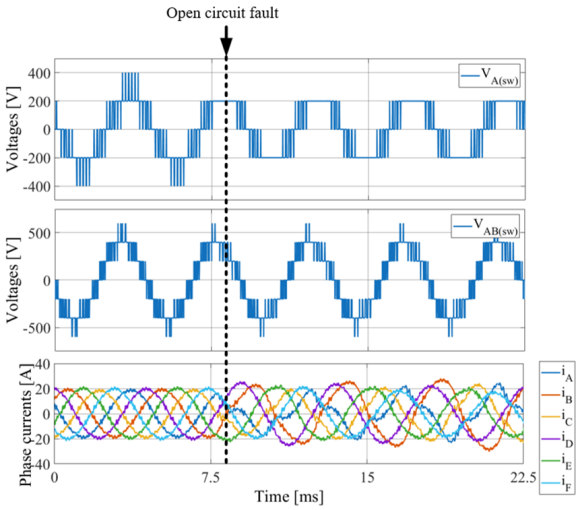


Figure 9. Waveforms at steady state under open-circuit fault of S_1 in HB1, from top to bottom: phase-to-neutral switching voltage A, line-to-line switching voltage AB, and six-phase currents.

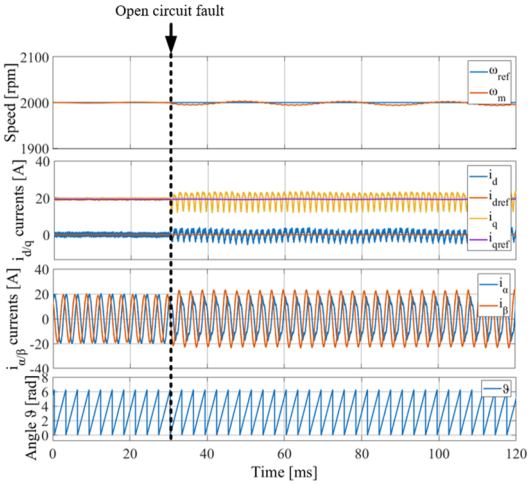


Figure 10. Waveforms at steady state under open-circuit fault of S_1 in the HB1, from top to bottom: mechanical speed, i_d and i_q currents, i_α and i_β currents, and electrical angle.

B. Short-circuit faults

If a short-circuit fault occurs in switch S1 located in HB1, as illustrated in Figure 8, all HBs of the faulty phase are switched off immediately and the algorithm can compensate for the fault, as illustrated in Figure 11. As can be seen, the mechanical speed and i_d-i_q currents follow the reference values, while the six-phase currents are not perfectly shared between the other phases. Figure 11 illustrates the entire dynamic process, starting from the occurrence of the fault to the eventual recovery of the system. The recovery time primarily reflects the comprehensive process managed by the control algorithm, which is designed to ensure the reliable and safe operation of the system. When a short-circuit fault occurs, the algorithm first detects the fault with high precision and isolates the faulty module to prevent any further damage. Following isolation, the system transitions into a compensation phase where power is redistributed among the remaining healthy modules, allowing the system to continue functioning despite the fault.

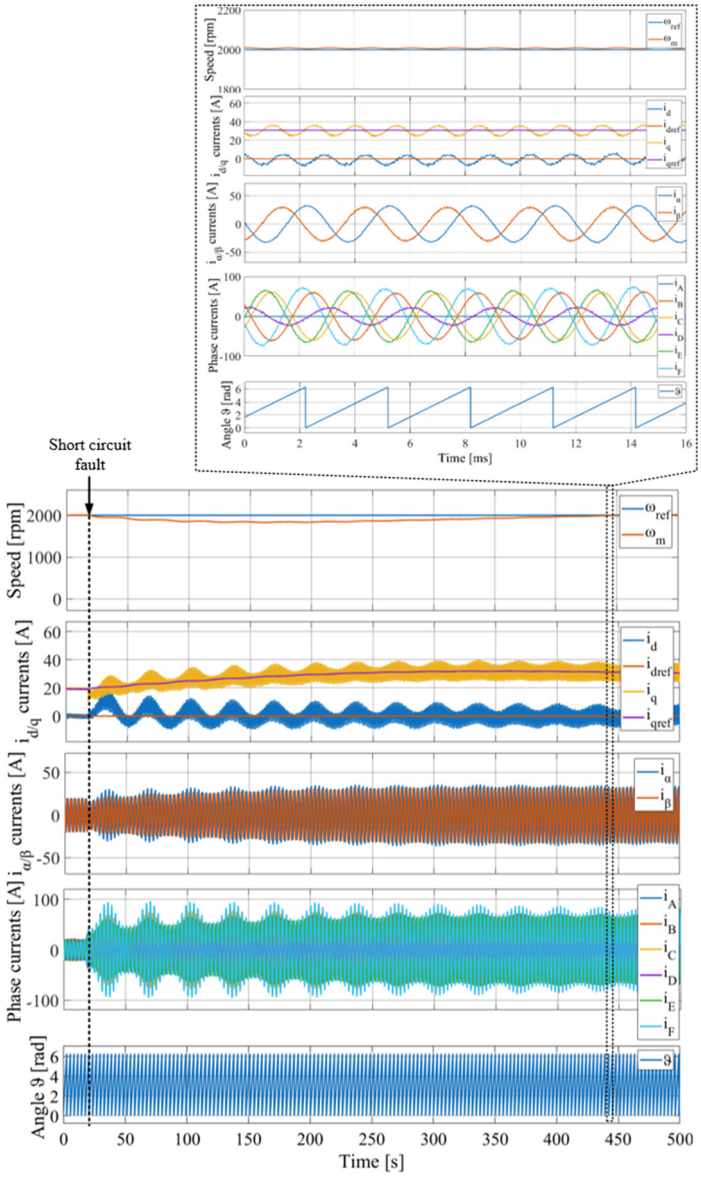


Figure 11. Waveforms at steady state under a short-circuit fault of S_1 in the HB1, from top to bottom: mechanical speed, i_d and i_q currents, i_α and i_β currents, six-phase currents and electrical angle.

When a short-circuit fault occurs, the algorithm first detects the fault with high precision and isolates the faulty module to prevent any further damage. Following isolation, the system transitions into a compensation phase where power is redistributed among the remaining healthy modules, allowing the system to continue functioning despite the fault. In the short-circuit condition, the THD of the current is close to 2.2%, the torque ripple is close to 4.3 Nm, and the unbalance current, calculated with respect to the maximum peak and minimum peak current, is approximately 31 A.

Once the fault is compensated, the control strategy focuses on restoring stability by mitigating transient effects. This ensures that the system can return to its nominal operating conditions without risking instability or performance degradation. This approach highlights the robustness of the control algorithm, which not only detects and isolates the fault but also actively compensates for its effects while maintaining operational integrity. While the recovery process prioritizes reliability and safety, it also showcases the system's ability to handle real-time fault events effectively. The results from both simulation and HIL tests demonstrate strong agreement in terms of the system's fault-tolerant performance under normal and faulty conditions. For instance, the Total Harmonic Distortion (THD) during open-circuit faults was consistent across both methods, with simulation and HIL results showing a value of approximately 2.1%. Similarly, under short-circuit faults, both approaches yielded a THD of 2.3%. Torque ripple and speed tracking also aligned closely, confirming the reliability of the simulation models and their applicability to real-world scenarios.

However, minor discrepancies were observed in some dynamic responses, particularly during transient recovery periods or in small overshoots of torque ripple. These differences can be explained by the inherent limitations of the HIL setup, such as lower resolution and sampling rates compared to the idealized conditions in simulations. Real-world factors like non-ideal switching characteristics, sensor noise, and communication delays further contribute to these deviations.

6. HIL Experimental Results

Hardware-in-the-Loop (HIL) tests are conducted to evaluate the system's real-time performance under practical operating conditions. Figure 12 illustrates the HIL test bench implemented for the six-phase PMSM supplied by a five-level CHB converter. As shown, the physical system is emulated using the HIL OPAL-RT OP4610XG, which is connected to the control board, known as the PED-board, via an adapter board. The PED-board is a control board based on the National Instruments sbRIO-9651 System on Module (SoM) integrated into the circuit. This SoM features a dual-core microprocessor (µP) and a Field-Programmable Gate Array (FPGA). Consequently, the software for the entire system is implemented in real time (RT) and FPGA, leveraging the LabVIEW graphical environment.

The main function of the adapter board is to acquire electrical parameters from the HIL and transmit them to the control board. Additionally, the adapter board provides signal conditioning for the acquired parameters, auxiliary isolated power supplies, and control signals for the power switches modeled within the HIL system. Figures 13 and 14 present the steady-state waveforms under the operating conditions listed in Table 2. The THD of the current is equal to 1.1%, and the torque ripple is close to 1 Nm.

As observed, the six-phase currents are perfectly sinusoidal, and the phase-to-neutral switching voltage of phase A, $V_{AN(sw)}$, exhibits five voltage levels. Additionally, Figure 15a illustrates the sinusoidal nature of the three-phase currents (i_A, i_B, i_C) under steady-state conditions, indicating effective current control and balanced operation of the six-phase PMSM. The mechanical speed (ω_m) closely follows the reference value, demonstrating the system's ability to maintain accurate speed regulation. The electrical angle (ϑ) maintains a

consistent phase relationship, which is critical for synchronized motor operation. Figure 15b shows the d-axis current (i_d) remains at zero, aligning with the objective of achieving a high power factor by decoupling the torque-producing (i_q) component from the flux-producing (i_d) component. The q-axis current (i_q) accurately tracks the reference signal, confirming the efficacy of the Vector Space Decomposition (VSD) control strategy in regulating torque.

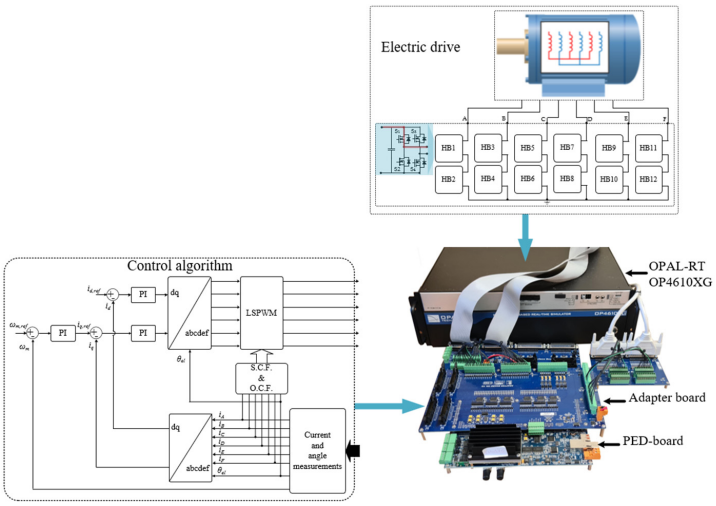


Figure 12. HIL test bench for the six-phase PMSM supplied by a 5-level CHB converter.

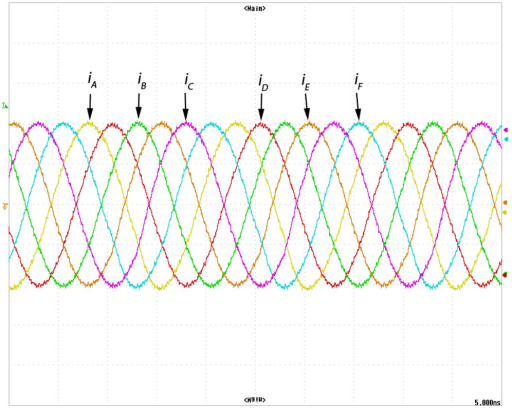


Figure 13. Six-phase currents waveform at steady state: i_A (yellow line), i_B (green line), i_C (magenta line), i_D (red line), i_E (orange line) and i_F (cyan line); 10 A/div, 1 ms/div.

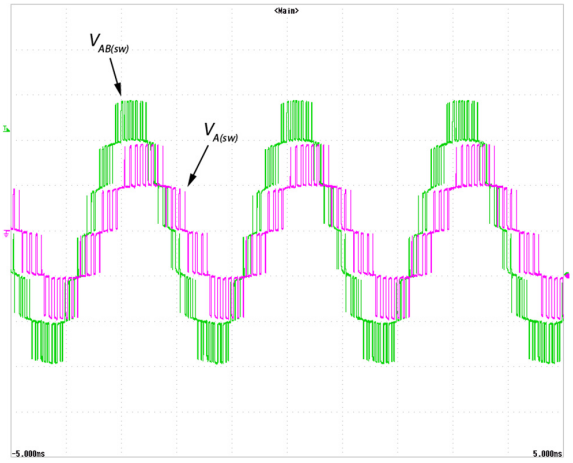
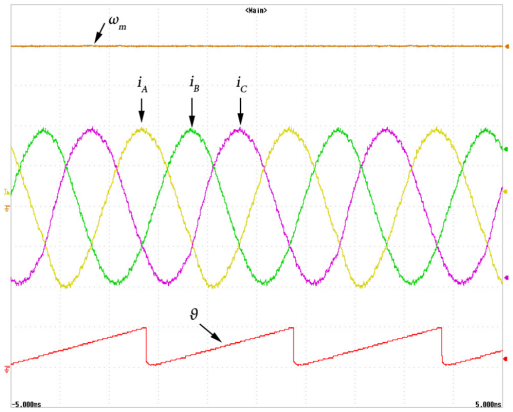
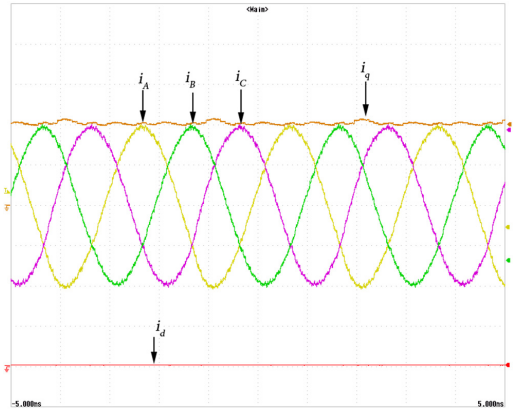


Figure 14. Voltage waveform at steady state: phase-to-neutral switching voltages $V_{AN(sw)}$ *(magenta line)* and line-to-line switching voltage $V_{AB(sw)}$ (green trace). 200 V/div, 1 ms/div.



(**a**)



(**b**)

Figure 15. Three-phase currents waveform at steady state: i_A (yellow line), i_B (green line) and i_C (magenta line) 10 A/div. (**a**) Mechanical speed ω_m (orange line) 500 rpm/div and electrical angle ϑ (red line) 5 rad/div; (**b**) d-axis i_d (red line) and q-axis current i_q (orange line) 10 A/div; and 1 ms/div.

When an open-circuit (OC) fault occurs in phase A, the six-phase currents display an asymmetrical distribution, and the phase-to-neutral switching voltage, $V_{AN(sw)}$, reduces to three voltage levels, as illustrated in Figures 16 and 17. Consequently, the line-to-line switching voltage, $V_{AB(sw)}$, retains five voltage levels. Despite the faulty condition, the system maintains its ability to track the reference speed signals accurately. Additionally, the THD of the current is equal to 2.1%, the torque ripple is 2.8 Nm, and the unbalanced current, calculated with respect to the maximum peak and minimum peak current, is approximately 10 A.

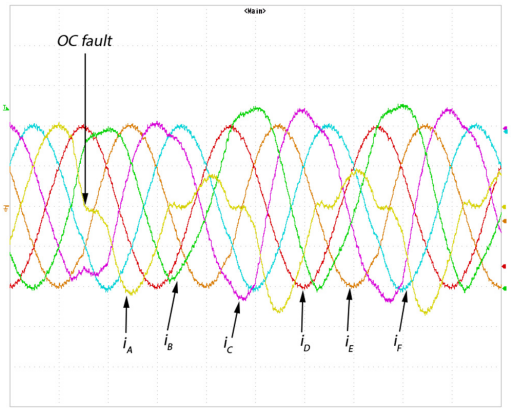


Figure 16. Six-phase current waveforms under OC fault: i_A (yellow line), i_B (green line), i_C (magenta line), i_D (red line), i_E (orange line) and i_F (cyan line); 10 A/div, 1 ms/div.

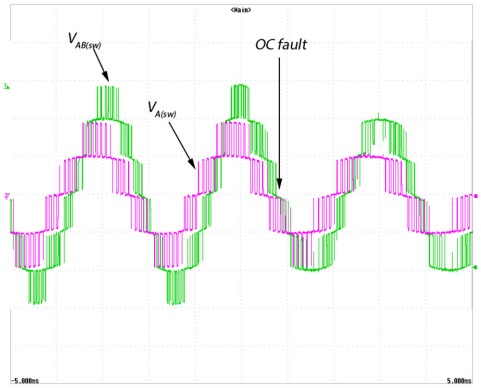


Figure 17. Voltage waveforms under OC fault: phase-to-neutral switching voltages $V_{AN(sw)}$ (magenta line) and line-to-line switching voltage $V_{AB(sw)}$ (green trace). 200 V/div, 1 ms/div.

Figure 18 showcases the steady-state waveforms during a short-circuit (SC) fault in phase A. It includes the three-phase currents (i_A, i_B, i_C), mechanical speed (ω_m) and q-axis current (i_q). The currents are scaled at 10 A/div, the mechanical speed at 500 rpm/div, and the time scale of the waveform at 1 ms/div. Under the short-circuit fault condition depicted in Figure 18, phase A experiences a significant disturbance, yet the system demonstrates remarkable resilience. The three-phase current waveform for i_A deviates from its sinusoidal shape due to the fault, while i_B and i_C exhibit compensatory behavior to mitigate the impact. Despite the asymmetry introduced by the fault, the mechanical speed (ω_m) continues to track the reference value with minimal deviation, highlighting the system's ability to maintain operational stability. The q-axis current (i_q) remains closely aligned with its reference signal, indicating that the torque regulation is effectively preserved, even in the presence of a fault. This performance underscores the effectiveness of the fault-tolerant VSD control strategy in isolating and compensating for faults, ensuring continuous and reliable motor operation. The ability to sustain accurate speed and torque control under fault conditions validates the proposed control methodology's robustness and reliability. Figure 19 shows the six-phase current during an SC fault occurring in phase A. Observing the figure, it can be seen that when the fault occurs, the control algorithm immediately compensates for it, maintaining the current in a sinusoidal shape. Even in this case, the machine's speed successfully tracks its reference signals. Finally, Figure 20 displays the steady-state waveforms during a short-circuit (SC) fault condition. It includes the three-phase currents (i_A, i_B, i_C), the mechanical speed (ω_m), and the q-axis current (i_q). The waveforms are scaled at 10 A/div for the currents, 500 rpm/div for the mechanical speed, and 1 ms/div for time.

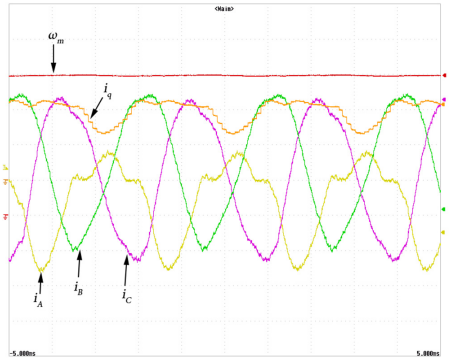


Figure 18. Waveforms at a steady state under OC fault: three-phase currents i_A (yellow line), i_B (green line), i_C (magenta line), mechanical speed ω_m (red line) and q-axis current i_q (orange line); 10 A/div, 500 rpm/div, 1 ms/div.

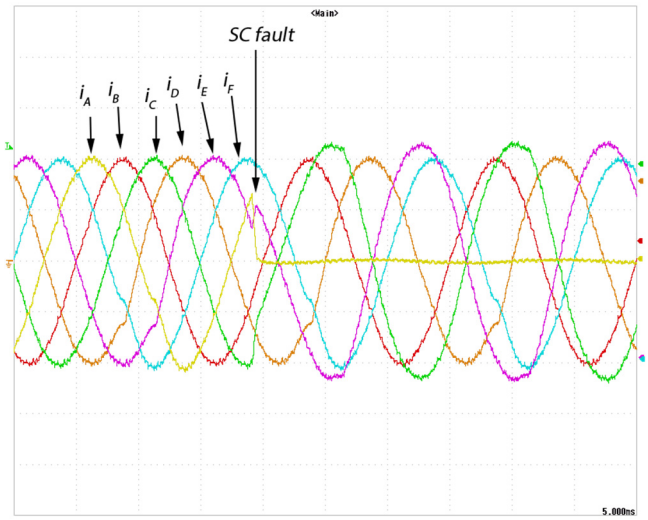


Figure 19. Six-phase current waveforms under SC fault: i_A (yellow line), i_B (green line), i_C (magenta line), i_D (red line), i_E (orange line) and i_F (cyan line); 10 A/div, 1 ms/div.

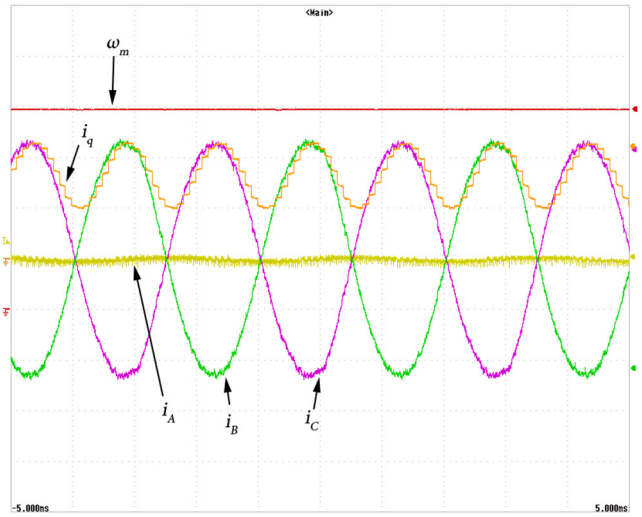


Figure 20. Waveforms at a steady state under SC fault: three-phase currents i_A (yellow line), i_B (green line), i_C (magenta line), mechanical speed ω_m (red line) and q-axis current i_q (orange line); 10 A/div, 500 rpm/div, 1 ms/div.

Under the short-circuit fault condition depicted in Figure 20, the three-phase current waveforms demonstrate asymmetry, with i_A showing a significant deviation from its sinusoidal shape due to the fault. The other phases, i_B and i_C, adjust accordingly to compensate for the fault, showcasing the system's fault-tolerant capabilities. In the short-circuit condition, the THD of the current is close to 2.3%, the torque ripple is close to 4.5 Nm, and the unbalance current, calculated with respect to the maximum peak and minimum peak current, is approximately 32 A.

Despite the disruption caused by the SC fault, the mechanical speed (ω_m) remains closely aligned with its reference value, indicating that the fault-tolerant control strategy effectively mitigates the impact of the fault on system performance. Similarly, the q-axis current (i_q), which governs torque production, continues to track its reference signal, ensuring stable torque control even under fault conditions. These results emphasize the robustness of the proposed control algorithm in detecting and compensating for short-circuit faults. The ability to sustain operational stability, maintain sinusoidal waveforms in

unaffected phases, and regulate speed and torque highlights the efficacy of the implemented fault-tolerant strategy.

7. Conclusions

The proposed system, comprising a six-phase permanent magnet synchronous machine (PMSM) paired with a five-level cascaded H-bridge (CHB) inverter, represents an advanced solution for enhancing reliability in energy conversion systems, particularly in offshore renewable energy units and electric vehicles. The integration of level-shifted pulse width modulation (LSPWM) with a modified Vector Space Decomposition (VSD) control strategy has been shown to improve fault-tolerant performance under both open-circuit and short-circuit fault conditions. The simulation results and Hardware-in-the-Loop (HIL) experiments demonstrated that the system maintains stable operation with sinusoidal current waveforms and accurate speed regulation, even during fault events. For instance, under normal conditions, the Total Harmonic Distortion (THD) of the current is approximately 1%, while the torque ripple is around 1 Nm. During an open-circuit fault, the THD increases to 2.1% and the torque ripple rises to 2.8 Nm, but the system effectively compensates for the fault and maintains operational stability. In the case of a short-circuit fault, the THD reaches 2.3% and the torque ripple is close to 4.5 Nm, yet the control strategy ensures continued speed tracking and torque production.

Despite its advantages, the proposed system has certain limitations that warrant further investigation. Firstly, the computational complexity of the fault-tolerant control algorithm may limit its real-time applicability in resource-constrained environments. Additionally, the transition from a five-level to a two-level topology under severe fault conditions introduces increased voltage stress on the remaining components, potentially impacting long-term reliability. The asymmetrical distribution of currents during fault events also highlights the need for further optimization in the compensation strategy.

Future research should focus on reducing the computational overhead of the fault-tolerant control algorithms, potentially leveraging advanced hardware architectures such as FPGA-based acceleration. Additionally, exploring more efficient methods for managing voltage stress and improving current balancing under fault conditions could enhance system robustness. Finally, experimental validation under more diverse operating scenarios, including multi-fault conditions and variable load profiles, would provide further insights into the scalability and practicality of the proposed system.

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