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Article

Design of a Control Scheme for Distribution Static Synchronous Compensators with Power-Quality Improvement Capability

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Abstract: Electric power systems are among the greatest achievements of the last century. Today, important issues, such as an ever-increasing demand, the flexible and reliable integration of distributed generation or a growth in disturbing loads, must be borne in mind. In this context, smart grids play a key role, allowing better efficiency of power systems. Power electronics provides solutions to the aforementioned matters, since it allows various energy sources to be integrated into smart grids. Nevertheless, the design of the various control schemes that are necessary for the correct operation of the power-electronic interface is a very important issue that must always be taken into consideration. This paper deals with the design of the control system of a distribution static synchronous compensator (DSTATCOM) based on flying-capacitor multilevel converters. The control system is tailored to compensate for both voltage sags by means of reactive-power injection and voltage imbalances caused by unbalanced loads. The design of the overall control is carried out by using the root-locus and frequency-response techniques, improving both the transient response and the steady-state error of the closed-loop system. Simulation results obtained using PSCAD™/EMTDC™ (Manitoba Hydro International Ltd., Commerce Drive, Winnipeg, MB, Canada) show the resultant voltage regulation.

Keywords: power quality; voltage sag; smart grid; distribution static synchronous compensator (DSTATCOM); flying-capacitor multilevel converter

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1. Introduction

Over the past century, electric power systems have been based on the paradigm of large power generation. Nevertheless, this paradigm has become obsolete, due to the depletion of conventional fuel supplies, such as oil and coal, the increase of demand, the availability of competitive distributed energy sources integrated into the grid and environmental issues [1]. Microgrids and smart grids are the alternatives that contribute toward achieving the emerging potential of distributed generation and to obtain more reliable power systems [2].

Microgrids can operate in an interconnected mode or in an islanded mode, and require power-electronic converters, due to the nature of most of the distributed energy sources [3]. On the other hand, a smart grid must integrate advanced sensing technologies, control methods and communications into the electricity grid. The smart grid is expected to exhibit the following key characteristics: self-healing, consumer friendly, attack resistant, power quality improvement, capability to accommodate all generation and storage options, optimal asset for markets and efficient operation [1].

The key technologies involved in smart grids include integrated communications across the grid, advanced control schemes, sensing, metering and measuring, advanced grid components and decision support and human interfaces. Among these technologies, the evolution of the advanced grid components is one of the most relevant issues, such as the next generation of power system devices, which include flexible AC transmission system (FACTS) devices [4].

Static synchronous compensators (STATCOM) and distribution static synchronous compensators (DSTATCOM) are two FACTS devices based on a voltage-source converter (VSC), which are widely used to improve voltage regulation and harmonic elimination and to balance the grid current [5,6]; they play a key role within the smart grid concept. They can therefore contribute toward enhancing power quality and obtaining a more reliable electricity grid.

Although there are many aspects involved in the design and operation of STATCOM and DSTACOM devices, this paper focuses on two particular issues: the VSC topology and the design of the control system.

For low-voltage and low-power applications, STATCOMs and DSTACOMs based on two-level VSCs are normally used. Nevertheless, as the rating of these devices continues to increase in the realm of reactive-power compensation, the power electronic converters are beginning to be higher-voltage points of the grid. In this way, multilevel converter topologies are at present the most popular topologies for high voltage applications: they have been advanced as a means to reduce the voltage stress on the switching devices [7] and to improve on the quality of the waveform with less filtering requirements. A number of multilevel converter topologies have been put forward, although the most popular are: neutral-point-clamped converters (NPC), flying-capacitor converters (FC) and H-bridge converters [8]. All of them have benefits and drawbacks, and various pulse-width modulation (PWM) techniques can be used to draw on the best control characteristics of these converters [9]. Although one of the handicaps of FC converters is the increased number of bulk capacitors with the number of levels, which is larger than in the case of NPC configurations, the control system to balance the voltages of the capacitors is more flexible in the case of the FC topology, due to a higher number of switching combinations than obtained in the case of NPC topologies [10]. The use of FC converters for STATCOM and DSTATCOM applications has previously been reported in the literature: a STATCOM based on an FC VSC topology

is used to compensate for a single-machine infinite bus [11]. The work shows that the FC VSC generates an output voltage with a very low harmonic distortion. The same authors propose a DSTACOM based on an FC VSC in [12]. In this paper, the control of the voltage balancing of the flying capacitors is carried out by using a hysteresis controller, which provides better results than other methods.

Although there are many proposals of control system strategies for the operation of both the STATCOM and the DSTATCOM, one of the most popular is the vector control theory [13,14]. A direct-vector control of a STATCOM is studied in [15]: this proposal uses a control strategy, which employs PI or an integration of PID, fuzzy and adaptive control mechanisms with better results than those obtained with classical vector control theory. A state feedback control system for a DSTATCOM is designed in [16]. The state feedback law employs linear quadratic regulators in order to track the reference state trajectories showing a satisfactory performance of the overall system. Mishra *et al.* [17] propose a dead-beat controller for a DSTATCOM. The results shows that the control system is very effective when compensating for not only balanced voltage sags, but also voltage imbalances. Another interesting control alternative is proposed in [6]: in this case, a control system based on neural network is designed for a DSTATCOM, including reactive power compensation, harmonic elimination and load balancing. Singh and Solanki [18] make a comparison between three different control strategies of a DSTATCOM, namely, the instantaneous reactive power, the synchronous reference frame theory and an Adaline-based control scheme, which uses a least-mean squares algorithm to estimate the current references.

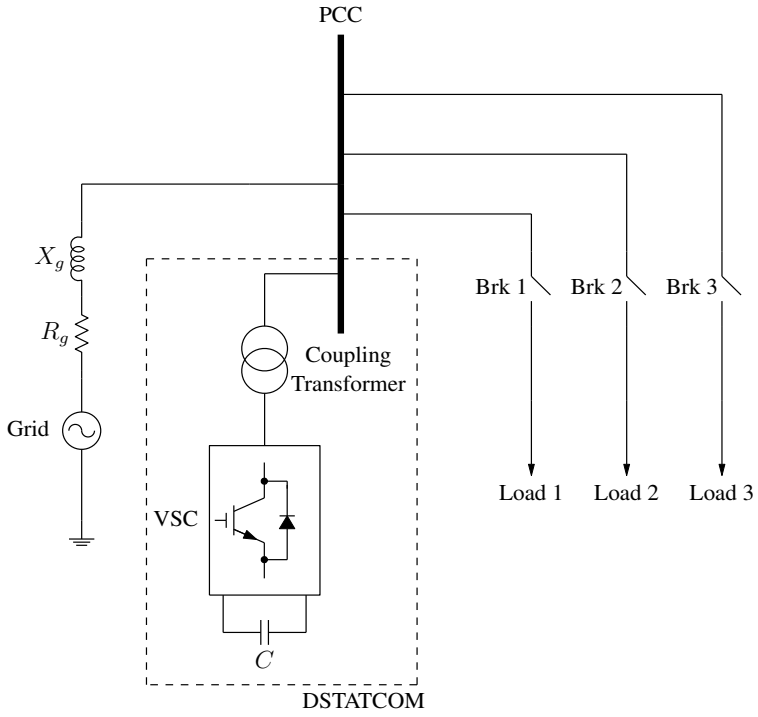
This paper deals with the design of a control system for a DSTATCOM, which employs a five-level flying-capacitor VSC. The DSTATCOM is tailored to inject up to 100 MVAr and is connected to a 13.8 kV distribution grid. The work focuses on the design methodology of the overall control system and uses classical linear control tools, such as the root-locus and frequency-response techniques, in order to tailor the control scheme. The control architecture employs the synchronous reference frame method and implements proportional-integral regulators combined with resonant-type regulators [19]. Unlike other references that design control systems for DSTATCOMs, comprehensive information about the design criteria is provided in this work, such as transient-response specifications, stability margins and the steady-state error. The control system is designed to compensate for both balanced voltage sags and voltage imbalances caused by unbalanced loads or asymmetrical faults. The injection of reactive power ameliorates the voltage sags, while the voltage imbalance compensation is achieved by balancing the grid current.

The paper is organized as follows. The dynamic model of the DSTACOM and the five-level flying-capacitor VSC topology are presented in Section 2. The configuration of the overall control system is explained in Section 3, and the various control subsystems are detailed, which are the voltage in the DC capacitor controller, the controller of the voltage at the coupling point, the control structure for the balancing of the grid current and the control algorithm to maintain the flying capacitor voltages balanced. The design of the various parameters of the control system is studied in Section 4. In addition, simulation results obtained by the implementation of the control system in PSCAD/EMTDC are also presented in this section. The main conclusions of this study are provided in Section 5.

2. Model of the DSTATCOM

The basic configuration of a DSTATCOM is shown in Figure 1: it consists of a VSC, which is connected to the grid by means of a coupling transformer. In this paper, a five-level flying-capacitor VSC is used, while a capacitor, C, is used as a DC energy storage system in the VSC. The grid comprises an AC voltage together with a resistance and a inductive reactance ($R_g - X_g$), which model the impedance of the line. In addition to the DSTATCOM, a number of loads can also be connected to the grid at the point of common coupling (PCC): in the example shown in Figure 1, up to three loads can be connected.

Figure 1. Example of a grid feeding three loads and a distribution static synchronous compensator (DSTATCOM) connected to the point of common coupling (PCC). Brk, Circuit breaker.



The equivalent circuit of the DSTATCOM connected at the PCC is depicted in Figure 2, in which v_s is the grid voltage, v is the voltage at the PCC and R_g and L_g are the resistance and the inductance model line impedance. As the VSC will be operated by a PWM scheme with a high switching frequency, its average model is taken into account [20], and the VSC has therefore been modeled as an ideal voltage source u; while v is the PCC voltage; i is the current injected into the grid by the DSTATCOM; i_g is the current of the grid and i_L is the load current. Finally, the coupling transformer is modeled using the resistance, R, and the inductance, L.

The five-level FC converter configuration is shown in Figure 3: the flying capacitors, C_1, C_2 and C_3, must be charged to $3V_{dc}/4$, $V_{dc}/2$ and $V_{dc}/4$, respectively, for the proper operation of the VSC. Under these conditions, each switch blocks $V_{dc}/4$, *i.e.*, half the voltage of the conventional two-level VSC. An additional advantage of using a multilevel converter topology is the reduction in not only the total harmonic distortion of the voltage, but also the switching losses. A detailed explanation of the main features of the five-level flying-capacitor VSC can be found in [11].

Figure 2. One-line equivalent circuit of the DSTATCOM.

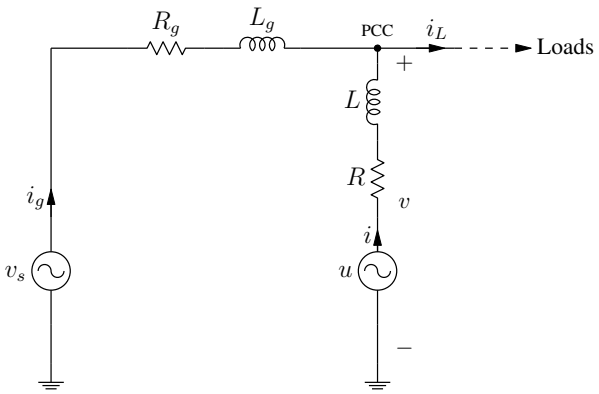
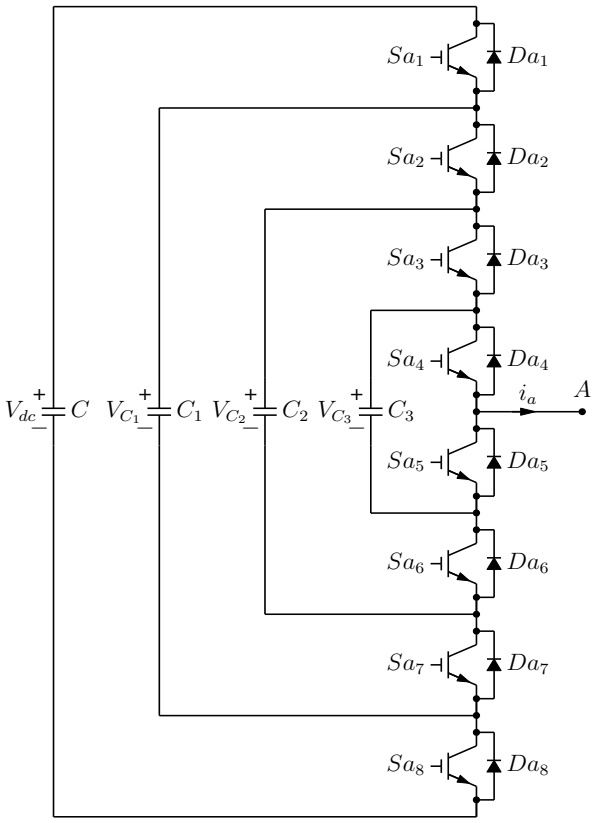


Figure 3. Phase leg of a five-level flying-capacitor converter.



The dynamic equation of the system plotted in Figure 2 can be obtained by employing a rotating reference frame through the use of Park's transformation [21]. In this work, the chosen transformation maintains the power invariant [22], and the synchronous reference frame (SRF) has been used, *i.e.*, the reference frame rotates at the fundamental frequency of the grid voltage, ω_1. Under the assumption that a three-wire VSC is used, the homopolar component of the current, i, will be zero, and the state-variable model of the DSTATCOM in the SRF can be written as [21,23]:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega_1 \\ -\omega_1 & -\frac{R}{L} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L}\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} u_d - v_d \\ u_q \end{bmatrix} \tag{1}$$

where the state variables, i_d and i_q, are the d and q components of the current, i, and u_d and u_q are the d and q components of the output voltage of the VSC, which are also the control inputs of System (1). As the SRF rotates at ω_1, the PCC voltage, v, only contains the d component, v_d. If the system is balanced, all the sinusoidal variables of System (1) contain only a positive sequence and become DC magnitudes in the SRF. Nevertheless, when imbalances exist, the variables will contain both positive and negative: in this situation, the negative sequences will convert into second-harmonic components in the SRF [24,25].

Since the homopolar component of the current, i, is zero, the instantaneous active power, p, and the instantaneous reactive power, q, injected by the VSC at the PCC can be obtained as [26]:

$$p = v_d i_d \tag{2}$$

$$q = -v_d i_q \tag{3}$$

The variables, p and q, are DC magnitudes that can be controlled by i_d and i_q, respectively, if the voltage, v_d, is measured.

It should be noted that System (1) is coupled, and changes in i_d will produce variations in i_q and *vice versa*. This can be avoided by obtaining an equivalent decoupled model through the application of certain mathematical manipulations:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 \\ 0 & -\frac{R}{L} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L}\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} w_d \\ w_q \end{bmatrix} \tag{4}$$

where w_d and w_q are the new control inputs and will be obtained after applying a specific control scheme. The original control inputs, u_d and u_q, can be calculated as:

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = L\begin{bmatrix} 0 & -\omega_1 \\ \omega_1 & 0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} w_d \\ w_q \end{bmatrix} + \begin{bmatrix} v_d \\ 0 \end{bmatrix} \tag{5}$$

Moreover, when considering a lossless VSC, the extracted power of the DC side must be equal to the output power of the VSC:

$$p_C + p_{FC} = \overbrace{u_d i_d + u_q i_q}^{p_{vsc}} \tag{6}$$

where p_{FC} is the power of the flying-capacitors and p_C is the power of the DC capacitor, C, which can be calculated according to the passive sign convention as:

$$p_C = -i_C v_{dc} = -C\frac{dv_{dc}}{dt}v_{dc} = -\frac{1}{2}C\frac{d\left(v_{dc}^2\right)}{dt} \tag{7}$$

The output power of the VSC is equal to the power injected into the grid, p, plus the power losses of the coupling transformer, p_t:

$$p_{vsc} = p + p_t = \overbrace{v_d i_d}^{p} + \overbrace{\underbrace{R\left(i_d^2 + i_q^2\right)}_{p_R} + \underbrace{\frac{L}{2}\left(\frac{d\left(i_d^2\right)}{dt} + \frac{d\left(i_q^2\right)}{dt}\right)}_{p_L}}^{p_t} \tag{8}$$

where p_R stands for the losses in the transformer resistance, which are usually negligible. The term p_L, models the losses in the inductance of the coupling transformer, which are zero in the steady state.

Under the assumption of a current controller designed to obtain a fast transient response in order to reach the steady state as quickly as possible, the term, p_L, can therefore be ignored, which implies that $p_{vsc} \approx p$ [14]. Furthermore, the FC voltages must be controlled in order to remain constant and balanced: if the control scheme of the FC voltages is tailored to obtain a fast transient response, then the power extracted from the DC side can be reduced to the power of the DC capacitor, p_C. If these considerations are borne in mind, Equation (6) can be written as:

$$-\frac{1}{2}C\frac{d\left(v_{dc}^2\right)}{dt} = v_d i_d \tag{9}$$

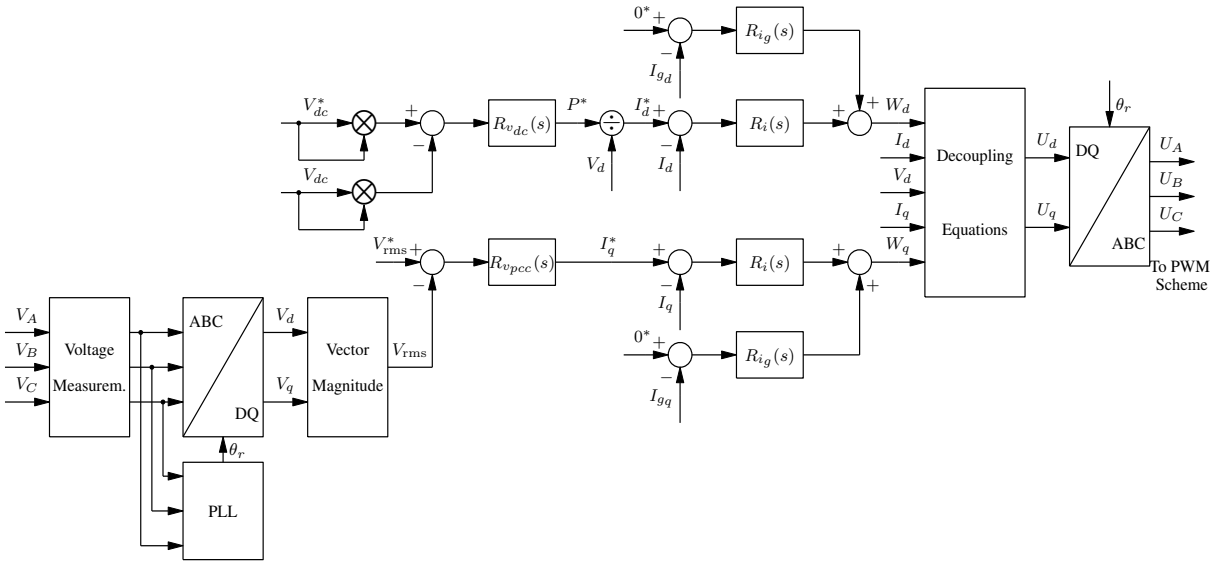
Equation (9) shows that the voltage in the DC capacitor can be controlled by the current, i_d.

3. Control-System Configuration

The main objective of the control system is three-fold: to contribute toward maintaining the grid voltage constant by means of either the injection or absorption of reactive power; to eliminate possible imbalances in the grid current, which can cause voltage imbalances at the PCC, and to control and to keep constant at a sufficient level the voltage in the DC capacitor to a proper operation of the DSTATCOM.

Figure 4 depicts the block diagram of the main control scheme in which all the variables are written in capital letters, since they are expressed in Laplace's domain.

Figure 4. Block diagram of the control system of the DSTATCOM. PLL, phase locked loop.



The superscript asterisk stands for reference values, and the control structure of each axis (*i.e.*, the d and q components) is based on the use of two nested control loops plus a resonant regulator. The overall control system employs a phase locked loop (PLL) in order to obtain the angle, θ_r, which is needed to carry out the variable transformation in the SRF. The inputs of the PLL are the measurements of the grid voltage, which are usually filtered to eliminate measurement noises. The decoupled Equation (5) is used to obtain the outputs, $U_d(s)$ and $U_q(s)$, which are transformed into the three-phase system variables, U_A, U_B and U_C, by means of the inverse Park transformation. These variables are used in a sinusoidal PWM scheme in order to generate the firing signals of the FC converter.

The design of the different regulators is carried out using the decoupled system (4), whose transfer function is:

$$G_{i_x}(s) = \frac{I_x(s)}{W_x(s)} = \frac{1}{Ls + R} \tag{10}$$

where subscript x stands for the d and q axes without distinction.

3.1. Control of the Voltage in the DC Capacitor

The voltage in the DC capacitor is controlled by means of the current, i_d, with a configuration of two nested feedback chains. The inner control loop employs the controller, $R_i(s)$, and is tailored to respond much faster than the outer control loop, which uses the regulator, $R_{v_{dc}}(s)$. As one of the objectives of the overall control system is to achieve zero-tracking error in steady state for step changes in the reference, both regulators use an integral action.

A proportional-integral (PI) regulator is proposed for the control of the current, i_d:

$$Z_d(s) = k_i \frac{I_d^*(s) - I_d(s)}{s} - k_p I_d(s) \tag{11}$$

where the variable, $Z_d(s)$, is the output of the controller, $R_i(s)$, k_i and k_p are the controller gains and $I_d^*(s)$ is the reference current. Another PI controller approach is normally used:

$$Z_d(s) = k_i \frac{I_d^*(s) - I_d(s)}{s} + k_p \left(I_d^*(s) - I_d(s)\right) \tag{12}$$

Nevertheless, Controller (12) yields a zero in the closed-loop transfer function, which results in a worse time response than that obtained with regulator (11).

The controller, $R_{v_{dc}}(s)$, is designed according to System (9), whose transfer function can be written as:

$$G_{v_{dc}}(s) = \frac{Y(s)}{P(s)} = -\frac{2}{Cs} \tag{13}$$

where $P(s) = V_d(s) I_d(s)$ and $Y(s) = V_{dc}^2(s)$.

The proposed control law for the regulator, $R_{v_{dc}}(s)$, of the outer control loop is:

$$P^*(s) = k_{i_{dc}} \frac{Y^*(s) - Y(s)}{s} + k_{p_{dc}} \left(Y^*(s) - Y(s)\right) \tag{14}$$

where $Y^*(s)$ is the set-point, $P^*(s)$ is the control output needed to maintain the capacitor voltage at the reference value and $k_{i_{dc}}$ and $k_{p_{dc}}$ are the gains of $R_{v_{dc}}(s)$. The reference current, $I_d^*(s)$, is then obtained by dividing the control output, $P^*(s)$, by the voltage at the PCC, $V_d(s)$.

An additional feature of controller $R_{v_{dc}}(s)$ is the inclusion of a reset-windup prevention action in order to stop the integration when the controller reaches either the lower or the upper limit [27].

3.2. Control of the Voltage at the PCC

As in the previous control scheme, the control of the PCC voltage also uses a configuration of two nested control loops. In this case, the voltage at the PCC can be modified by controlling the current, i_q (*i.e.*, the DSTATCOM absorbs or injects reactive power).

The inner control loop employs the regulator, $R_i(s)$, with the control law:

$$Z_q(s) = k_i \frac{I_q^*(s) - I_q(s)}{s} - k_p I_q(s) \tag{15}$$

where $I_q^*(s)$ is the reference value of the q component of the current. It should be noted that the parameters of the regulators, $R_i(s)$, are chosen to be identical in both axes.

The controller for the voltage at the PCC, $R_{v_{pcc}}(s)$, generates the reference value, $I_q^*(s)$, and may be designed in a simple integration approach:

$$I_q^*(s) = k_{i_v} \frac{V_{\text{rms}}^*(s) - V_{\text{rms}}(s)}{s} \tag{16}$$

where k_{i_v} is the controller gain; $V_{\text{rms}}^*(s)$ is the PCC voltage reference and $V_{\text{rms}}(s)$ is the RMS measured value of the voltage at the PCC. Since the transformation used in this paper is a power invariant $dq0$ transformation, the RMS values of the variables of the three-phase system equals the magnitude of the resulting vector in the SRF under balanced sinusoidal conditions [22]. Hence, $V_{\text{rms}}(s)$ can be substituted by $V_d(s)$ as $V_q(s) = 0$ in the SRF. The design of the controller, $R_{v_{pcc}}(s)$, must also take into account the dynamic model of the filtering process used in the voltage measurements.

3.3. Control System for Balancing the Grid Current

The previously explained control schemes are able to regulate the voltage at the PCC when operating under balanced conditions (e.g., compensation of balanced voltage sags), as all the variables are transformed into DC quantities in the SRF. The approach in which PI regulators are used therefore provides a satisfactory result. Nevertheless, unbalanced loads and unbalanced short-circuit faults cause current imbalances, which result in voltage imbalances [28]. Under these circumstances, and assuming a three-wire three-phase system, the PCC voltage and the grid current will contain positive and negative sequences, which are transformed in the SRF into a DC component and a second harmonic component, respectively.

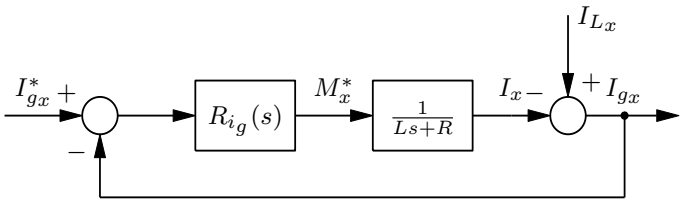
As the internal model principle (IMP) determines that, in order to obtain zero tracking error, a stable closed-loop system must include the generating polynomials of the reference input and the disturbance input in the denominator of the open-loop system [29], PI-type regulators might not be able to deal with the second harmonic component. As an alternative, a resonant-type regulator, which includes the generating polynomial of a sinusoidal input of frequency $2\omega_1$ in its denominator, is therefore proposed.

According to Figure 2, the grid current can be written as $i_g = i_L - i$. The grid current can therefore be modified by controlling the DSTATCOM current, as the simplified scheme in Figure 5 shows. As the control objective is to maintain the grid current balanced, the reference value for the second harmonic component of the grid current is zero ($I_{g_x}^*(s) = 0$). The output of the controller, $R_{i_g}(s)$, is the variable, $M_x^*(s)$, which is obtained with the proposed control law:

$$M_x^*(s) = \overbrace{\underbrace{k\frac{1+Ts}{1+fTs}}_{R_{PL}(s)}\underbrace{\frac{s}{s^2+(2\omega_1)^2}}_{R_R(s)}}^{R_{i_g}(s)} \left(I_{g_x}(s)^* - I_{g_x}(s)\right) \tag{17}$$

where the term, $R_R(s)$, is a resonant controller with resonant frequency $2\omega_1$ (*i.e.*, the second harmonic), according to the IMP, and the term, $R_{PL}(s)$, can be a phase-lead compensation ($f < 1$) or a phase-lag compensation ($f > 1$) and is calculated to achieve a required stability margin (*i.e.*, the phase margin or the gain margin).

Figure 5. Simplified control system for the grid current. Subscript x stands for d and q axes.



The output of the closed-loop control system shown in Figure 5 is:

$$I_{g_x}(s) = \overbrace{\frac{-R_{PL}(s)s}{(Ls+R)\left(s^2+(2\omega_1)^2\right)-R_{PL}(s)s}}^{F(s)} I^*_{g_x}(s) + \overbrace{\frac{(Ls+R)\left(s^2+(2\omega_1)^2\right)}{(Ls+R)\left(s^2+(2\omega_1)^2\right)-R_{PL}(s)s}}^{F_D(s)} I_{L_x}(s) \quad (18)$$

The frequency responses of the transfer functions, $F(s)$ and $F_D(s)$, show that $F(j2\omega_1) = 1$ and $F_D(j2\omega_1) = 0$, respectively. The time response of Equation (18) therefore shows zero tracking error in the steady state for sinusoidal reference signals and sinusoidal disturbances of frequency $2\omega_1$. Moreover, as the term, $R_R(s)$, contains a zero in the origin, the regulator, $R_{i_g}(s)$, exhibits a bandpass behavior, which allows the controller to be used in parallel with the regulator, $R_i(s)$, and with no interaction between them. Both controllers can therefore be designed independently [19,30].

3.4. Phase-Shifted PWM and Flying-Capacitor Voltage Control

Different switching schemes can be used to control the output voltage of an FC multilevel converter: when a high switching frequency is required, one of the most frequently used techniques is that of the phase-shifted SPWM (sinusoidal pulse-width modulation) switching method, since its implementation is simple. For a given number of levels, n, this scheme employs a common sinusoidal modulating signal with frequency f_1, which is compared with a number of triangular carrier signals with frequency f_{sw} equal to $n-1$ [8,31]. These triangular signals are shifted to an angle $\theta = 2\pi/(n-1)$, and the results of these comparisons are used to turn the different converter switches on and off. One of the advantages of this technique is that the output voltage has an equivalent switching frequency of n times the frequency, f_{sw}. This allows the frequency of the carrier signals to be decreased, thus reducing the switching losses [32]. If a three-phase converter is considered, three modulating signals with a shifting phase of $120°$ are required (*i.e.*, one modulating signal per leg).

An additional controller with which to balance the FC voltages is also required in order to cancel out possible voltage imbalances. The cause of these voltage imbalances may be asymmetrical conditions in the converter parameters or differences in the switching of the power devices. The solution implemented in this paper was originally proposed in [33] and consists of using a closed-loop control system that

modifies the modulating signal by adding a square waveform in order to increase or reduce the voltage in the flying capacitors. This square waveform can be written as:

$$v_{sq} = A \text{ sign}(i) D \tag{19}$$

where A is the amplitude of the waveform, v_{sq}; D is a function that indicates that there is a duty cycle decrease ($D = -1$), a duty cycle increase ($D = 1$) or that the duty cycle is not changed ($D = 0$), variable i is the leg current and "sign" is the sign function.

An hysteresis comparator is used to compare the FC voltage with its reference. The output of this comparator is driven by a logic function that calculates the value of D and, therefore, modifies the duty cycle.

4. Case Study

The test system depicted in Figure 1 has been simulated in PSCAD/EMTDC. It comprises a 13.8 kV, 50 Hz, three-phase distribution system. The features of the three loads are the following:

- Load 1 (inductive-resistive load): active power 30 MW and reactive power 18 MVAr.
- Load 2 (inductive-resistive load): active power 70 MW and reactive power 35 MVAr.
- Load 3 (resistive load): active power 7.5 MW.

The loads are connected sequentially by means of circuit breakers. The DSTATCOM is connected to the PCC by means of the secondary side of a three-phase transformer with a winding ratio of 20 kV/75 kV. The transformer's primary and secondary windings are delta and star connected, respectively. The resistance and the leakage inductance of the transformer, referred to the 20 kV, secondary side, are $R = 7$ mΩ and $L = 5$ mH, respectively. The impedance of the grid has been modeled using an inductance $L_g = 2.2$ mH. A 660-μF capacitor is used as the DC energy storage system of the five-level FC VSC plotted in Figure 3, while the value of each flying capacitor is 100 μF. The DC voltage level is set to 120 kV. Ideal IGBT (Insulated-Gate Bipolar Transistor) switches are considered to carry out the simulations. However, taking into account that current IGBT valves can block voltages up to 6.5 kV with switching frequencies in the range of 1 kHz [34], ideal IGBT valves with a maximum blocking voltage of 4 kV are taken into consideration. As the DC voltage is 120 kV, according to Figure 3 each equivalent switch of the five-level FC VSC must block 30 kV, which implies the series connection of eight 4 kV IGBT valves per equivalent switch under the assumption of linearity and symmetry. Since a five-level FC VSC includes eight equivalent switches per leg, as shown in Figure 3, each leg of the converter therefore contains 64 IGBT switches. The switching frequency of each valve is set to $f_{sw} = 1{,}050$ Hz, signifying that the effective switching frequency for the five-level FC VSC is 4,200 Hz (*i.e.*, four times the individual switching frequency, f_{sw}).

4.1. Design of the Control System

The different regulators in the control system have been designed using the root-locus and the frequency-response techniques. The controllers, $R_i(s)$, are designed using System (10) and must be tailored to obtain a faster time response for the inner control loop than the outer control loop. This

signifies that it is not necessary to pay attention to their dynamics when designing the remaining controllers. In order to obtain a fast time response with no overshoot and since the inner control loop contains two poles, the design criterion has been to choose two equal real poles with location $s_1 = s_2 = -1,000$, as shown in Figure 6 in which the closed-loop system poles have been plotted using a square. The resultant gains of controller (11) are $k_i = 5,000$ and $k_p = 9.993$. The time response for a step input in the reference is plotted in Figure 7, which shows that the 1% settling time is lower than 7 ms and that there is no overshoot.

Figure 6. Root locus for the current control, $R_i(s)$.

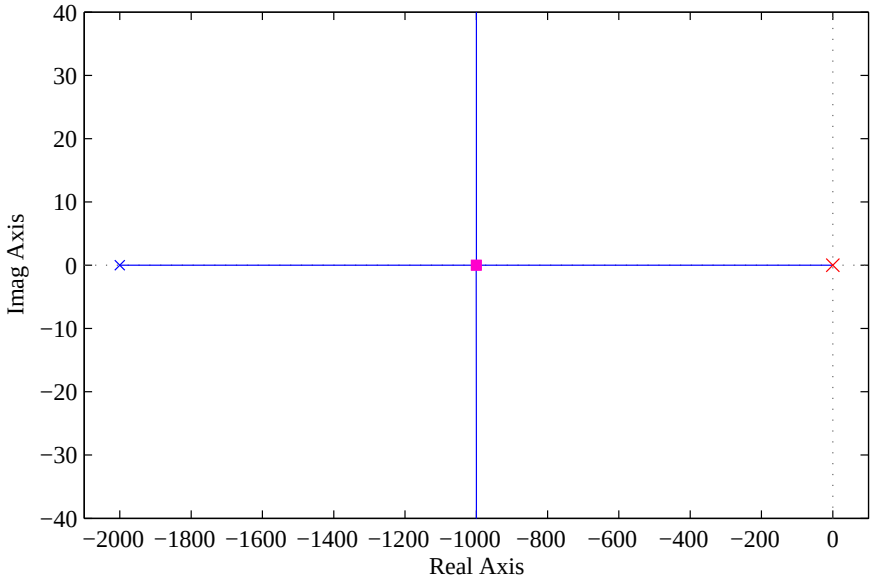
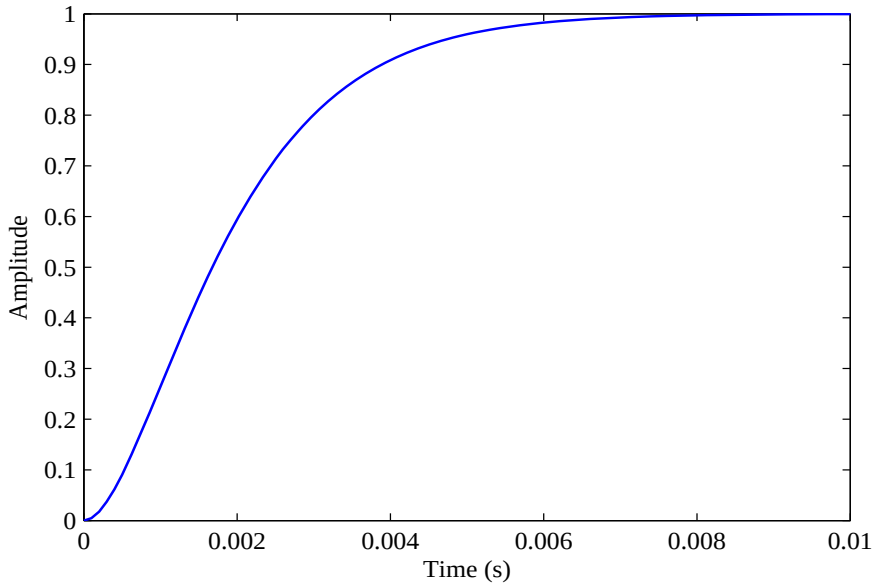


Figure 7. Step response obtained with the current control, $R_i(s)$.



The controller, $R_{v_{dc}}(s)$, must be designed to obtain a time response that is much slower than the inner control loop response. Under this design constrain, the controller gains are calculated by ignoring the dynamics of the inner control loop. In this case study, the desired locations of the poles of the closed-loop

system are $s_1 = -100$ and $s_2 = -20$, which is the dominant pole. The dynamics associated with pole s_1 can therefore be ignored in comparison with that obtained with pole s_2 [35]. Figure 8 shows the pole location of the closed-loop system (*i.e.*, $s_1 = -100$ and $s_2 = -20$) for the voltage control of the DC capacitor. The gains of the controller (14) obtained for this location are $k_{i_{dc}} = -0.6$ and $k_{p_{dc}} = -0.036$. Figure 9 plots the time response for a step change in the reference: in this case, the regulator, $R_{v_{dc}}(s)$, introduces a zero in the transfer function of the closed-loop system, which causes a 9% overshoot, while the 1%-settling time is 160 ms.

Figure 8. Root locus for the control of the DC-capacitor voltage, $R_{v_{dc}}(s)$.

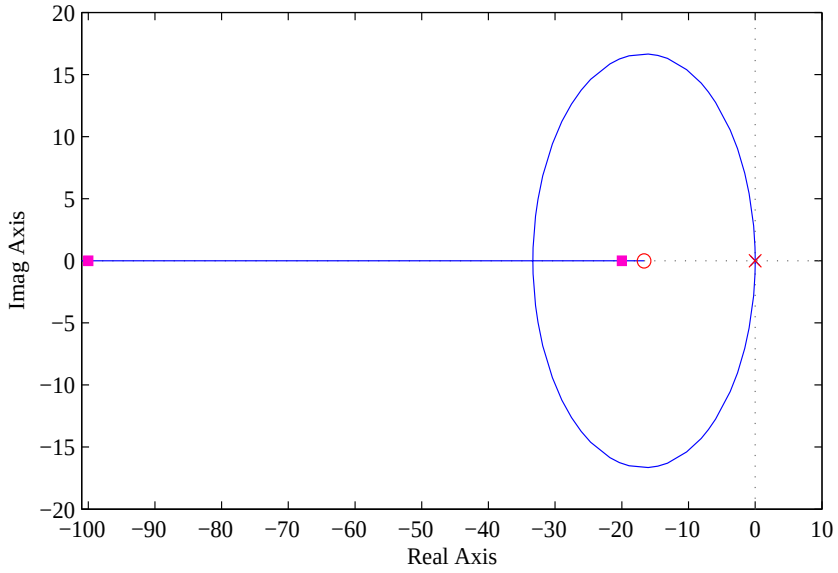
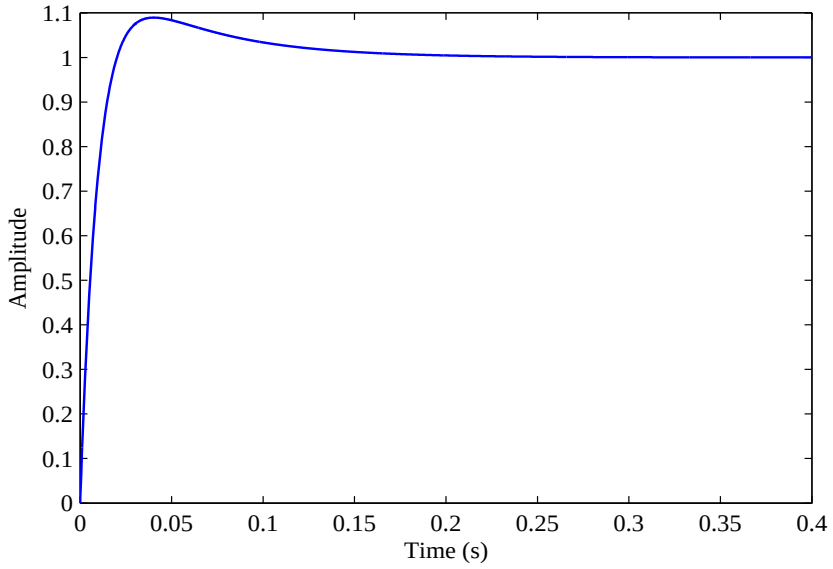


Figure 9. Step response obtained with the control of the DC-capacitor voltage, $R_{v_{dc}}(s)$.



The controller for the PCC voltage has been designed by including a first-order low pass filter in the voltage measurement with transfer function:

$$H_v(s) = \frac{1}{\tau s + 1} \tag{20}$$

where τ is the smoothing time constant and has been set to 10 ms for this example. The design procedure of the controller, $R_{v_{pcc}}(s)$, involves several simulations, and the gain must be chosen carefully, since the Thevenin equivalent system may change at any time depending on the load [17]. For this example, the gain has been set to $k_{i_v} = 100$.

The criteria used to design the regulator, $R_{i_g}(s)$, in order to balance the grid current have been to obtain a phase margin of $60°$, with a crossover gain frequency sufficiently high to obtain a fast time response. Nevertheless, a high value of the crossover gain frequency may cause not only the amplification of unwanted harmonics [30], but also interactions with the current regulators, $R_i(s)$. The crossover gain frequency has therefore been set to $\omega_o = 1.5\omega_2$, where ω_2 is twice the fundamental frequency (*i.e.*, the second harmonic).

The design procedure to obtain the parameters of Regulator (17) is explained in [35] and uses the frequency response of the open loop transfer function. The previously established design specifications yield a phase-lead compensator for the term, R_{PL}(s), of Controller (17), with the following parameters: $k = 793.02$, $T = 2.4 \cdot 10^{-3}$ and $f = 0.05$. Figure 10 shows the Bode diagram of the frequency response obtained with $R_{i_g}(s)$, showing a phase margin of $60°$ at $\omega_o = 1.5\omega_2$, whereas the resulting time response of the closed-loop system when the reference is a sinusoidal input of frequency $2\omega_1$ is plotted in Figure 11a; a perfect tracking is achieved in less than two periods of the input. Moreover, Figure 11b shows the time response of the closed-loop system for a sinusoidal disturbance input of frequency $2\omega_1$; in this case, the control system is also able to reject the disturbance.

Figure 10. Bode diagrams of the frequency response of the open-loop system: (**a**) magnitude and (**b**) phase.

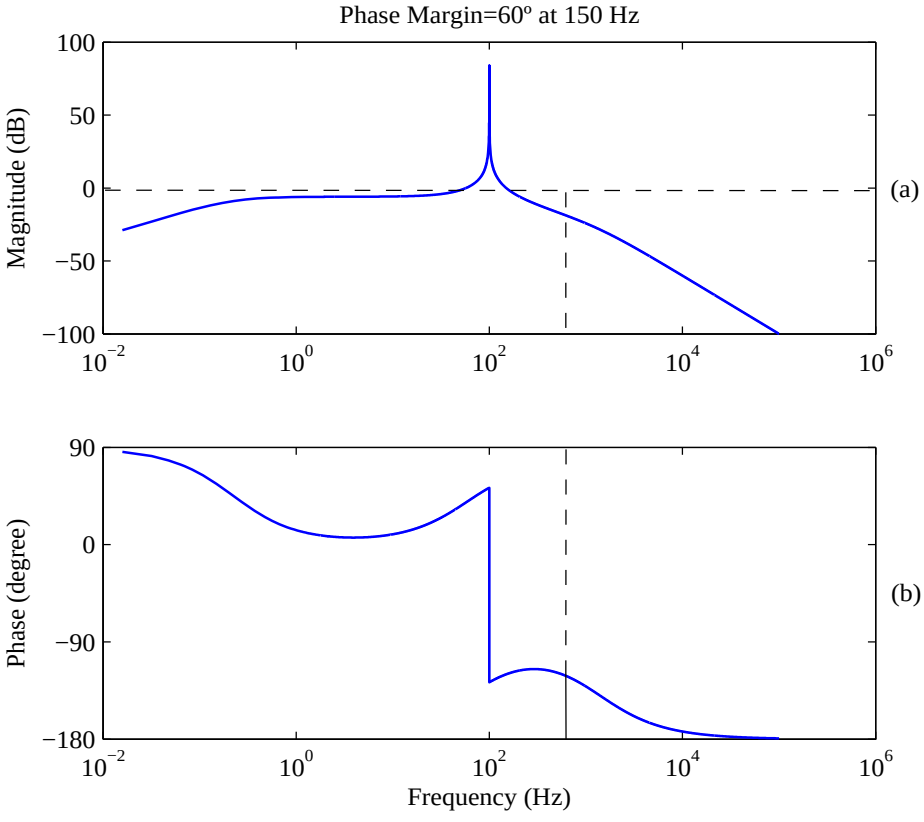
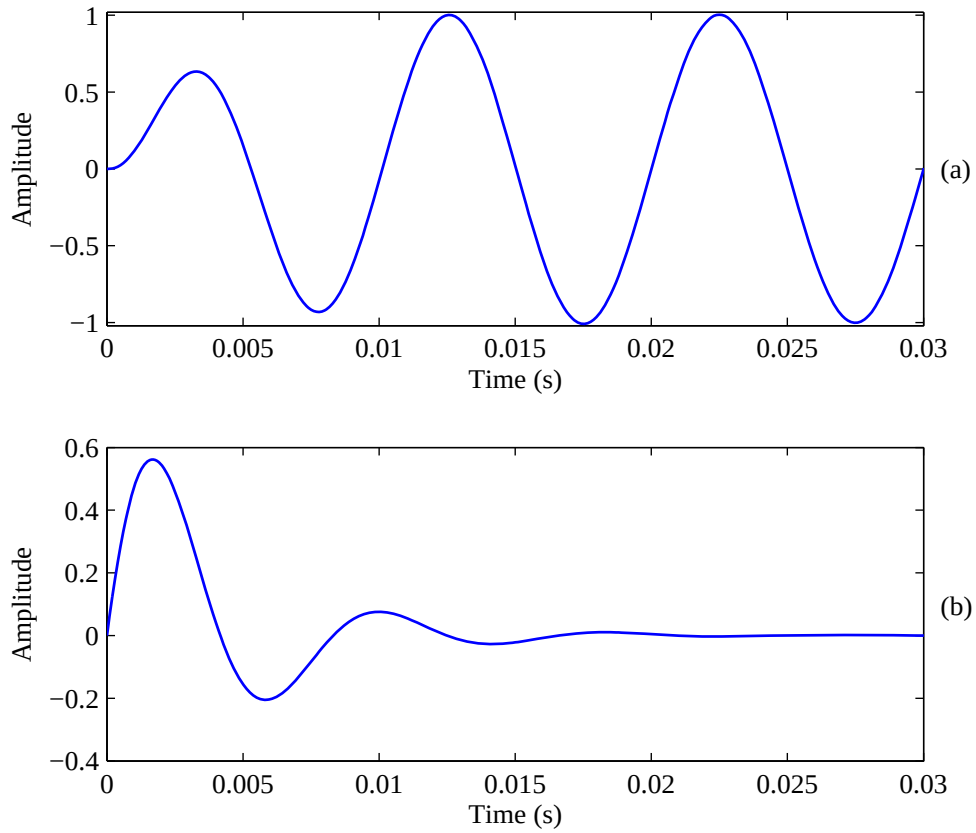


Figure 11. Time response of the closed-loop system for: (**a**) the sinusoidal reference of frequency $2\omega_1$; and (**b**) the sinusoidal disturbance of frequency $2\omega_1$.



4.2. Simulation Results

Having shown the design of the overall control system, details are now provided of a comprehensive simulation case: the DSTATCOM is initially connected to the grid; the control system of the voltage in the DC capacitor, the FC voltage control and the controllers for the currents, i_d and i_q, operate at this time, and the remaining controllers have not yet been connected. Since the DC capacitor is discharged, the control system is responsible for increasing the capacitor charge until the DC voltage level reaches 120 kV, and the flying capacitors are also charged. Load 1 is connected at instant $t = 0.25$ s, causing a balanced voltage sag of 7%. In this situation, the DSTATCOM does not yet compensate for this voltage sag. Load 2 is connected at $t = 0.4$ s and produces a balanced voltage sag of approximately 20%. The PCC voltage control of the DSTATCOM is then connected at $t = 0.5$ s in order to compensate for the voltage sag by means of the reactive-power injection. Load 3 is connected to the PCC at instant $t = 0.8$ s, and a line-to-line short-circuit fault via a 4.2-Ω resistor involving Phases B and C occurs simultaneously at the PCC. The grid current is therefore unbalanced and causes a voltage imbalance at the PCC owing to the voltage drop in the line inductance. It should be stressed that neither the current imbalance nor the voltage imbalance contain a homopolar component, since the short-circuit fault involves only two phases without ground connection. In order to compensate for the imbalance of the current and, therefore, the voltage imbalance, the control system used to balance the grid current is connected at $t = 1$ s. The total simulation time is 1.2 s.

Figure 12 shows the RMS voltage at the PCC: the voltage sags caused by the connections of Load 1 and Load 2 can be clearly seen at instants $t = 0.25$ s and $t = 0.4$ s, respectively. When the DSTATCOM begins to regulate the PCC voltage, the balanced voltage sag is completely canceled out, and the time response of the PCC voltage does not have any overshoot. Nevertheless, when the unbalanced fault occurs at $t = 0.8$ s, the DSTATCOM control system is not able to compensate for the voltage imbalance until the controller used to balance the grid current is connected at $t = 1$ s. During this time interval, the RMS voltage at the PCC contains not only a DC component, but also a second harmonic component. Once the grid-current regulator is connected, the DSTATCOM is able to balance the voltage at the PCC. The three line-to-neutral voltages at the PCC for the interval $0.46 \text{ s} \leq t \leq 0.56$ s are plotted in Figure 13a: it will be observed that all three line-to-neutral voltages have the same amplitude of 11.27 kV when the DSTATCOM has compensated for the balanced voltage sag (*i.e.*, from $t = 0.5$ s). Moreover, the three waveforms contain a very low distortion.

Figure 12. RMS voltage at the PCC.

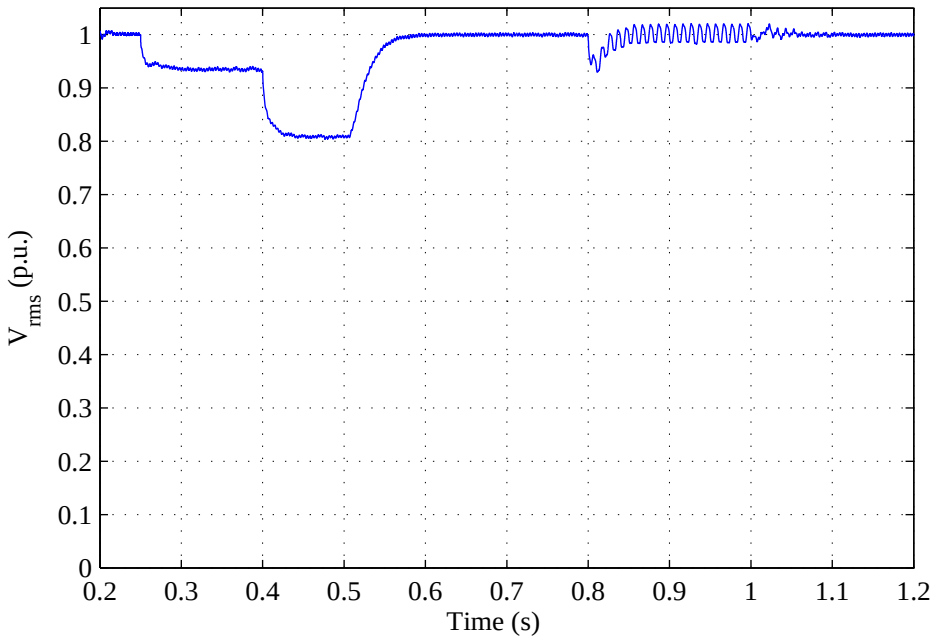
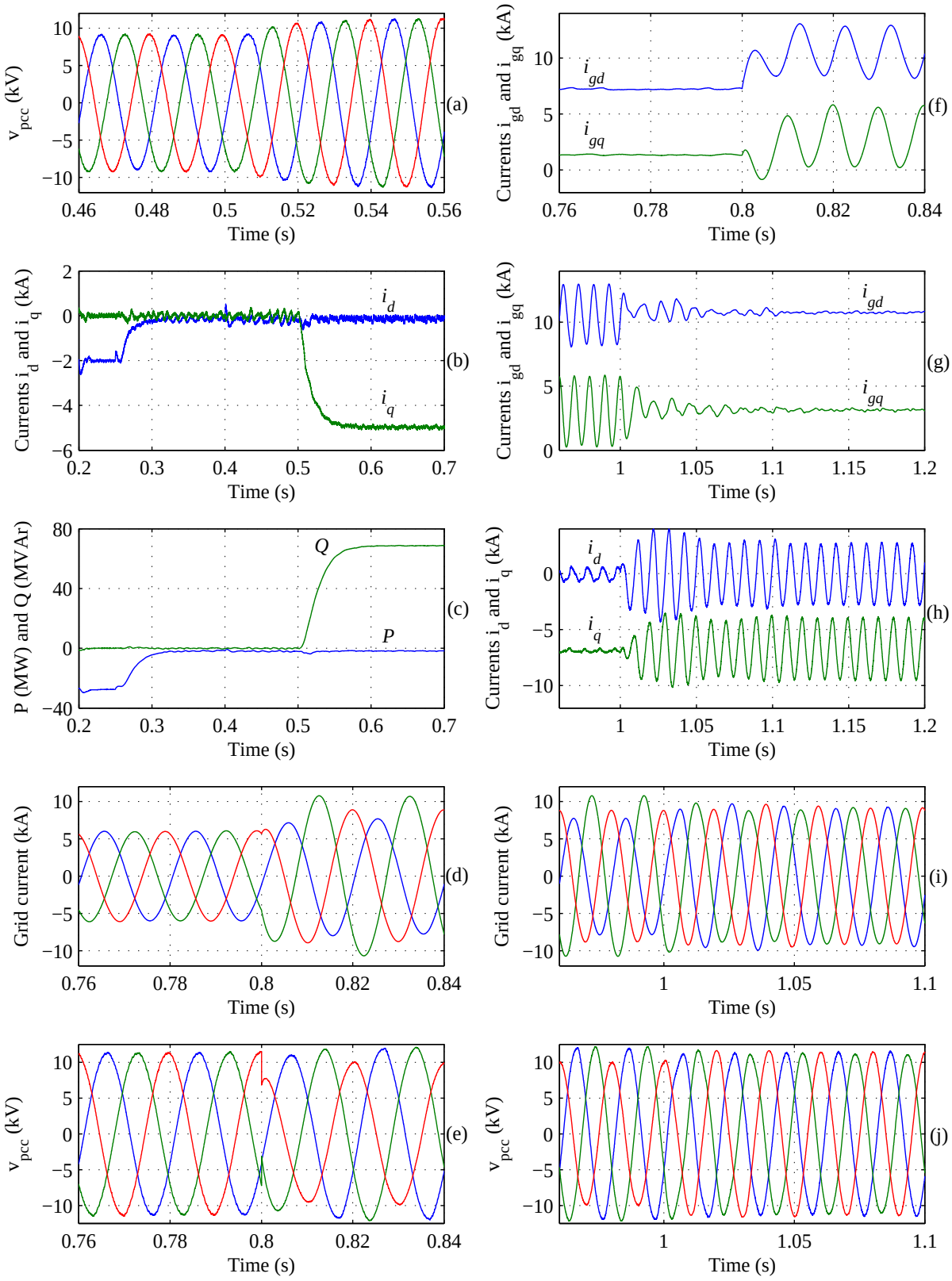


Figure 13b shows the d and q components of the current injected into the grid by the DSTATCOM for the time interval $0.2 \text{ s} \leq t \leq 0.7$ s; the time responses of both components are fully decoupled, and the current, i_d, is initially negative, as the DSTATCOM absorbs active power in order to charge the capacitors of the VSC (*i.e.*, the DC capacitor and the flying capacitors) and to maintain the voltage in the DC capacitor at its reference value. This active-power absorption can be seen in Figure 13c, which plots the active and reactive powers injected into the grid: it will be noted that the active power is proportional to the current, i_d, and that the reactive power is proportional to the current, i_q. At instant $t = 0.5$ s, the control system of the PCC voltage increases the reactive power injected into the grid in order to compensate for the voltage sag caused at $t = 0.3$ s, without active power consumption.

Figure 13. Waveforms obtained for several time intervals: (**a**) PCC line-to-neutral voltage (0.46 s $\leq t \leq 0.56$ s); (**b**) DSTATCOM currents i_d and i_q; (**c**) active and reactive powers injected into the grid (0.2 s $\leq t \leq 0.7$ s); (**d**) grid line currents; (**e**) PCC line-to-neutral voltages; (**f**) grid currents i_{g_d} and i_{g_q} (0.76 s $\leq t \leq 0.84$ s); (**g**) grid currents i_{g_d} and i_{g_q}; (**h**) DSTATCOM currents i_d and i_q; (**i**) grid line currents grid and (**j**) PCC line-to-neutral voltages (0.96 s $\leq t \leq 1.1$ s).



At instant $t = 0.8$ s, the line-to-line short-circuit takes place; the three line currents of the grid are plotted in Figure 13d, showing that the three currents are unbalanced after the fault. Furthermore, as the different PI controllers designed to operate the DSTATCOM do not have sufficient bandwidth to deal with voltage imbalances, the three resulting line-to-neutral voltages at the PCC are also unbalanced, as shown in Figure 13e. The current imbalance can also be observed when analyzing the d and q components in the SRF of the grid current: at $t = 0.8$ s, both components contain not only a DC component, but also a second harmonic component, as Figure 13f shows. When the control system designed to ameliorate the imbalances of the grid current is connected at $t = 1$ s, the DSTATCOM compensates for the second harmonic component of the grid current shown in Figure 13f by means of the injection of current containing a second harmonic. This result can be seen in Figures 13g,h: the resonant-type controller, which has been tailored to eliminate the second harmonic of the grid current in the SRF, performs effectively to achieve a balanced grid current. Obviously, the current injected by the DSTATCOM is then unbalanced. Moreover, the balancing current process can also be analyzed by observing the three-phase system magnitudes: the three line currents of the grid are plotted in Figure 13i, which shows no current imbalances at the steady state. As a consequence, the three line-to-neutral voltages are also balanced, as shown in Figure 13j.

Although the controller used to balance the grid current has been designed to eliminate current imbalances, which only contain positive and negative sequences, it should be stressed that this design can also be extended to compensate for those imbalances that involve the homopolar component. Furthermore, various resonant regulators can be used in parallel in order to eliminate current harmonics.

The time response of the voltage in the DC capacitor is shown in Figure 14: the value at the steady state is 120 kV, and the control system is able to maintain the DC voltage value almost constant, regardless of the various voltage sags and current imbalances for which the DSTATCOM must compensate.

Figure 14. Voltage in the DC capacitor.

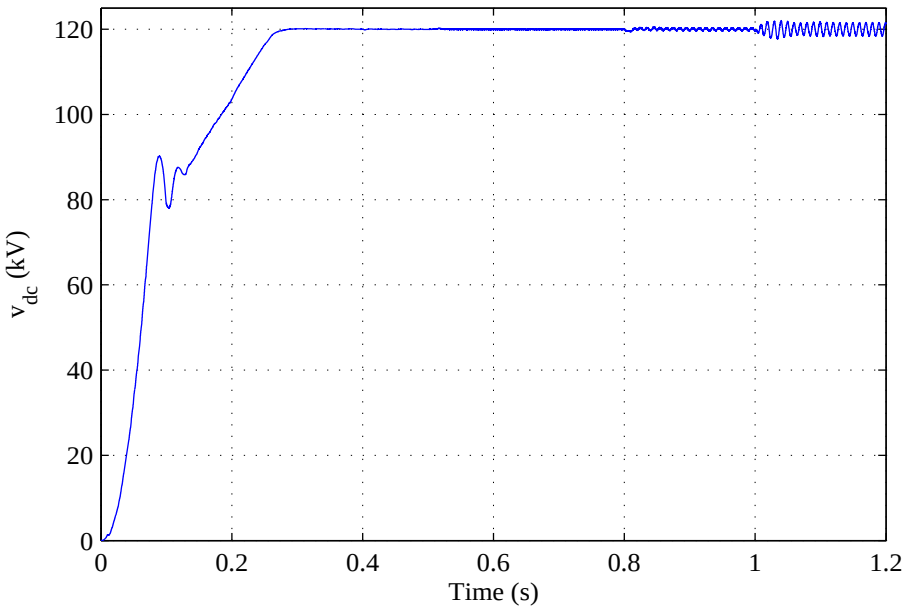
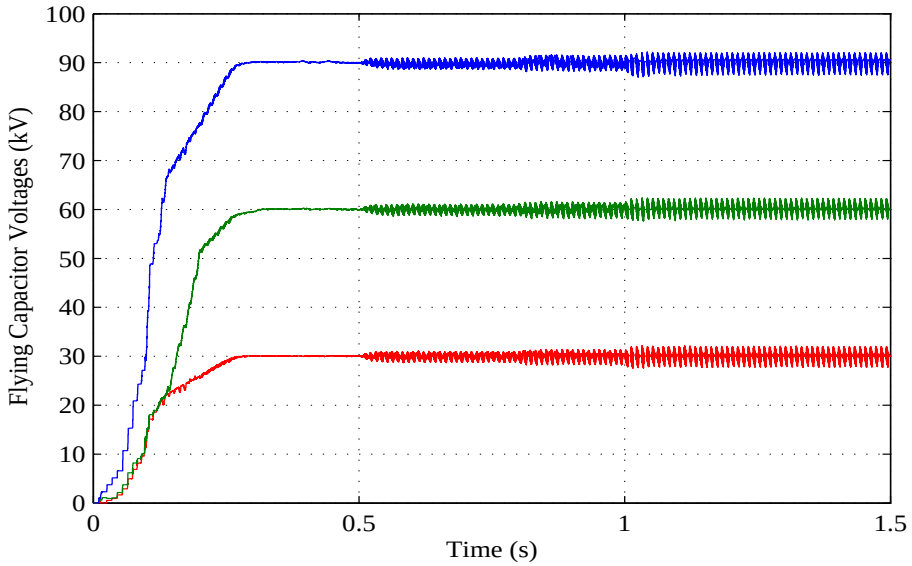


Figure 15 shows the flying capacitor voltages corresponding to leg A of the VSC depicted in Figure 3. The FC voltages of the other two legs of the VSC have been omitted for reasons of simplicity. The

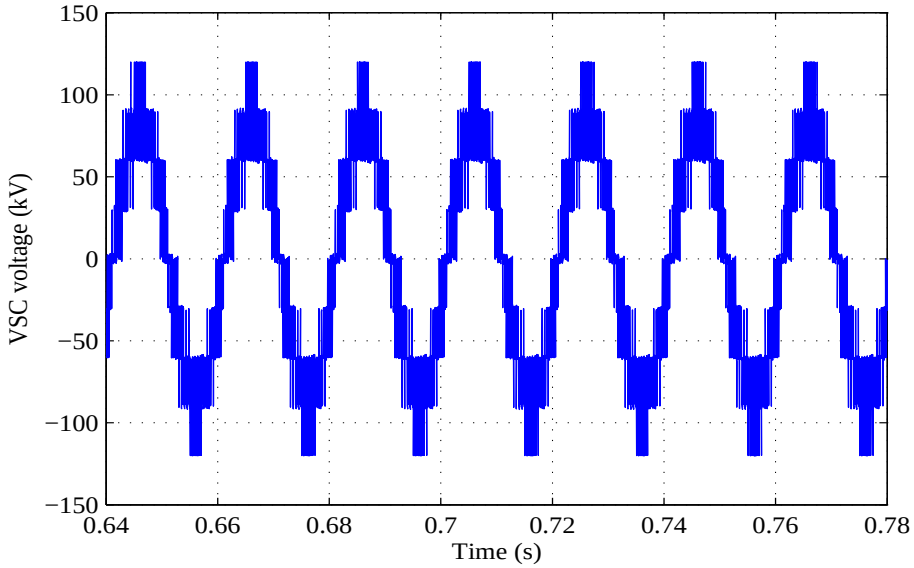
amplitude of the square wave was initially set to 30 kV in order to charge the flying capacitors to their references, namely 90 kV for C_1, 60 kV for C_2 and 30 kV for C_3. Once the FC voltages are equal to their references, the amplitude of the square wave is reduced to 5 kV at $t = 0.3$ s, and the control system maintains the voltage in the flying capacitors constant and balanced, despite the voltage sags at the PCC and the imbalances of the grid current.

Figure 15. Voltages of the flying capacitors (leg A of the voltage-source converter (VSC)) in kV: V_{C_1} (blue), V_{C_2} (green) and V_{C_3} (red).



The line-to-line output voltage of the five-level FC VSC corresponding to the time interval $0.64 \text{ s} \leq t \leq 0.78$ s is plotted in Figure 16: the line-to-line output voltage contains nine levels (*i.e.*, $2n - 1$ levels) and is close to a sinusoidal waveform with a small harmonic distortion, which implies an advantage over the more conventional two-level and three-level VSC topologies.

Figure 16. Line-to-line output voltage of the five-level flying-capacitor (FC) VSC ($0.64 \text{ s} \leq t \leq 0.78$ s.).



5. Conclusions

This paper has presented the design of a control system for the operation of a DSTATCOM based on a five-level flying-capacitor VSC connected to a distribution grid. The control system is tailored to compensate for voltage sags and voltage imbalances caused by unbalanced loads. The compensation of these voltage imbalances is achieved by balancing the grid current. The overall control system is split into various subsystems: the first one is responsible for controlling the voltage in the DC capacitor; a second subsystem works to regulate the voltage at the PCC, whereas a third subsystem is employed to balance the grid current. Finally, a fourth control scheme deals with the balancing of the voltages in the flying capacitors. Basic linear regulators are used in the design, such as PI controllers and resonant controllers. The design has been carried out using classical linear control tools, namely, the root-locus and the frequency response techniques, with special attention paid to the criteria and specifications of the design. This fact allows one not only to obtain a better time response of the overall control system, but also to provide a design methodology that can be used to add more functionalities to the DSTATCOM, such as compensation or current harmonics by adding various resonant controllers in parallel.

The DSTATCOM and the control system have been implemented in PSCAD/EMTDC. The simulation results obtained show that the DSTATCOM performs very effectively in terms of dynamics and steady-state error when compensating for voltage sags and voltage imbalances.

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Author Contributions

Pedro Roncero-Sánchez and Enrique Acha defined the control-system configuration. Enrique Acha was responsible of the design of the case study, while the simulations were carried out by Pedro Roncero-Sánchez. Both authors have participated in the writing process of the paper.

Conflicts of Interest

The authors declare no conflicts of interest.

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