Energies **2015**, *8*, 2032-2047; doi:10.3390/en8032032

OPEN ACCESS

energies

ISSN 1996-1073

www.mdpi.com/journal/energies

Article

A Varied VSVM Strategy for Balancing the Neutral-Point Voltage of DC-Link Capacitors in Three-Level NPC Converters

Shi Weng Gui *, Zhen Jun Lin and Sheng Hua Huang

State Key Laboratory of Advanced Electromagnetic Engineering and Technology, Huazhong University of Science and Technology, Wuhan 430074, China;
E-Mails: linzhenjun@hust.edu.cn (Z.J.L.); huangsh@163.com (S.H.H.)

* Author to whom correspondence should be addressed; E-Mail: gabrielgsw@hust.edu.cn; Tel.: +86-27-8754-2626.

Academic Editor: Frede Blaabjerg

Received: 6 January 2015 / Accepted: 28 February 2015 / Published: 13 March 2015

Abstract: In the research field of multilevel converters, three-level NPC (neutral-point-clamped) converters, which unfortunately may cause the deviation of the neutral-point voltage of DC-link capacitors, are widely discussed. Theoretically, virtual space vector modulation (VSVM) could guarantee the balance control of the neutral-point voltage. However, there still exist some uncontrollable space vector regions. Based on VSVM, this paper proposes a varied virtual space vector modulation (VVSVM) method for three-level NPC converters. Under complete modulation conditions, this method can control the balance of the neutral-point voltage of DC-link capacitors by adjusting the duty cycle of small vectors and regulating the current generated by virtual medium vectors. Compared with commonly used VSVM methods and mixed modulation strategies, this method is simpler and more practical. The effectiveness and validity of this method are verified by simulations and experiments.

Keywords: three level; neutral-point-clamped (NPC) converter; space vector modulation (SVM); virtual space vector modulation (VSVM); varied virtual space vector modulation (VVSVM)

---

1. Introduction

Multilevel converter topologies are considered to be the best choice for medium and high voltage applications for their less output harmonic voltage and higher voltage level. Among the multilevel converter topologies, the three-level neutral-point clamped (NPC) converter, as shown in Figure 1a, is a widely-researched topology [1,2]. Nevertheless, owing to its topology characteristics, the capacitor's neutral-point voltage sometimes fluctuates when the three-level NPC converter works, and this causes harmonic distortion of the three phase output voltage, which limits its wide use [3–5].

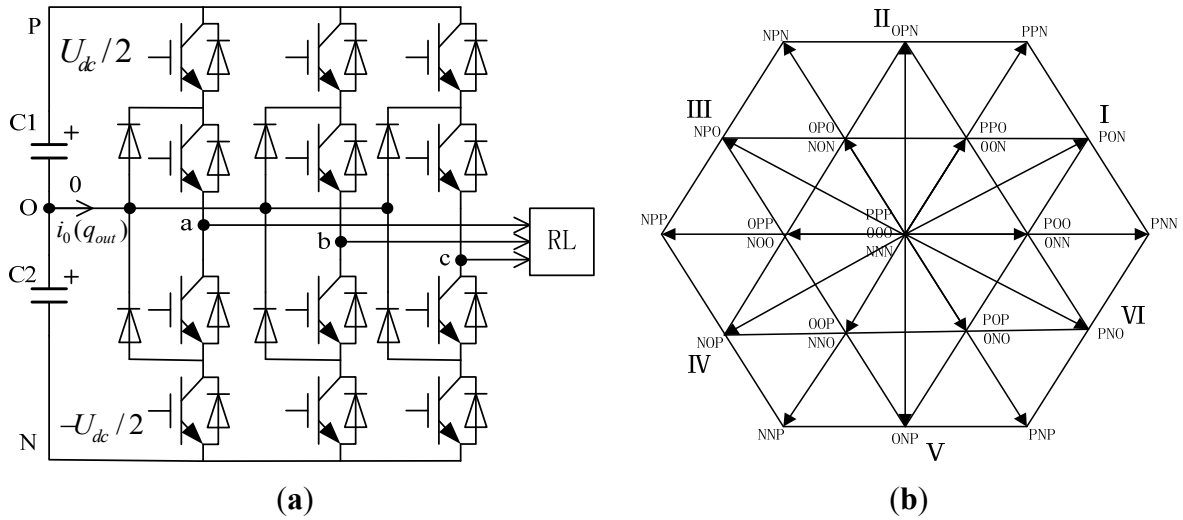


Figure 1. Schematic of a three-level NPC converter. (**a**) Topology structure of three-level NPC converter; (**b**) Distribution diagram of voltage vectors.

In recent years, the balance control of neutral-point voltage has been a hot topic and some strategies have been proposed in [6–9]. Among these strategies, space vector modulation (SVM) is one of the most commonly used modulation strategies, which has the advantages of low switching frequency and better output voltage quality [10,11]. However, when SVM is applied, the medium vectors will affect the neutral-point voltage, which will cause low-frequency oscillations in the neutral-point voltage under high modulation conditions [12]. The paper [13] proposed an improved SVM excluding medium vectors. It can solve the low-frequency voltage oscillation issue. However, without the medium vectors to synthesize the space vectors, this will increase the possibility of distortion of the output voltage and increase the harmonic content of the output voltage. The paper [14] proposed a new SVM, which can balance the neutral-point voltage of DC-link capacitors by modulating the conduction time of the switch tube.

Furthermore, the papers [15,16] proposed a VSVM method which has been theoretically proven not to cause oscillation on the neutral-point voltage. This strategy employs an optimized virtual space vector with less distortion of the output voltage. However, the criterion to design the controller for neutral-point balancing is not presented in these papers. In practice, the balance of neutral-point voltage of DC-link capacitors is not very satisfactory, owing to the asymmetric parameters of components, switching delay and asymmetry of DC-link capacitors. Based on VSVM, the paper [17] proposed a method to balance the neutral-point voltage according to the fact that positive and negative

small vectors have opposite effects on the neutral-point voltage. Although this method combines the merits of VSVM and SVM, the neutral-point voltage can't be controlled in some space vector regions when the modulation index m is between 0.667 and 1 ($0.667 < m < 1$), because there is not a pair of positive and negative small vectors in some vector regions. The papers [18–21] proposed some mixed strategies switching between the method of VSVM and SVM in some space vector regions, but the above methods are quite complex to manipulate. The paper [22] proposed a method to restrict the fluctuation of the neutral-point voltage of DC-link capacitors by optimizing the switch tube order. Because the three-level NPC converter itself has many vectors, increasing the number of switch sequence choices makes it more complex to programme.

In this paper, a varied virtual space vector modulation (VVSVM) is proposed on the basis of VSVM not affecting the balance of DC-link capacitors voltage theoretically [15], and the proposed strategy is designed to keep the balance of the neutral-point voltage of DC-link capacitors through adjusting the duty cycle of small vectors and regulating the current generated by virtual medium vectors. Unlike the conventional VSVM, when the modulation index is between 0.667 and 1, this strategy can maintain the balance of the neutral-point voltage of DC-link capacitors in all vector regions where the conventional VSVM strategy cannot. Experiment and simulation have verified the effectiveness of the proposed strategy.

2. Varied Virtual Space Vector Modulation

In the typology of a three-level NPC converter, as shown in Figure 1a, P, O and N represent three output voltage values: $U_{dc}/2$, 0, $-U_{dc}/2$, where U_{dc} is the DC-link voltage. Figure 1b is the distribution diagram of the voltage vectors, from which we can know that the NPC converter has 27 space vectors. According to the definition and distribution of virtual space vectors in VSVM [15,16], this paper designs a group of new varied virtual space vectors. Taking sextant I as an example, the virtual voltage vectors are established in sextant I, as shown in Figure 2a.

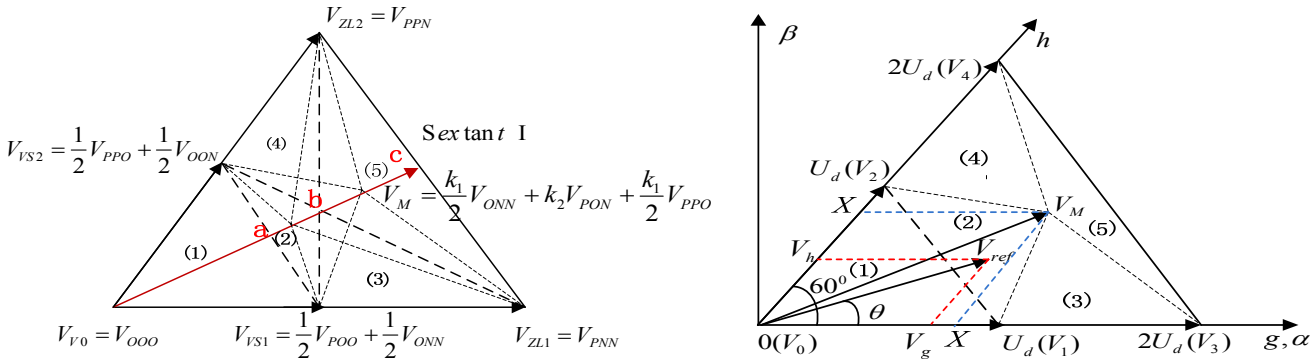


Figure 2. *Cont.*

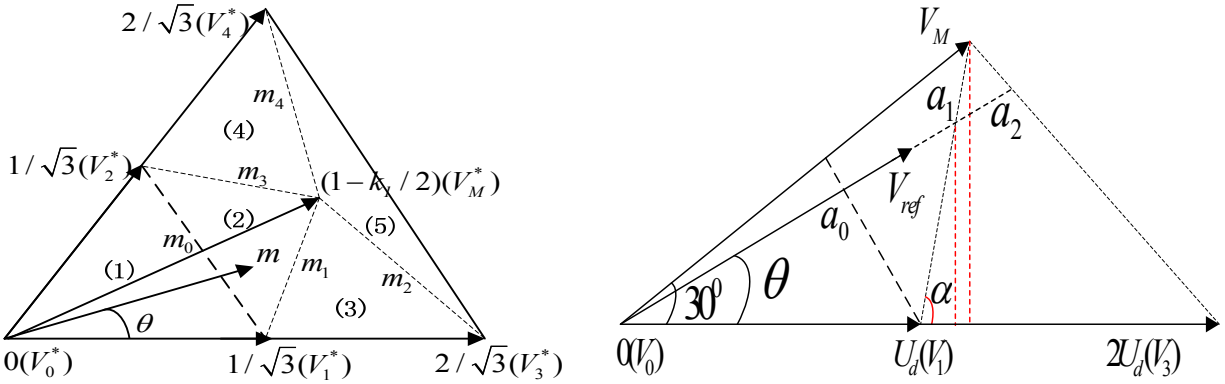


Figure 2. Distribution of varied virtual space voltage vectors in sextant I; (**a**) Definition and distribution of varied virtual space voltage vectors in sextant I; (**b**) Virtual space voltage vectors in g_h coordinate; (**c**) Distribution diagram of varied virtual vectors in Sextant I (60° Sextant); (**d**) The calculation of m_1.

2.1. The Definition of Varied Virtual Space Vectors

(a) Definition of virtual small vectors: the virtual small vectors are built under the precondition that positive and negative small vectors have opposite interactions on the neutral-point voltage fluctuation. Taking the positive and negative small vectors (*POO* ($-i_a$), *ONN* (i_a)) for example, the virtual small vector (V_{VS1}) is formed as follows (V_{VS2} is formed in a similar way):

$$V_{VS1} = k \cdot V_{POO} + (1-k) \cdot V_{ONN}, and\ 0 \le k \le 1 \tag{1}$$

Assuming that the three phases current (i_a, i_b, i_c) stay unchanged in a short switching period T_S, during the duty cycle T_{VS1} of a virtual small vector V_{VS1}, the three phase load current i_a, i_b, i_c is connected to the neutral-point O, the charge flowing out from which is represented as:

$$q_{VS1} = -i_a \cdot k \cdot T_{VS1} + i_a \cdot (1-k) \cdot T_{VS1} \tag{2}$$

It is noted that when k = 1/2, the charge from the neutral-point O: q_{VS1} = 0, so during the duty cycle T_{VS1} of virtual small vector V_{VS1}, the neutral-point voltage of DC-link capacitors is not affected.

(b) Definition of varied virtual medium vectors: assuming that during a switching period T_S, the three-phase currents i_a, i_b, i_c stay steady, and $i_a + i_b + i_c = 0$. By combining the small vectors V_{PPO} (i_c) and V_{ONN} (i_a) and the medium vectors V_{PON} (i_b), a virtual medium vector V_M is synthesized as follows:

$$V_M = (\frac{k_1}{2} \cdot V_{ONN} + k_2 \cdot V_{PON} + \frac{k_1}{2} \cdot V_{PPO}) \tag{3}$$

$$k_1 + k_2 = 1,\ and\ \ k_1 > 0,\ k_2 > 0 \tag{4}$$

From Equations (3) and (4), it can be seen that during the duty cycle T_m of virtual medium vector V_M, the three phase load current will be connected to the neutral-point O respectively at a different time. The charge flowing out from the neutral-point (O) is described as follows, during the duty cycle T_m of the virtual medium vector:

$$\begin{aligned} q_{T_m} &= \int_0^{T_S} i_o dt = \int_0^{T_m \cdot \frac{k_1}{2}} i_a dt + \int_0^{T_m \cdot k_2} i_b dt + \int_0^{T_m \cdot \frac{k_1}{2}} i_c dt \\ &= T_m \cdot (\frac{k_1}{2} \cdot i_a + k_2 \cdot i_b + \frac{k_1}{2} \cdot i_c) \\ &= T_m \cdot (1 - \frac{3k_1}{2}) \cdot i_b \end{aligned} \quad (5)$$

Equation (6) describes the relationship between the voltage of capacitors and the charge flowing out from the neutral-point:

$$\Delta(U_{c1} - U_{c2}) = \frac{1}{C} \cdot q_{T_m} \quad (6)$$

During the duty cycle T_m of varied virtual space vector, the following conclusions are drawn according to Equations (5) and (6):

(1) When k_1 = 2/3, the virtual medium vector locates at the point b, and the charge q_{Tm} flowing out from the neutral-point O is zero. This virtual medium vector will not cause a fluctuation of the neutral-point voltage, which is the same as the neutral-point voltage in the traditional VSVM (modulation index m = 0.667). Because the length of the virtual medium vector stays steady in the process of synthesizing the voltage space vector V_{ref}, the traditional VSVM can't use the virtual medium vector to balance the neutral-point voltage of DC-link capacitors.

(2) When 1 > k_1 > 2/3, the virtual medium vector locates between a and b.

- If i_b > 0, the charge flowing out from the neutral-point O: q_{Tm} < 0, and U_{C1} gets smaller; U_{C2} get larger.
- If i_b < 0, the charge flowing from the neutral-point O: q_{Tm} > 0, and U_{C1} gets larger; U_{C2} get smaller.

(3) When 2/3 > k_1 > 0, the virtual medium vector locates between b and c.

- If i_b > 0, the charge flowing from the neutral-point O: q_{Tm} > 0, and U_{C1} gets larger; U_{C2} get smaller.
- If i_b < 0, the charge flowing out from the neutral-point O: q_{Tm} < 0, and U_{C1} gets smaller; U_{C2} get larger.

(c) Definition of virtual zero vectors: V_{V0} = V_{OOO}. The virtual zero vectors don't affect the neutral-point voltage.

(d) Definition of virtual long vectors: V_{VL1} = V_{PNN}, V_{VL2} = V_{PPN}. The virtual long vectors don't affect the neutral-point voltage.

2.2. Judgment of Small Regions in 60° Sextant

As shown in Figure 2a, taking sextant I for example, it can be divided into five small regions (1)–(5), according to the location of vectors (U_{dc} denotes the DC-link voltage, V_{ref} is the reference vector, θ is the reference vector angle, U_d denotes U_{dc}/3 and the modulation index is defined as: $m = |V_{ref}| / \sqrt{3} U_d$).

The length of varied virtual medium vector can be represented by Equation (7):

$$\begin{cases} |V_{\mathrm{M}}| = \sqrt{3}U_{\mathrm{d}}(1-k_1/2) \\ U_{\mathrm{d}} = U_{\mathrm{dc}}/3 \end{cases} \tag{7}$$

As shown in Figure 2d, the following formula is derived as:

$$\begin{cases} \tan\alpha = \dfrac{|V_{\mathrm{M}}|/2}{\sqrt{3}\cdot|V_{\mathrm{M}}|/2 - U_{\mathrm{d}}} \\ \tan\alpha = \dfrac{a_1\cdot\sin\theta}{a_1\cdot\cos\theta - U_{\mathrm{d}}} \end{cases} \tag{8}$$

where:

$$m_1 = a_1/(\sqrt{3}U_{\mathrm{d}}) \tag{9}$$

As shown in Figure 2c, from Equations (8) and (9), the m_1 is written as:

$$m_1 = \frac{|V_{\mathrm{M}}|}{\sqrt{3}(\sin\theta(2U_{\mathrm{d}} - \sqrt{3}|V_{\mathrm{M}}|) + |V_{\mathrm{M}}|\cos\theta)} \tag{10}$$

Similarly, the calculation formulas of m_0, m_1, m_2, m_3, m_4 are expressed as follows:

$$\begin{cases} m_0 = 1/(\sqrt{3}\cos\theta + \sin\theta) \\ m_1 = \dfrac{|V_{\mathrm{M}}|}{\sqrt{3}(\sin\theta(2U_{\mathrm{d}} - \sqrt{3}|V_{\mathrm{M}}|) + |V_{\mathrm{M}}|\cos\theta)} \\ m_2 = \dfrac{2|V_{\mathrm{M}}|}{\sqrt{3}(\sin\theta(4U_{\mathrm{d}} - \sqrt{3}|V_{\mathrm{M}}|) + |V_{\mathrm{M}}|\cos\theta)} \\ m_3 = \dfrac{|V_{\mathrm{M}}|}{\sqrt{3}(\sin(60^0-\theta)(2U_{\mathrm{d}} - \sqrt{3}|V_{\mathrm{M}}|) + |V_{\mathrm{M}}|\cos(60^0-\theta))} \\ m_4 = \dfrac{2|V_M|}{\sqrt{3}(\sin(60^0-\theta)(4U_{\mathrm{d}} - \sqrt{3}|V_{\mathrm{M}}|) + |V_{\mathrm{M}}|\cos(60^0-\theta))} \end{cases} \tag{11}$$

The small region in which the reference vector locates is confirmed according to Equations (7) and (11), the modulation index and the regulation of judging small region (Table 1).

Table 1. Judging the small region of the reference vector.

Small region	Condition 1	Condition 2
(1)	$0 < m \le m_0$	-
(2)	$m_0 < m \le m_1$	$0 \le \theta < \pi/6$
	$m_0 < m \le m_3$	$\pi/6 \le \theta < \pi/3$
(3)	$m_1 < m \le m_2$	$0 \le \theta < \pi/6$
(4)	$m_3 < m \le m_4$	$\pi/6 \le \theta < \pi/3$
(5)	Other	-

2.3. Synthesis of Vectors

From the divided small regions in sextant I above, three virtual voltage vectors are determined to synthesize the reference vector. To simplify the calculation, we choose 60° coordinate (g_h coordinate) to calculate the time of vector synthesis. Taking the space voltage vector V_{ref} which locates at region (2) for example, the duty cycle of the relative vectors is calculated as follows.

As shown in Figure 2b, in the g_h coordinate, the reference voltage vector V_{ref} can be represented as:

$$\begin{cases} V_g = V_{ref}(\cos\theta - \sin\theta/\sqrt{3}) \\ V_h = 2V_{ref}\cdot\sin\theta/\sqrt{3} \end{cases} \quad (12)$$

According to the principle of vectors synthesis, the modulation rules of the nearest three vectors are established as follows:

$$\begin{cases} T_s\cdot V_g = U_d\cdot T_1 + X\cdot T_m \\ T_s\cdot V_h = U_d\cdot T_2 + X\cdot T_m \\ T_s = T_1 + T_2 + T_m \end{cases} \quad (13)$$

where ($X = U_d(1 - k_1/2)$ represents the projection of virtual medium vector on the *g*-axis and *h*-axis.)

From Equations (12) and (13), we obtain the following equation:

$$\begin{cases} T_1 = \dfrac{T_s\cdot[V_h\cdot X + V_g\cdot(U_d - X) - U_d\cdot X]}{U_d\cdot(U_d - 2X)} \\ T_2 = \dfrac{T_s\cdot[V_g\cdot X + V_h\cdot(U_d - X) - U_d\cdot X]}{U_d\cdot(U_d - 2X)} \\ T_m = T_s - T_1 - T_2 \end{cases} \quad (14)$$

Similarly, the duty cycle of other virtual vectors is calculated, and Table 2 shows the duty cycle of virtual vectors in sextant I.

Table 2. Duty cycle of voltage vectors in sextant I.

Small region	Duty cycle 1	Duty cycle 2	Duty cycle 3
region(1) V_0, V_1, V_2	$T_1 = \dfrac{T_s\cdot V_g}{U_d}$	$T_2 = \dfrac{T_s\cdot V_h}{U_d}$	$T_0 = T_s - T_1 - T_2$
region(2) V_1, V_2, V_{M1}	$T_1 = \dfrac{T_s\cdot[V_h\cdot X + V_g\cdot(U_d - X) - U_d\cdot X]}{U_d\cdot(U_d - 2X)}$	$T_2 = \dfrac{T_s\cdot[V_g\cdot X + V_h\cdot(U_d - X) - U_d\cdot X]}{U_d\cdot(U_d - 2X)}$	$T_m = T_s - T_1 - T_2$
region(3) V_1, V_3, V_{M1}	$T_3 = \dfrac{T_s\cdot[V_g\cdot X + V_h\cdot(U_d - X) - U_d\cdot X]}{U_d\cdot X}$	$T_m = \dfrac{T_s\cdot V_h}{X}$	$T_1 = T_s - T_3 - T_m$
region(4) V_2, V_4, V_{M1}	$T_4 = \dfrac{T_s\cdot[V_h\cdot X + V_g\cdot(U_d - X) - U_d\cdot X]}{U_d\cdot X}$	$T_m = \dfrac{T_s\cdot V_g}{X}$	$T_2 = T_s - T_4 - T_m$
region(5) V_3, V_4, V_{M1}	$T_3 = \dfrac{T_s\cdot[V_g\cdot(2U_d - X) + V_h\cdot X - 2U_d\cdot X]}{4U_d\cdot(U_d - X)}$	$T_4 = \dfrac{T_s\cdot[V_h\cdot(2U_d - X) + V_g\cdot X - 2U_d\cdot X]}{4U_d\cdot(U_d - X)}$	$T_m = T_s - T_3 - T_4$

2.4. The Amplitude of the NP Voltage Oscillations

In a switching period, the NP voltage ripple of the NPC converter is defined as:

$$\Delta u_1 = \frac{I_{ave}\cdot T_m}{C} \quad (15)$$

where Δu_1 is the amplitude of the ripple on the neutral-point voltage, I_{ave} is the average neutral-point current, T_m is the duty cycle of the virtual medium vector, C is the value of the DC-link capacitors. Thus, increasing the value of the capacitors and the switching frequency is helpful for balancing the neutral-point voltage.

3. Neutral-Point Balancing Strategy

3.1. Neutral-Point Balancing Algorithm in Small Region (1)

Taking sextant I for example, we choose the small vectors to synthesize the reference vector when reference vector V_{ref} locates in small region (1) in this paper. Assuming that the three phase output currents (i_a, i_b, i_c) stay constant in a switching period T_S, where d_{min} symbolizes the duty cycle of virtual small vector (V_1), d_{min_p} and d_{min_n} respectively represents the duty cycle of the positive small vector (V_{POO}) and negative small vector (V_{ONN}), and $d_{min\_p} + d_{min\_n} = d_{min}$; $i_{min\_p}(-i_a)$ represents the neutral-point current of dc-link capacitors during the duty cycle of positive small vector; $i_{min\_n}(i_a)$ represents the neutral-point current of DC-link capacitors during the duty cycle of negative small vector. As shown in Figure 1a, the charge q_{out} flowing out of the neutral-point O over a switching period T_S can be represented as follows:

$$\begin{aligned} q_{out} &= i_{min\_p} \cdot d_{min\_p} + i_{min\_n} \cdot d_{min\_n} \\ &= i_{min\_p} \cdot k \cdot d_{min} + i_{min\_p} \cdot (k-1) \cdot d_{min} \\ &= (2k-1) i_{min\_p} \cdot d_{min}, \ and \ (0 \le k \le 1) \end{aligned} \tag{16}$$

During the switching period T_S, the relationship between the capacitors voltage and the charge flowing out of the neutral-point O can be represented as:

$$\Delta(U_{c1} - U_{c2}) = \frac{1}{C} \cdot q_{out} \tag{17}$$

From Equations (16) and (17), we can obtain the following equation:

$$\Delta(U_{c1} - U_{c2}) = \frac{1}{C} \cdot (2k-1) \cdot d_{min} \cdot i_{min\_p} \tag{18}$$

If the voltage transducer detects the deviation (ΔU) of neutral-point voltage, then during the next switching period the current of the positive and negative small vectors should generate voltage $-\Delta U$ to offset the deviation, and keep the balance of the neutral-point voltage of DC-link capacitors. Therefore, according to Equation (18), we could calculate the value of control factor k in the next sampling period.

3.2. Balancing Strategy for Neutral-Point Voltage in Small Regions (2)–(5)

The neutral-point current generated by the virtual medium vector is used to offset the voltage deviation of DC-link capacitors, which can realize the voltage balance in the small regions (2)–(5). As a result, the balance of neutral-point voltage can be maintained in VVSVM, when the modulation index is between 0 and 1 ($0 < m < 1$).

Taking sextant I for example, the location of virtual medium vector could be determined by detecting the fluctuation of neutral-point voltage in the next sampling period to maintain the balance of the neutral-point voltage. During the duty cycle of virtual medium vector, the following equation is obtained according to Equations (5) and (6):

$$\begin{cases} \Delta(U_{c1} - U_{c2}) = \dfrac{1}{C} \cdot T_m \cdot (1 - \dfrac{3k_1}{2}) \cdot i_b \\ (0 < k_1 < 1) \end{cases} \tag{19}$$

If the reference vector voltage V_{ref} locates between small region (2) to (5) and the deviation ΔU of the neutral-point voltage is detected, the virtual medium vector current could generate $-\Delta U$ voltage to offset the deviation during the next switching period T_S. According to Equation (19), the fluctuation of neutral-point voltage of DC-link capacitors can only judge whether the virtual medium vector locates at a-b or b-c as shown in Figure 2a. Because the neutral-point voltage doesn't change a lot in a sampling period, this paper uses T_m' of the previous sampling period to calculate the approximate value of k_1.

4. Simulation and Experimental Verification

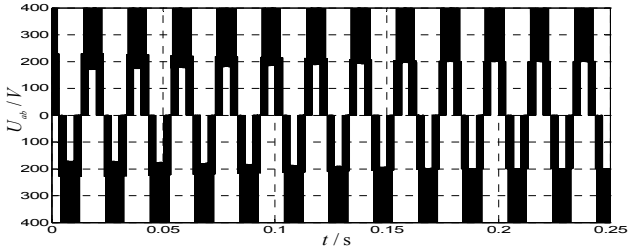
This section presents the simulation and experiment results of three level neutral-point NPC converter to verify the effectiveness of the proposed VVSVM strategy by comparing it with the VSVM strategy. Simulation and experiment environments are performed as follows: DC-link voltage: U_{dc} = 400 V; three-phase resistance-inductance load: R = 15 Ω, L = 10 mH; DC-link capacitors: $C_1 = C_2$ = 2000 μF; sampling frequency: 8 kHz; fundamental frequency: 50 Hz. The dead time of the system is set as 3 μs and the modulation index is 0.83.

4.1. Simulation Results

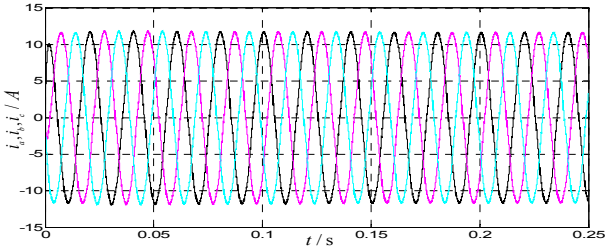
To verify the balancing performance of the proposed modulation technique, the initial voltage of the DC-link capacitors is set as: U_{C1} = 230 V, U_{C2} = 170 V. In the simulation process, from 0 s to 0.02 s, the deviation of capacitors voltage is maintained at 60 V by VSVM and VVSVM, and after 0.02 s the deviation of capacitors voltage is controlled to be zero.

Figure 3a–c shows the simulation results of VSVM which uses small vectors to balance the neutral-point voltage. Figure 3d–f shows the simulation results of the proposed VVSVM. By comparison of Figure 3c,f, either the VSVM or VVSVM can balance the capacitors voltage, but the dynamic balancing process of the capacitors voltage in VVSVM is faster than that of the capacitors voltage in VSVM.

When the modulation index is $1 > m > 0.667$ in VSVM strategy, the tip of reference vector (V_{ref}) is bound to fall in the region (5) of sextants I–VI because there is no pair of positive and negative small vectors for synthesizing V_{ref} in the small region (5). Thus, the VSVM strategy can't balance the deviation of capacitors voltage in this region. However, in the region (5), the proposed VVSVM strategy can control the balance of neutral-point voltage by regulating the current of the virtual medium vectors in region (5). So the balancing adjustment time of VVSVM is less than that of VSVM. From Figure 3a,d, it can be seen that line-line voltage waveform varies responding to the capacitors voltage varying through using VSVM and VVSVM.



(**a**)



(**b**)

Figure 3. *Cont.*

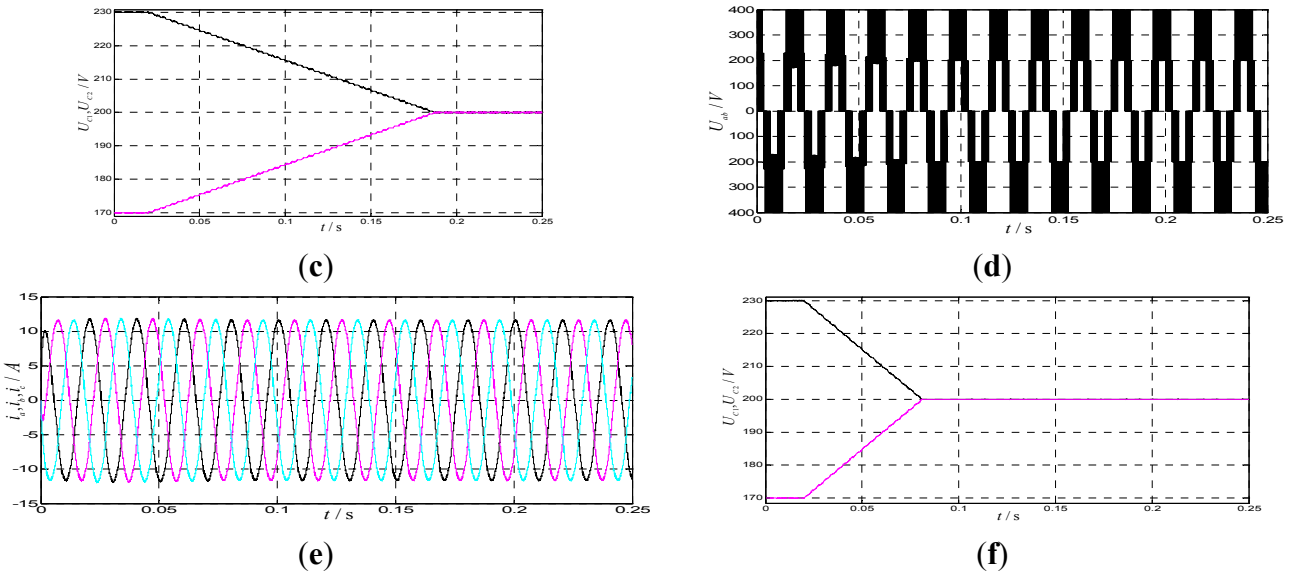


Figure 3. Simulation results of balancing DC-link capacitors voltage; (**a**) balancing process of line-to-line voltage in VSVM; (**b**) three phase currents in VSVM; (**c**) balancing process of DC-link capacitors voltage in VSVM; (**d**) balancing process of line-to-line voltage in VVSVM; (**e**) three phase currents in VVSVM; (**f**) balancing process of DC-link capacitors voltage in VVSVM.

Figure 4a,b shows the simulation results of VSVM under the condition of varying load. Figure 4c,d shows the simulation results of VVSVM under the condition of varying load. The voltage of DC-link capacitors is initially set as U_{C1} = 200 V, U_{C2} = 200 V. The load resistance suddenly changes from 15 to 8 Ω at 0.02 s. It can be seen that the load currents vary from 12 to 21 A at 0.04 s. Comparing Figure 4b,d, it can be seen that the voltage of the DC-link capacitors barely changes responding to changing the load, using the VVSVM. However, in VSVM strategy the DC-link capacitors voltage fluctuates obviously. Figure 5 shows the simulation results of VSVM and VVSVM in the case of varying DC-link voltage. The DC-link capacitors voltage is initially set as U_{C1} = 175 V, U_{C2} = 175 V. The DC-link voltage increased from 350 to 400 V at 0.04 s. Owing to the currents amplitude varying little along with transformed DC-link voltage, it can be seen from Figure 5c,f that the balancing effectiveness of VVSVM is the same as that of VSVM from the simulation results. However, it can be concluded that the VVSVM can better control the voltage balancing of the DC-link capacitors under varying DC-link voltage conditions.

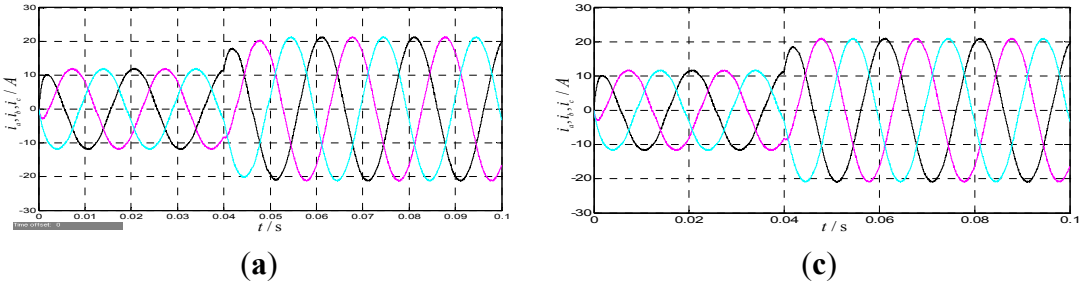


Figure 4. *Cont.*

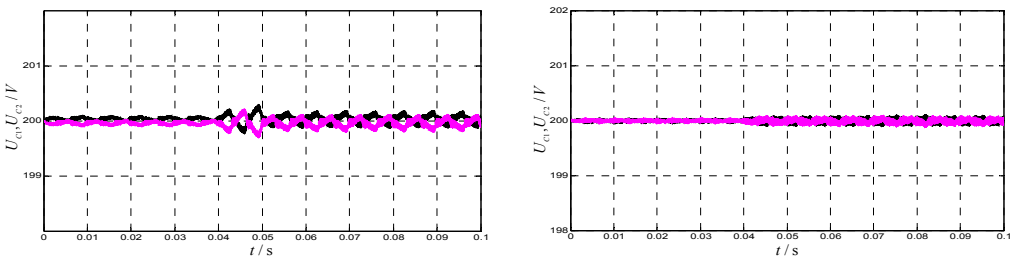


Figure 4. Simulation results of varying load. (**a**) response of the currents to varying load in VSVM; (**b**) capacitors voltage during varying load in VSVM; (**c**) response of the currents to varying load in VVSVM; (**d**) capacitors voltage during varying load in VVSVM.

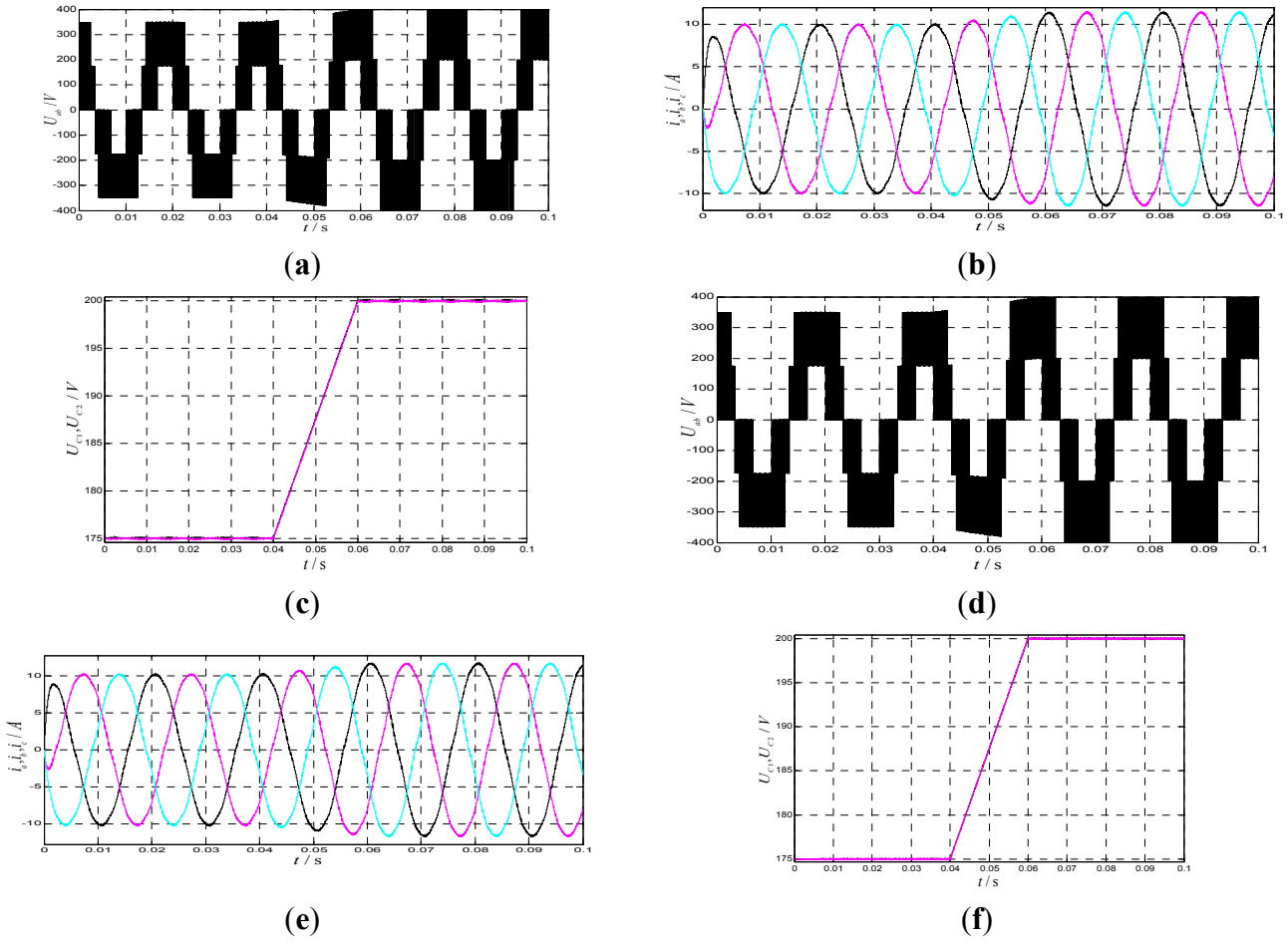


Figure 5. Simulation results of varying DC-link capacitors voltage; (**a**) varying process of line-to-line voltage in VSVM; (**b**) three phase currents in VSVM; (**c**) varying process of DC-link capacitors voltage in VSVM; (**d**) varying process of line-to-line voltage in VVSVM; (**e**) three phase currents in VVSVM; (**f**) varying process of DC-link capacitors voltage in VVSVM.

4.2. Experiment Results

To verify the effectiveness of the proposed VVSVM, three-level converter is made of six IGBT (Insulated Gate Bipolar Transistor) dual-modules 2MBI100U4H-170. The main processor is implemented with TMS320F28335 DSP (Digital Signal Processor) controller and EP3C10E144C8 FPGA (Field Programmable Gate Array) is used to generate and output pulse width modulation (PWM) signals for the converter.

Figure 6a,b shows the dynamic balancing of the DC-link capacitors voltage in VSVM and VVSVM, respectively. The voltage deviation is kept at a set value by subtracting a deviation value from the voltage difference of the DC-link capacitors, so the initial deviation between U_{C1} and U_{C2} can be controlled. In the initial conditions, the deviation of U_{C1} and U_{C2} is keep at 60 V, and then controlled to be 0 V. From Figure 6a,b, it can be seen that the balancing time of the proposed VVSVM is half of that of VSVM, which is significant to the application of the high power and large current. Thus it could be concluded that the proposed VVSVM has a good effectiveness of balancing the capacitors voltage.

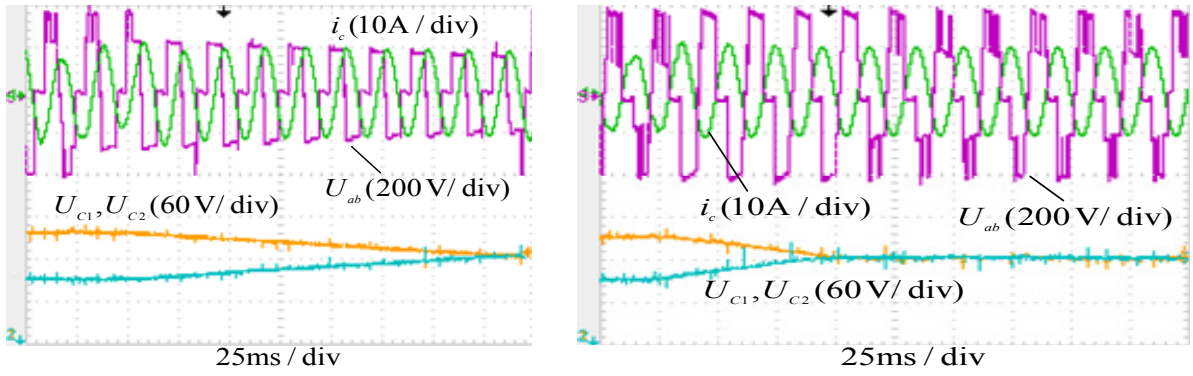


Figure 6. Experiment results of balancing the capacitors voltage: (**a**) VSVM; (**b**) VVSVM.

Figure 7 shows the balanced state waveforms of the line-to-line voltage and the DC-link capacitors voltage using VSVM and VVSVM. From Figure 7b, it can be seen that when conducting the proposed VVSVM, the line-to-line voltage is a steady three-level wave, that's to say, U_{C1} and U_{C2} stay steady.

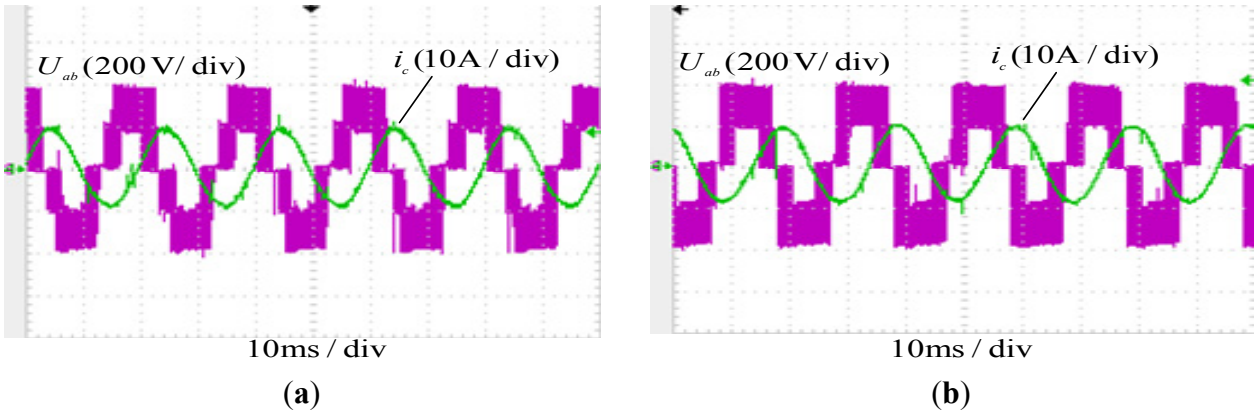


Figure 7. *Cont.*

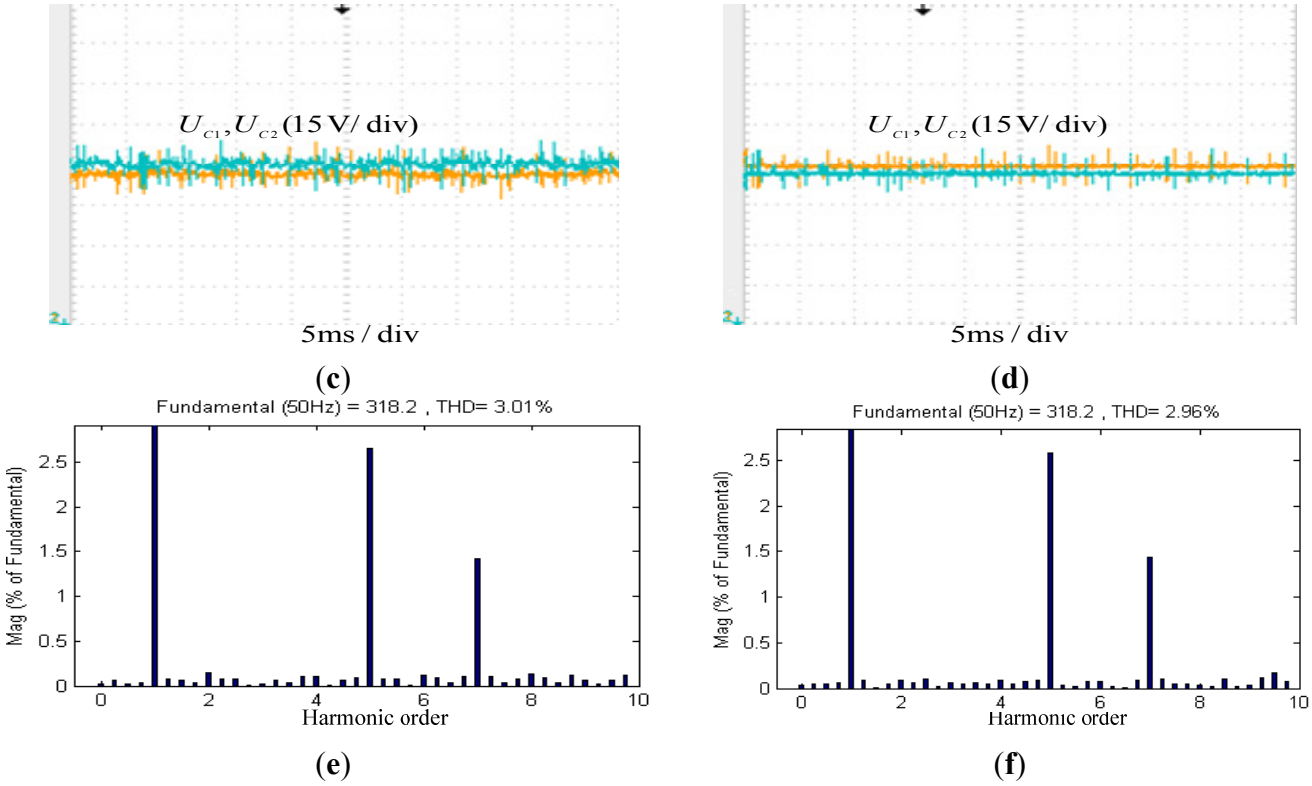


Figure 7. Experimental results of VSVM and VVSVM; (**a**) the line to line voltage and the load current in VSVM; (**b**) the line to line voltage and the load current in VVSVM; (**c**) balanced steady state of U_{C1} and U_{C2} in VSVM; (**d**) balanced steady state of U_{C1} and U_{C2} in VVSVM; (**e**) FFT (Fast Fourier Transformation) analysis of line-to-line voltage in VSVM; (**f**) FFT analysis of line-to-line voltage in VVSVM.

Comparing Figure 7c,d, the ripple amplitude of the capacitors voltage in VVSVM is smaller than that in VSVM. The FFT (Fast Fourier Transformation) analysis of the output line-to-line voltage with VSVM and VVSVM is illustrated in Figure 7e,f. THD of the VSVM is about 3.01% and the THD of VVSVM decreases to 2.96%. The 5th and 7th harmonics are included in three level wave of the line to line voltage in VSVM and VVSVM. Figure 8a,b shows the transient behavior of VSVM and VVSVM respectively, when the load varies abruptly. An asynchronous motor is used to verify the effectiveness of the proposed VVSVM in the case of varying load. A step change in the load is done, the asynchronous motor current varies from 7 to 20 A as shown in Figure 8. Since the asynchronous motor current can't vary abruptly in a very short time, thus, from Figure 8a,b, the balancing performance of the proposed VVSVM seems to be the same as that of VSVM. However, from the experimental results, the proposed VVSVM has better effectiveness of balancing voltage of DC-link capacitors compared to VSVM. It can be concluded that the capacitors voltage ripple is suppressed satisfactorily under the case of varying load when employing VVSVM.

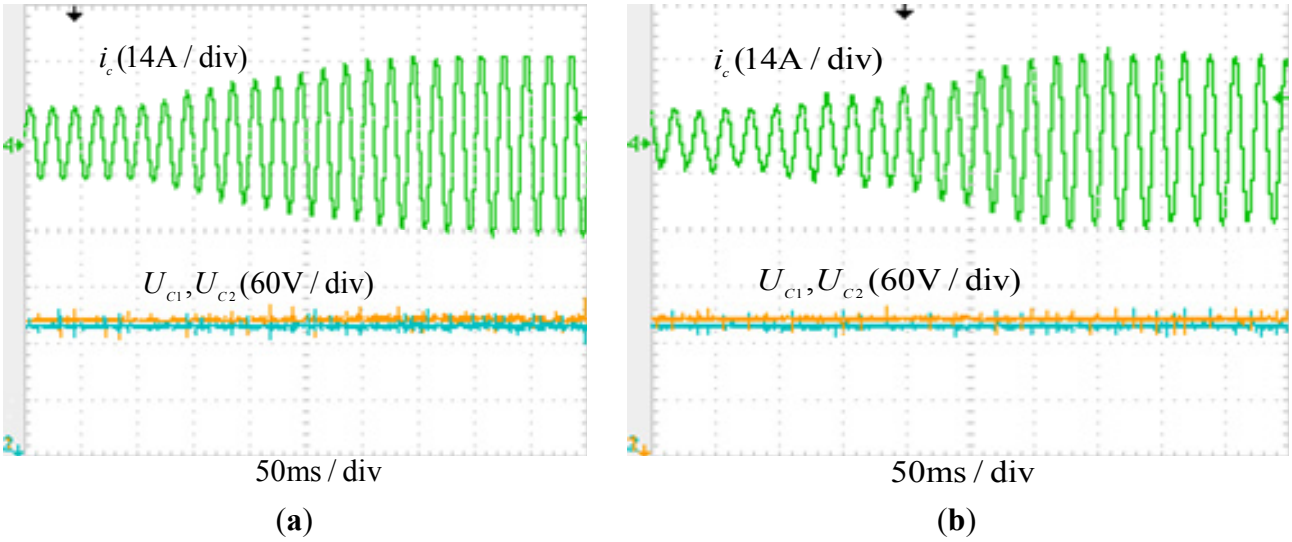


Figure 8. Experimental results of varying load. (**a**) VSVM; (**b**) VVSVM.

Figure 9a,b shows the experimental results of VSVM and VVSVM when the DC-link voltage is changed from 300 to 400 V. The figures show that the load current varies responding to changing DC-link voltage. From the analysis above, the neutral-point current flowing in/out of the capacitors is the only reason causing the capacitors' voltage unbalance, so the difference of balancing effectiveness in both VSVM and VVSVM is not very obvious in the case of varying DC-link voltage. However, from the experimental results, it can be seen that the proposed VVSVM is also able to maintain the neutral-point voltage balance in this case.

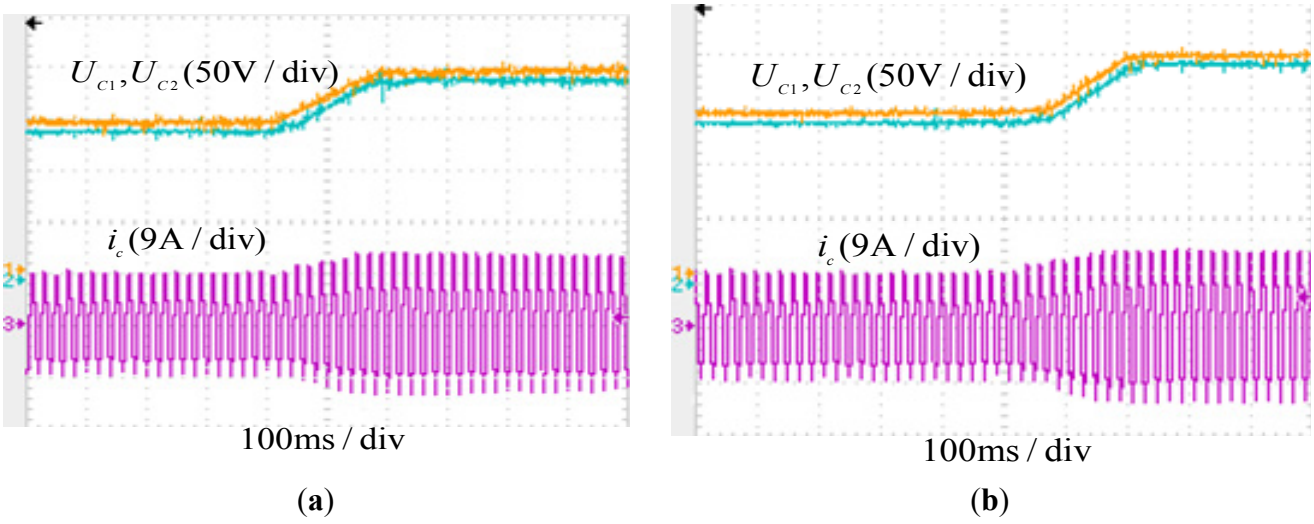


Figure 9. Experimental results of varying DC-link voltage. (**a**) VSVM; (**b**) VVSVM.

5. Conclusions

This paper proposed a VVSVM strategy for balancing the neutral-point voltage through adjusting the duty cycle of small vectors and regulating the current generated by virtual medium vectors. In the case of higher modulation index (m > 0.667), compared with VSVM which can't balance the neutral-point voltage in some vector regions (small region (5) in the paper), the proposed VVSVM can

perfectly keep the balance of neutral-point voltage in all the vector regions. Simulation and experiment show that when employing VVSVM, the balance of neutral-point voltage can be effectively maintained with less distortion of the output voltage, thus providing an effective strategy for high voltage applications.

Acknowledgments

The authors gratefully acknowledge Shanming Wan and Fang Wu for their work on the hardware setup. This project is supported by the National Natural Science Foundation of China under Grants 51377064 and 51407080.

Author Contributions

Shi Weng Gui conducted the theory analysis and the simulation. Shi Weng Gui and Zhen Jun Lin performed the experimental test, and Sheng Hua Huang designed the whole project and edited the manuscript.

Conflicts of Interest

The authors declare no conflict of interest.

References

1. Rodriguez, J.; Bernet, S.; Bin, W.; Pontt, J.O.; Kour, S. Multilevel voltage source converter for industrial medium voltage drives. *IEEE Trans. Ind. Electron.* **2007**, *54*, 2930–2945.
2. Chaves, M.; Margato, E.; Silva, J.F.; Pinto, S.F. New approach in back-to-back m-level diode-clamped multilevel converter modeling and direct current bus voltages balancing. *IEEE Trans. Power Electron.* **2010**, *3*, 578–589.
3. Nabae, A.; Takahashi, I.; Akagi, H. A new neutral-point clamped PWM inverter. *IEEE Trans. Ind. Appl*. **1981**, *5*, 518–523.
4. Rodriguez, J.; Bernet, S.; Steimer, P.K.; Lizama, I.E. A survey on neutral-point-clamped inverter. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2219–2230.
5. Ke, M.; Frede, B. The impact of power switching devices on the thermal performance of a 10 MW wind power NPC converter. *Energies* **2012**, *5*, 2559–2577.
6. Bendre, A.; Venkataramanan, G.; Rosene, D.; Srinivasan, V. Modeling and design of a neutral-point voltage regulator for a three-level diode-clamped inverter using multiple-carrier modulation. *IEEE Trans. Ind. Electron.* **2006**, *53*, 718–726.
7. Pou, J.; Zaragoza, J.; Ceballos, S.; Saeedifard, M.; Boroyevich, D. A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter. *IEEE Trans. Power Electron.* **2012**, *27*, 642–651.
8. Seo, J.H.; Choi, C.H.; Hyun, D.S. A new simplified space-vector PWM method for three-level inverters. *IEEE Trans. Power Electron.* **2001**, *16*, 545–550.
9. Chaturvedi, P.K.; Jain, S.; Agarwal, P. Reduced switching loss pulse width modulation technique for three-level diode clamped inverter technique for three-level diode clamped inverter. *IET Power Electron.* **2011**, *4*, 393–399.

10. Beig, A.R.; Narayanan, G.; Ranganathan, V.T. Modified SVPWM algorithm for three level VSI with synchronized and symmetrical waveforms. *IEEE Trans. Ind. Electron.* **2007**, *54*, 486–494.
11. Zhang, H.; Finney, S.J.; Massoud, A.; Williams, B.W. An SVM algorithm to balance the capacitor voltages of the three-level NPC active power filter. *IEEE Trans. Power Electron.* **2008**, *23*, 2694–2702.
12. Pou, J.; Pindado, R.; Boroyevich, D.; Rodriguez, P. Evaluation of the low frequency neutral-point voltage oscillation in three-level inverter. *IEEE Trans. Ind. Appl.* **2005**, *52*, 1582–1588.
13. Grigoletto, F.B.; Pinheiro, H. A space vector PWM modulation scheme for back-to-back three-level diode-clamped converters. In Proceedings of the Power Electronics Conference, 2009, COBEP'09, Bonito-Mato Grosso do Sul, Brazil, 27 September–1 October 2009; pp. 1058–1065.
14. Choi, U.-M.; Lee, K.B. Space vector modulation strategy for neutral-point voltage balancing in three-level inverter systems. *IET Power Electron.* **2013**, *6*, 1390–1398.
15. Busquets-Monge, S.; Bordonau, J.; Boroyevich, D.; Somavilla, S. The nearest three virtual space vector PWM—A modulation for the comprehensive neutral-point balancing in the three-level NPC inverter. *IEEE Power Electron. Lett.* **2004**, *2*, 11–15.
16. Busquets-Monge, S.; Somavilla, S.; Bordonau, J.; Boroyevich, D. Capacitor voltage balance for the neutral-point-clamped converter using the virtual space vector concept with optimized spectral performance. *IEEE Power Electron. Lett.* **2007**, *22*, 1128–1135.
17. Hu, C.; Wang, Q.; Li, G.; Feng, J.; Jiang, W. A neutral-point potential balancing algorithm for three-level inverter based on virtual-space-vector. *Trans. China Electrotech. Soc.* **2009**, *24*, 100–107.
18. Xia, C.; Shao, H.; Zhang, Y.; He, X. Adjustable proportional hybrid SVPWM strategy for neutral-point-clamped three-Level inverters. *IEEE Trans. Ind. Electron.* **2013**, *60*, 4234–4241.
19. Zhang, Y.; Zhao, Z.; Zhu, J. A hybrid PWM applied to high-power three-level inverter-fed induction-motor drives. *IEEE Trans. Ind. Electron.* **2011**, *58*, 3409–3420.
20. Jiang, W.D.; Du, S.W.; Chang, L.C.; Zhang, Y.; Zha, Q. Hybrid PWM strategy of SVPWM and VSVPWM for NPC three-level voltage-source inverter. *IEEE Trans. Power Electron.* **2010**, *25*, 2607–2619.
21. Govindaraju, C. Efficient sequential switching hybrid modulation techniques for multiphase multilevel inverters. *IET Power Electron.* **2011**, *4*, 557–569.
22. Das, S.; Narayanan, G. Novel switching sequences for a space-vector-modulated three-level inverter. *IEEE Trans. Ind. Electron.* **2012**, *59*, 1477–1487.