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Promise and Challenges of High-Voltage SiC Bipolar Power Devices

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Abstract: Although various silicon carbide (SiC) power devices with very high blocking voltages over 10 kV have been demonstrated, basic issues associated with the device operation are still not well understood. In this paper, the promise and limitations of high-voltage SiC bipolar devices are presented, taking account of the injection-level dependence of carrier lifetimes. It is shown that the major limitation of SiC bipolar devices originates from band-to-band recombination, which becomes significant at a high-injection level. A trial of unipolar/bipolar hybrid operation to reduce power loss is introduced, and an 11 kV SiC hybrid (merged pin-Schottky) diodes is experimentally demonstrated. The fabricated diodes with an epitaxial anode exhibit much better forward characteristics than diodes with an implanted anode. The temperature dependence of forward characteristics is discussed.

Keywords: silicon carbide; power device; carrier lifetime; conductivity modulation; merged pin-Schottky (MPS) diodes

1. Introduction

Silicon carbide (SiC) has received increasing attention as a wide bandgap semiconductor well suited for high-voltage power devices. The promise of SiC power devices stems from its superior physical properties and rapid progress in growth and device technologies [1–5]. SiC (4H polytype) unipolar devices such as metal-oxide-semiconductor field effect transistors (MOSFETs) and Schottky barrier diodes (SBDs) with blocking voltages of 600–1700 V have been commercialized, demonstrating substantial reduction of power loss in various power conversion systems. Higher-voltage (3.3–6.5 kV) SiC power MOSFETs have currently been developed [6–8], and 15 kV SiC MOSFETs have also been demonstrated [8]. These very high-voltage SiC MOSFETs can be fabricated with process technology similar to that used for 1 kV-class SiC MOSFETs, though some modifications are required in the cell design and termination structure. However, the specific on-resistance (R_{on}) of power MOSFETs significantly increases with increasing the blocking voltage (V_B), following the relationship of $R_{on} \sim V_B^{2.2–2.5}$. The on-resistance further increases at elevated temperature due to the mobility drop. For ultrahigh-voltage (>10 kV) power devices, SiC bipolar devices are promising, because the resistance of the thick voltage-blocking layer can remarkably be reduced by the conductivity modulation effect, and the on-resistance exhibits a very small temperature dependence [9]. A drawback of bipolar devices is, of course, the slower switching speed and thereby the increased switching loss. Thus, the choice of unipolar/bipolar devices must be carefully determined taking account of the operation condition required for individual applications [10]. Another weak point of SiC bipolar devices is the large built-in potential caused by the wide bandgap of SiC (3.26 eV). Thus, a forward voltage drop of about 2.8 V is required before significant current flows in SiC bipolar devices except for bipolar junction transistors. This large built-in voltage (knee voltage) naturally results in a relatively high forward voltage drop at low current density.

In recent years, ultrahigh-voltage SiC pin diodes [11–13], thyristors [14], bipolar junction transistors [15], and insulated-gate bipolar transistors (IGBTs) [16–18] have been reported. Using 10 kV SiC MOSFETs or 15 kV SiC IGBTs, several power converters such as boost converters and modular-leg converters have been fabricated, demonstrating good power efficiencies [19–22]. The major technological challenges for development of ultrahigh-voltage SiC bipolar devices include fast epitaxial growth, reduction of extended defects, control of carrier lifetimes, surface passivation, and packages. The most critical concern about the reliability of SiC bipolar devices is degradation caused by expansion of single-Shockley stacking faults, which nucleate from basal plane dislocations when excess carriers are injected and recombine [23,24]. Elimination of basal plane dislocations in SiC wafers is one of the most important challenges for commercialization of SiC bipolar power devices. Furthermore, development of ultrahigh-voltage packages is another challenge. Although some packages and modules with special insulating materials have been reported for such high-voltage devices [25,26], the ultrahigh-voltage package technology is still not mature.

Though the performances of these devices and converters reported are promising, the ideal characteristics limited by the intrinsic material properties of SiC have not been well studied. In the first part of this paper, the forward characteristics of SiC pin diodes having different thickness of i-layer (voltage-blocking layer) are simulated, and the major intrinsic limitations are discussed. Although 10–30 kV-class SiC pin diodes exhibit good characteristics when the carrier lifetime is long, the forward voltage drop significantly increases when the breakdown voltage exceeds 50–60 kV. It is shown that this limitation originates from the band-to-band recombination in SiC, being an inherent limitation of SiC. In the second part, a trial of unipolar/bipolar hybrid operation with SiC pin diodes is described. The characteristics of merged pin-Schottky (MPS) diodes having epitaxial junction and implanted junction are compared. The epitaxial MPS diodes show good hybrid operation as expected and a high breakdown voltage of 11.3 kV is demonstrated by adopting an appropriate junction termination.

2. Results

2.1. Simulation of Forward Characteristics of Ultrahigh-Voltage SiC Pin Diodes

Figure 1 shows the structure of a SiC pin diode simulated in this study. The anode is 5 μm-thick, doped to 5×10^{20} cm^{-3}, and the cathode (n^+-layer beneath the i-layer) is 10 μm-thick, doped to 5×10^{18} cm^{-3}. These structures were optimized to achieve highest carrier-injection efficiencies (for example, see Figure S1). Although a higher doping concentration is generally desirable to enhance the injection efficiency, one should consider bandgap narrowing [27]. When the doping concentration becomes too high, a bandgap narrowing phenomenon occurs for the anode or cathode, which remarkably decreases the injection efficiency. Furthermore, when the thickness of the anode or cathode is not enough, the carrier recombination at the anode/cathode contact becomes significant and this recombination increases the minority-carrier current inside the anode/cathode, leading to the decreased injection efficiency [28]. Therefore, the anode and cathode structures were fixed and the thickness of i-layer was varied in this study. The i-layer was a lightly-doped n-type epilayer with a donor concentration of 1×10^{14} cm^{-3}, which is technically achievable with the current technology. Since the switching frequency in ultrahigh-voltage power converters is usually low, the major component of power loss in semiconductor devices is the on-state loss. Thus, the forward characteristics of SiC pin diodes were mainly investigated in this study. In recent years, elimination of carrier-lifetime killers has been reported [29,30] and the carrier lifetime of n-type SiC has substantially been improved from about 1–2 μs (as-grown) to 30 μs or even longer [31,32]. In this study, the forward characteristics were simulated by changing the carrier lifetime in a wide range.

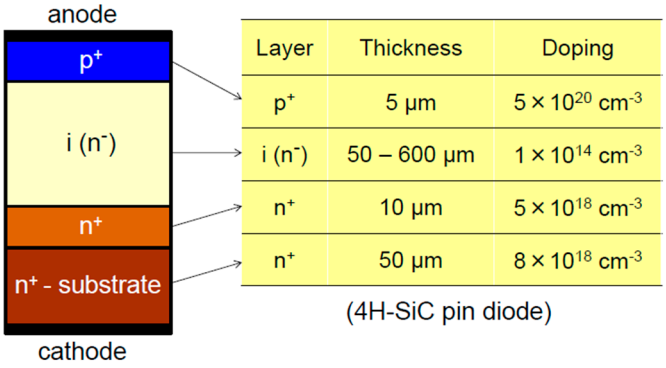

Figure 1. Schematic structure of a SiC pin diode simulated in this study.

Figure 2 depicts the i-layer thickness dependence of breakdown voltage for SiC pin diodes having the structure shown in Figure 1. The breakdown voltage almost linearly increases with the i-layer thickness, because the doping concentration of the i-layer is low and the diodes are of complete punchthrough structure. However, the breakdown voltage shows a slight saturation trend when the thickness exceeds 300 μm, where the electric field strength at the end of the i-layer (space charge region) becomes significantly lower than that at the junction interface. Roughly speaking, the diodes with an i-layer thickness of 100, 300, and 500 μm are 15, 40, and 58 kV-class, respectively.

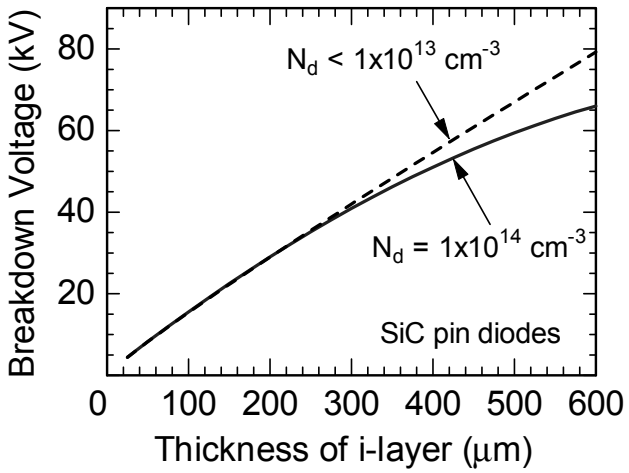

Figure 2. Dependence of breakdown voltage for SiC pin diodes on i-layer thickness. The solid and dashed lines denote the results for the i-layer doping concentration of 1×10^{14} cm^{-3} and $<1 \times 10^{13}$ cm^{-3}, respectively.

As a typical example, the forward characteristics of SiC pin diodes having an i-layer thickness of 200 μm (28 kV class) are presented in Figure 3, where the carrier lifetime in the i-layer was changed from 1 μs to 100 μs (an analytical expression for the characteristics of a pin diode and brief discussion are given in Note S1). As expected, the characteristics are remarkably improved by increasing the carrier lifetime, which is consistent with the studies on lower-voltage SiC pin diodes reported in literature [33,34]. Note that the carrier lifetimes longer than 10 μs do not contribute very much to reduction of the forward voltage drop. For example, the forward voltage drop at a current density of 100 A/cm^2 is reduced from 3.93 V to 3.20 V by increasing the carrier lifetime from 1 μs to 10 μs. However, improvement of the forward voltage drop is marginal when the lifetime is further increased to 20 μs or longer.

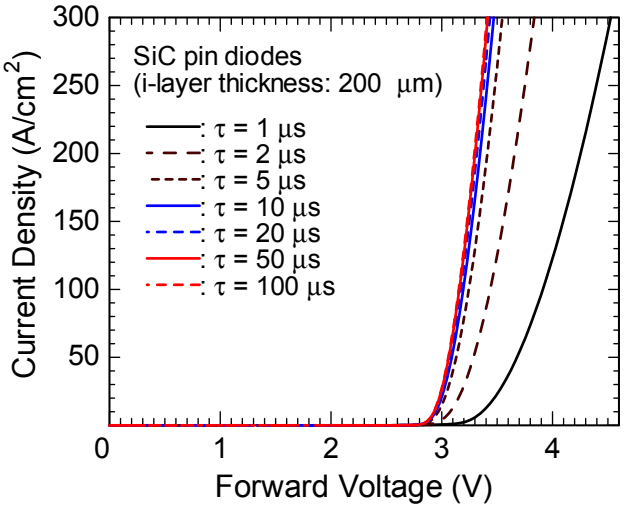

Figure 3. Forward characteristics of SiC pin diodes having an i-layer thickness of 200 μm (28 kV class). The carrier lifetime in the i-layer was changed from 1 μs to 100 μs.

Figure 4 shows the forward characteristics of SiC pin diodes having different i-layer thicknesses from 100 μm (15 kV class) to 600 μm (65 kV class). Here the carrier lifetime was fixed at 50 μs. The diode with an i-layer thickness of 100 μm exhibits nearly ideal characteristics; The differential on-resistance is as low as 0.76 mΩcm^2 and the forward voltage drop is 3.02 V at 100 A/cm^2. Since the on-resistance include a substrate resistance of 0.08 mΩcm^2, the actual differential on-resistance of the thick i-layer is estimated to be about 0.68 mΩcm^2. However, the on-resistance and forward voltage drop considerably increase to 12.2 mΩcm^2 and 4.62 V, respectively, for the diode having a 600 μm-thick i-layer, even though the lifetime is as long as 50 μs.

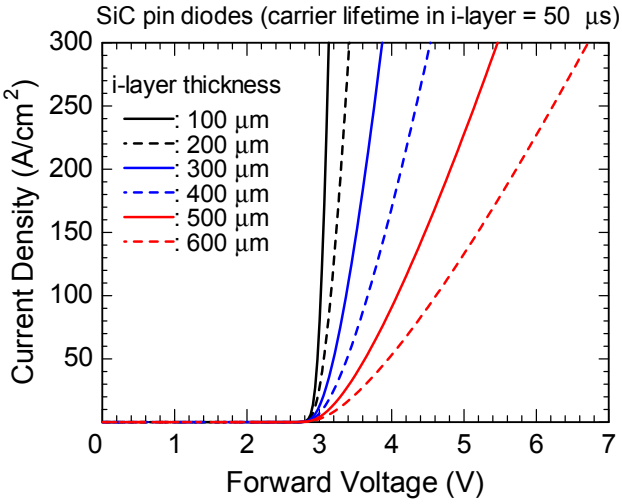

Figure 4. Forward characteristics of SiC pin diodes having different i-layer thicknesses from 100 μm (15 kV class) to 600 μm (65 kV class). Here the carrier lifetime was fixed at 50 μs.

Figure 5 demonstrates the i-layer thickness dependence of the forward voltage drop at a current density of 100 A/cm^2 for SiC pin diodes, where the carrier lifetime in the i-layer was varied from 1 μs to 200 μs (the lifetime dependence of the forward voltage drop can be seen in Figure S2). The right axis indicates the density of on-state loss at 100 A/cm^2. For a given carrier lifetime, the forward voltage drop monotonically increases with increasing the i-layer thickness. As in the case of Figure 3, reduction of forward voltage drop is not very significant when the carrier lifetime becomes very

long (>50 μs). To clarify the conductivity modulation of high-voltage SiC pin diodes, the profiles of excess carrier concentration inside the i-layer at a current density of 100 A/cm^2 are plotted in Figure 6. Here the diode with a 600 μm-thick i-layer was considered and the carrier lifetime was varied from 5 μs to 200 μs. The excess carrier concentration is significantly higher than the background carrier concentration in the i-layer (1×10^{14} cm^{-3}) even for the case of a relatively short lifetime (5 μs), and it increases with increasing the carrier lifetime. However, the excess carrier concentration does not show further increase very much when the carrier lifetime exceeds 50 μs, which is the main reason why improvement of the forward characteristics is almost saturated for very long carrier lifetime as shown in Figure 5. This result identifies the major limitation of SiC pin diodes (and other bipolar devices) in terms of the on-state loss and its origin is discussed in Section 3.

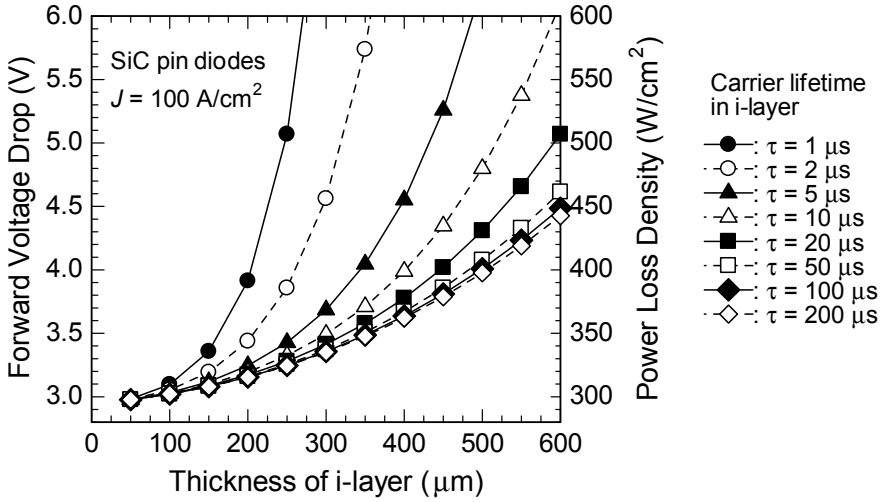

Figure 5. Dependence of the forward voltage drop at a current density of 100 A/cm^2 for SiC pin diodes on the i-layer thickness. Here the carrier lifetime in the i-layer was varied from 1 μs to 200 μs. The right axis indicates the density of on-state loss at 100 A/cm^2.

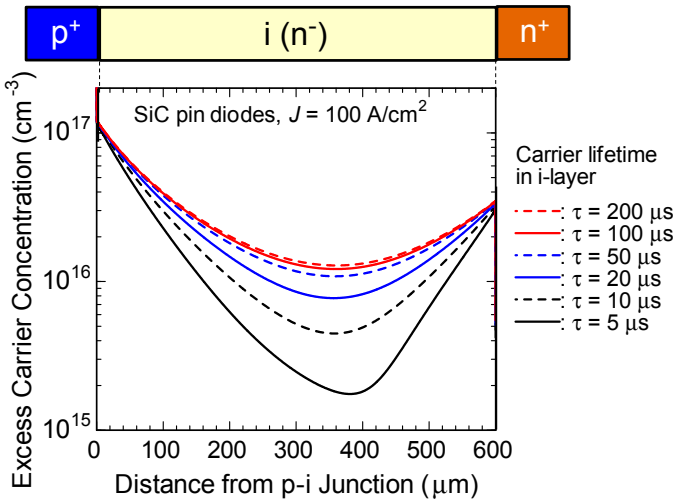

Figure 6. Profiles of excess carrier concentration inside the i-layer at a current density of 100 A/cm^2 for a SiC pin diode. The i-layer thickness is 600 μm and the carrier lifetime was varied from 5 μs to 200 μs.

2.2. Characteristics of Ultrahigh-Voltage SiC Merged Pin-Schottky (MPS) Diodes

As shown in Figure 4, a relatively large knee voltage of about 2.8 V is a major drawback of SiC pin diodes (and other bipolar devices except bipolar junction transistors). The high knee voltage originates

from the large built-in potential of a pn junction in SiC and is an inherent characteristic, which is caused by the wide bandgap (3.26 eV). Since the forward voltage drop of SiC pin diodes is never smaller than 2.8 V at room temperature, the on-state loss of SiC pin diodes can be larger than that of SiC Schottky barrier diodes in the case of partial load (relatively low current density). To overcome this issue, merged pin-Schottky (MPS) diodes have been proposed in Si [35] and then this device concept has been employed to reduce the leakage current caused by tunneling as well as to enhance the surge current capability of SiC Schottky barrier diodes (SBD) [36,37]. In this study, high-voltage SiC MPS diodes, the junction of which was fabricated by either epitaxial growth or ion implantation, were fabricated and tested to reduce the forward voltage drop at relatively low current density. Figure 7 illustrates the schematic structures of SiC MPS diodes fabricated in this study. The main junction was formed by either (a) epitaxial growth or (b) Al^+ ion implantation. Due to the difference in junction formation, the "epitaxial" MPS diode has a mesa structure (Figure 7a), while the "implanted" MPS diode does a planar structure (Figure 7b). The details of fabrication process are described in Section 4.

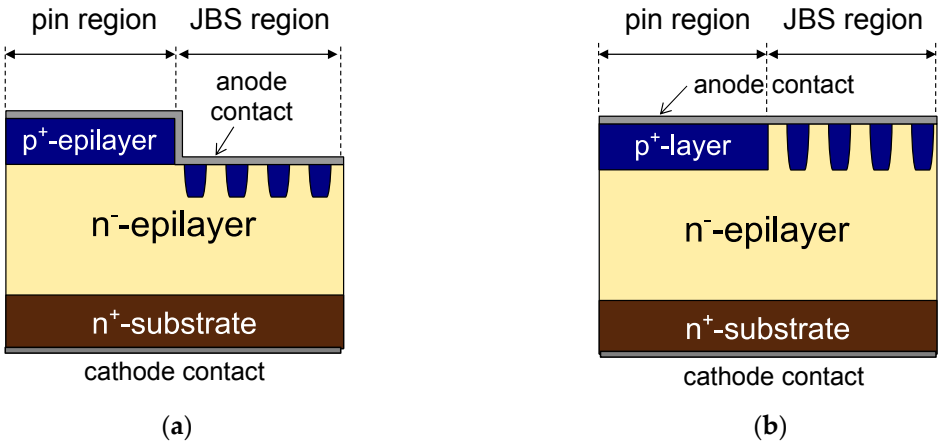

Figure 7. Schematic structures of SiC MPS diodes fabricated in this study. The main junction was formed by either (**a**) epitaxial growth or (**b**) Al^+ ion implantation. The widths of the pin and JBS (Junction-Barrier Schottky) regions were both 150 μm and of a stripe-like geometry. The active area was 3.6×10^{-3} cm^2.

Figure 8 depicts the forward characteristics for two types of SiC MPS diodes (epitaxial or implanted anode) fabricated in this study. In both diodes, the current starts to flow at a forward voltage of 0.9 V, which corresponds to the knee voltage of Ti/SiC Schottky barrier diodes. From the semilogarithmic plots of forward characteristics, the barrier height of Ti Schottky was estimated as 1.12 eV, which is consistent with a previous report [38]. The differential on-resistance in this unipolar operation was approximately 85–100 $m\Omega cm^2$ irrespective of the formation process of the main junction (anode). This on-resistance is slightly higher than but reasonably agrees with the drift resistance calculated from the structure of a lightly-doped n-type epilayer. The epitaxial MPS diode exhibited the second knee voltage at about 3.2 V, which means the onset of bipolar operation caused by minority-carrier injection. Above this second knee voltage, the differential on-resistance was remarkably reduced by the conductivity modulation effect and it reaches 14.9 $m\Omega cm^2$ at a current density of 100 A/cm^2. On the other hand, the implanted MPS diode did not show a clear "second knee voltage" and the current density gradually increased and the differential on-resistance slowly decreased with the current. As a result, the forward voltage drop at 100 A/cm^2 was much smaller for the epitaxial MPS diode (4.65 V) than for the implanted MPS diode (7.81 V). Therefore, SiC epitaxial MPS diodes are promising because the forward voltage drop can be remarkably reduced at relatively low current density ("partial load" condition) compared with SiC pin diodes and the voltage drop at high current density is much lower than that of a SiC Schottky barrier diode with the same breakdown

voltage, though the forward voltage at high current density is slightly higher than that of a pure SiC pin diode (For comparison, see Figure S3).

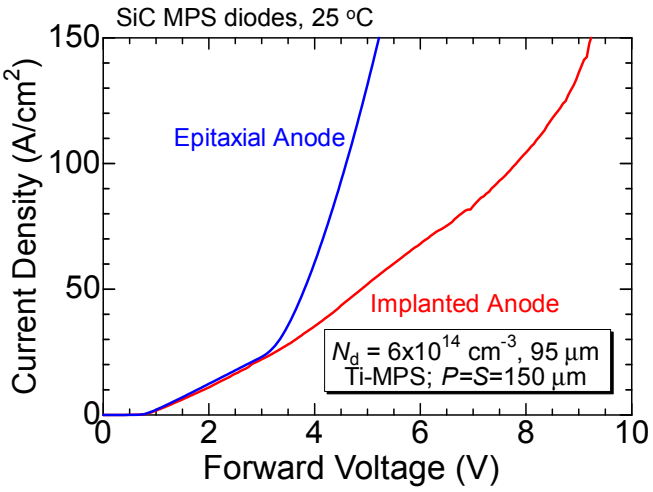

Figure 8. Forward characteristics for two types (epitaxial or implanted anode) of SiC MPS diodes fabricated in this study. The widths of the pin-region (*P*) and JBS region (*S*) were both 150 µm.

Figure 9 shows the forward characteristics of (a) epitaxial and (b) implanted MPS diodes at different temperatures from 25 to 300 °C. In both diodes, the current density in the unipolar operation at a given forward voltage (below 2.5 V) decreased at elevated temperature, which is similar to the characteristics of Schottky barrier diodes. In the bipolar operation, the knee voltage gradually decreased with elevating the temperature, leading to higher current density at high temperature. This phenomenon is naturally expected because the built-in potential of a pn junction declines when the temperature is elevated. The increase of current density in the bipolar operation by increasing the temperature is more significant for the implanted MPS diode compared with the epitaxial MPS diode, and the characteristics of the implanted MPS diode gradually approach those of the epitaxial MPS diode at high temperature. However, the epitaxial MPS diode showed better performance even at 300 °C. More quantitative analyses are described in the next section.

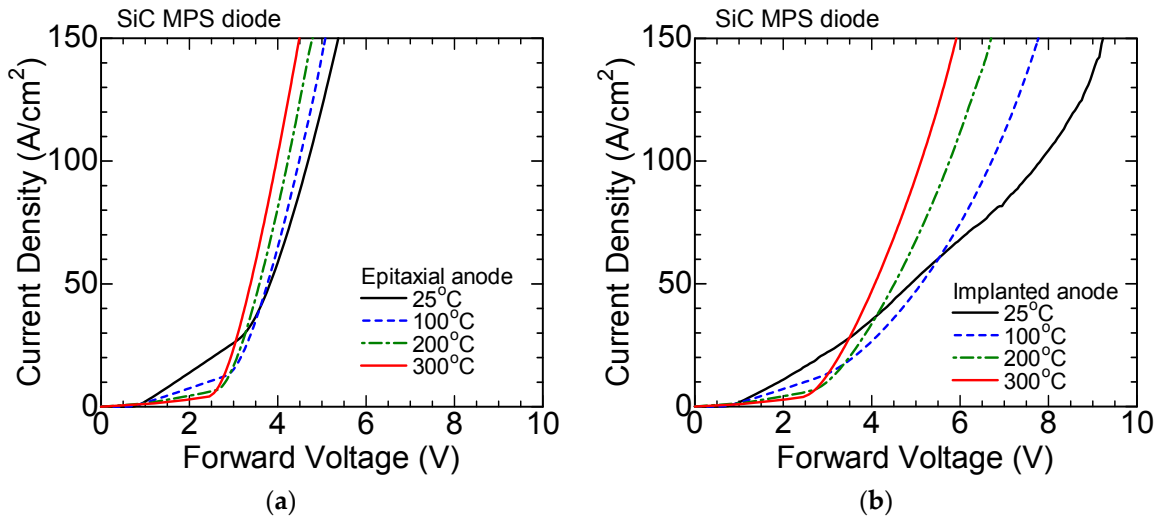

Figure 9. Forward characteristics of (**a**) epitaxial and (**b**) implanted SiC MPS diodes at different temperatures from 25 to 300 °C.

The reverse characteristic of a fabricated SiC MPS diode is shown in Figure 10, where the current-voltage curve of an epitaxial MPS diode was measured by a high-voltage DC sweep. The diode exhibited a very high breakdown voltage of 11.3 kV, which is about 90% of the ideal parallel-plane breakdown voltage determined by the epilayer structure. As far as the blocking performance is concerned, there is not a significant difference between the epitaxial and implanted MPS diodes, because the breakdown occurs in the JTE region for the diodes fabricated in this study (The i-layer structure and the JTE region are almost identical for both the diodes).

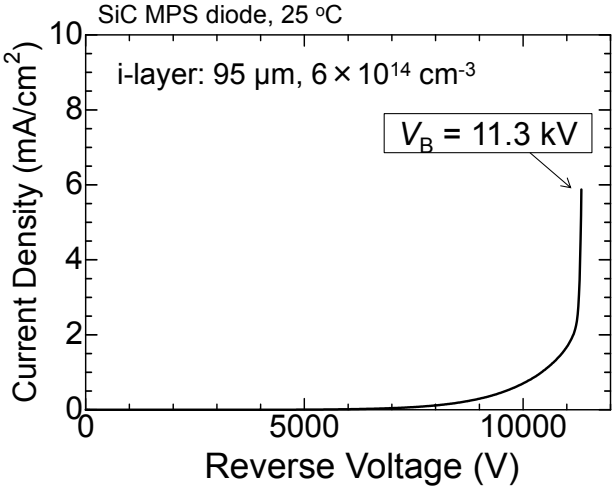

Figure 10. Reverse characteristic of a SiC epitaxial MPS diode fabricated in this study.

3. Discussion

3.1. Limitation of Ultrahigh-Voltage SiC Bipolar Devices

As shown in Figures 5 and 6, the major limitation of ultrahigh-voltage SiC pin diodes is the large forward voltage drop and high differential on-resistance when the i-layer thickness becomes very thick (for example, 600 μm (65 kV class)). The forward characteristics are not improved even if an extremely long carrier lifetime over 100 μs is assumed. Therefore, recombination paths of excess carriers are analyzed and discussed in this subsection. It should be noted that the carrier lifetime employed in the simulation is so-called Shockley-Read-Hall (SRH) lifetime (τ_{SRH}) determined by indirect recombination via deep levels. In a semiconductor, band-to-band (direct) and Auger recombinations also take place, and these recombination processes must be taken into account especially when the excess carrier concentration is high [39]. Thus, the decay of excess carrier concentration in SiC was theoretically analyzed.

Recombination of excess carriers in n-type semiconductor can be expressed by the following differential equation [39]:

$$\frac{d\Delta n}{dt} = -\frac{\Delta n}{\tau_{SRH}} - B(n_0 + p_0 + \Delta n)\Delta n - C_n({n_0}^2 + 2n_0\Delta n + \Delta n^2)\Delta n - C_p({p_0}^2 + 2p_0\Delta n + \Delta n^2)\Delta n \quad (1)$$

here, Δn, n_0, and p_0 are the excess carrier concentration, the equilibrium electron concentration (1×10^{14} cm^{-3} in the present case), and the equilibrium hole concentration, respectively. Regarding the carrier recombination, SRH recombination (τ_{SRH}), band-to-band (direct) recombination (coefficient: B), and Auger recombination (coefficients: C_n, C_p) were considered. The SRH lifetime was assumed to be independent of the excess carrier concentration. Table 1 summarizes these parameters employed in this analysis [40]. Both the SRH lifetime and the initial excess carrier concentration were varied in wide ranges, and the time decay of the excess carrier concentration was calculated.

Table 1. Carrier recombination coefficients used in the calculation [40].

Parameter	Value	Unit
B	1.5×10^{-12}	cm^3/s
C_n	5.0×10^{-31}	cm^6/s
C_p	2.0×10^{-31}	cm^6/s

Figure 11a shows the decay curves of the excess carrier concentration in n-type SiC having a long SRH lifetime of 100 μs. A relatively fast decay is observed when the initial excess carrier concentration is high. For each decay curve, the differential slope was calculated and defined as the effective carrier lifetime (τ_{eff}). Figure 11b depicts the effective carrier lifetime as a function of time for several different initial excess carrier concentrations from 1×10^{14} cm^{-3} to 1×10^{18} cm^{-3}.

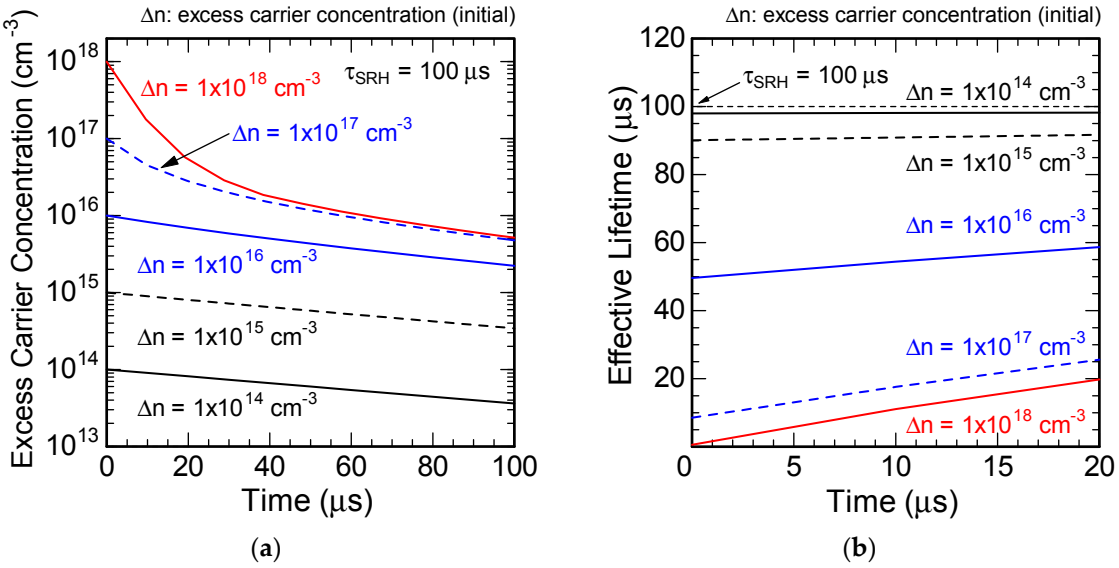

Figure 11. (**a**) Decay curves of the excess carrier concentration in n-type SiC having a long SRH lifetime of 100 μs for several different initial excess carrier concentrations from 1×10^{14} cm^{-3} to 1×10^{18} cm^{-3}; (**b**) Effective carrier lifetime as a function of time for several different initial excess carrier concentrations.

When the excess carrier concentration is relatively low, 1×10^{15} cm^{-3}, the effective lifetime is 90–92 μs, close to the SRH lifetime (100 μs). However, the effective lifetime at the initial decay drops drastically with increasing the excess carrier concentration and it reaches 8.5 μs at 1×10^{17} cm^{-3} and 0.6 μs at 1×10^{18} cm^{-3}. Figure 12 plots the effective carrier lifetime as a function of the excess carrier concentration calculated in this study.

Results for different SRH lifetimes from 2 μs to 200 μs are shown, and the lifetimes limited purely by band-to-band (direct) recombination and Auger recombination are indicated by dashed and dotted lines, respectively. It is well known that direct and Auger recombinations become significant when the carrier concentration is very high. As shown in Figure 12, however, the direct recombination severely affects the effective carrier lifetime even at a relatively low excess carrier concentration of 1×10^{16} cm^{-3} when the SRH lifetime is very long (>50 μs). In such a case, the effective carrier lifetime is mainly limited not by SRH recombination but by direct recombination. This situation is more pronounced as the SRH lifetime becomes longer. The ambipolar diffusion constant (D_a) and ambipolar diffusion length (L_a) of excess carriers are given by the following equations:

$$D_a = \frac{n+p}{n/D_n + p/D_p}, \quad (2)$$

$$L_a = \sqrt{D_a \tau_{eff}}. \quad (3)$$

where n and p are the electron concentration ($n = n_0 + \Delta n$) and hole concentration ($p = p_0 + \Delta n$), respectively. D_n and D_p are the diffusion constants of electrons and holes, respectively. Based on Figures 11 and 12, the ambipolar diffusion length can be estimated to be 210 μm at an excess carrier concentration of 1×10^{15} cm^{-3}, 140 μm at 1×10^{16} cm^{-3}, and decreased to 45 μm at 1×10^{17} cm^{-3} for a SRH lifetime of 100 μs. Since the excess carrier concentration inside the i-layer of a pin diode is in the 10^{16}–10^{17} cm^{-3} range at high current density (Figure 6), the ambipolar diffusion length at such current density is almost saturated at about 50–150 μm, even if all the defects can be eliminated. The estimated ambipolar diffusion length (about 100 μm) is sufficiently long to highly modulate a 200 μm-thick i-layer [35] but not enough for a 600 μm-thick i-layer. As discussed above, this limitation originates from band-to-band (direct) recombination in SiC, which is an intrinsic property of the material. Thus, band-to-band recombination is the major factor which inherently limits the performance of ultrahigh-voltage SiC pin diodes and possibly other bipolar devices.

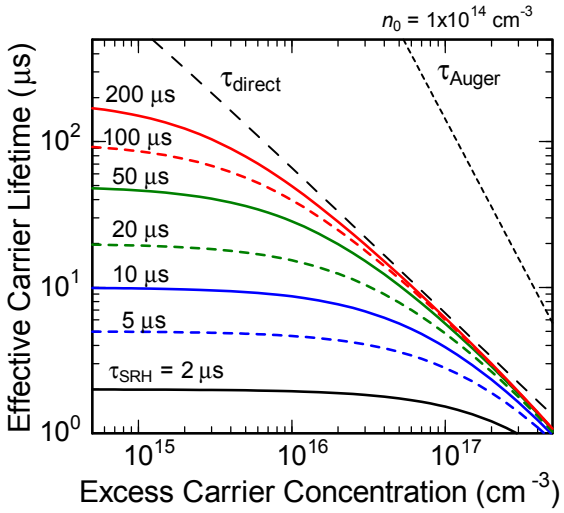

Figure 12. Effective carrier lifetime in SiC as a function of the excess carrier concentration.

As a future work, it is important to predict the limitation of SiC pin diodes in the wide temperature range, especially at high temperature. To this end, basic studies on the temperature dependence of carrier recombination coefficients (both band-to-band and Auger recombinations) are essential.

3.2. Comparison of SiC MPS Diodes Formed by Epitaxial Growth and Ion Implantation

Based on the results shown in Figure 9, the differential on-resistances in the (a) unipolar and (b) bipolar operations were determined at each temperature and are plotted in Figure 13. Here the differential on-resistance was defined at a forward voltage of 2 V for the unipolar operation and at a current density of 100 A/cm^2 for the bipolar operation. As shown in Figure 13a, the unipolar on-resistance is almost independent of the type of MPS diodes, namely epitaxial or implanted junctions, though the epitaxial MPS diode exhibited slightly lower on-resistance. Since the i-layer (lightly-doped n-type epilayer) is very thick (95 μm), the impact of implantation-induced damage, which is created inside the implanted p-type anode as well as near the implantation tail [41], is very small, as far as the majority carrier conduction is concerned. Thus, the differential on-resistance in the unipolar operation should be determined simply by the bulk resistance of the very thick n-type epilayer. This is the reason why the difference in the unipolar on-resistance between epitaxial and implanted MPS diodes was very small. The increase of the unipolar on-resistance at elevated temperature is ascribed to the decrease of electron mobility due to enhanced phonon scattering. The temperature dependence of the unipolar

on-resistance shown in Figure 13a is consistent with the temperature dependence of electron mobility in lightly-doped n-type SiC [4].

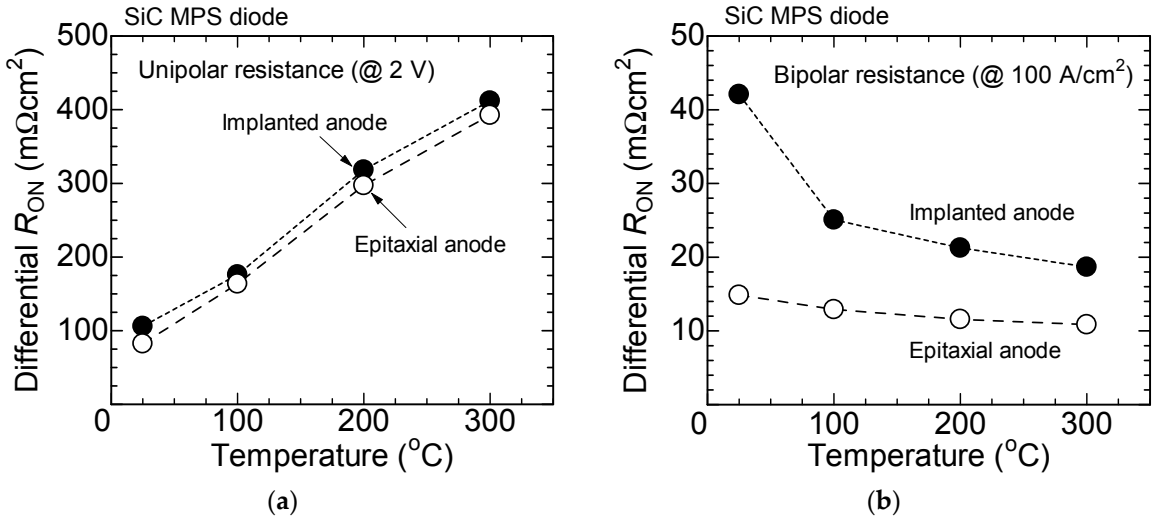

Figure 13. Differential on-resistances of fabricated SiC MPS diodes in the (**a**) unipolar and (**b**) bipolar operations at different temperatures. The results for epitaxial and implanted MPS diodes are shown.

In contrast, a definite difference was observed for the differential on-resistance in the bipolar operation. As shown in Figure 13b, the bipolar on-resistance is reduced at high temperature, which can be attributed to the increased carrier lifetime and the enhanced injection efficiency of holes from the p-type anode to the lightly-doped n-type epilayer. The latter is naturally expected owing to the increased ionization of Al acceptors at elevated temperature, which are energetically deep in SiC. Since a high density of deep levels and extended defects are generated inside the p-type anode and near the main junction by ion implantation and subsequent annealing, the carrier lifetime is substantially shortened in these regions. The short charrier lifetime near the main junction kills the injection efficiency, leading to considerable decrease of the conductivity modulation effect and thereby to the increased differential on-resistance of the implanted MPS diode. This result is consistent with a report on 4.5 kV SiC pin diodes formed by implantation [42]. When the carrier lifetime in the i-layer is long enough, the differential on-resistance of a pin diode is low and its temperature dependence is small [9], which is the major reason why the bipolar on-resistance of the epitaxial MPS diode in this study was much lower and showed the small temperature dependence. However, the increase of carrier lifetime at elevated temperature significantly contributes to the conductivity modulation and to decrease of the differential on-resistance when the carrier lifetime is short, because the conductivity of more and more region inside the i-layer is modulated with increasing the temperature. This trend is more significant for the bipolar on-resistance of the implanted MPS diodes as shown in Figure 13b.

Since a potential of unipolar/bipolar hybrid operation could be demonstrated with high-voltage SiC diodes in this study, monolithic integration of SiC vertical power MOSFET and IGBT is an attractive challenge. Since MOSFETs exhibit no knee voltage in the on-state characteristics, remarkable reduction of on-state loss can be expected by the hybrid operation of MOSFET and IGBT. However, the unipolar on-resistance becomes unacceptably high for extremely high-voltage devices and at high temperature. Thus, such hybrid devices must have severe limitations when the breakdown voltage is higher than 20 kV or the operation temperature exceeds 200 °C. The proposed hybrid MOSFET-IGBT devices will be promising for 8–15 kV switching devices.

4. Materials and Methods

For simulation of SiC pin diodes, a commercial device simulator, a Synopsis TCAD-Sentaurs device [43], was used. The standard set of physical properties of 4H-SiC embedded in the simulator was employed. In the simulation, incomplete ionization of dopants (nitrogen donors and aluminum acceptors) and a bandgap narrowing effect for heavily-doped materials were taken into account. In simulation of SiC pin diodes, accurate models for the carrier statistics and basic transport properties of SiC are included. However, the injection-level dependence of SRH carrier lifetime and carrier-carrier scattering are not known in SiC. Therefore, we assumed an injection-level independent SRH lifetime and neglected carrier-carrier scattering. These assumptions induce certain inaccuracy in the present simulation. Establishment of these physical models is an important subject of study in the future.

In the simulation, a heavily-doped n-type SiC substrate was assumed beneath the active pin diode. The thickness and resistivity of the substrate were 50 μm and 0.016 Ωcm, respectively, where the substrate thinning was considered because the active region (mainly i-layer) is very thick. The contact resistivity for the anode and cathode was neglected for simplicity. For calculating the ideal breakdown voltage, a latest set of impact ionization coefficients [44] was employed. The diode temperature was fixed at room temperature (300 K) in all the simulations.

In fabrication of SiC MPS diodes, a 95 μm-thick n-type epilayer grown on a heavily doped n-type substrate was used as a starting material. The n-type epilayer was intentionally doped with nitrogen to 6×10^{14} cm^{-3}. Before formation of the p-type anode, thermal oxidation at 1400 °C for 48 h was performed to enhance the carrier lifetime [30,32]. The low-injection carrier lifetime can be increased from 2 μs to about 30 μs by this process. After removal of the formed oxide, the anode region was formed by either epitaxial growth or Al^+ implantation. In the case of epitaxial growth, the anode consists of two p-type layers, 2.0 μm-thick layer doped to 1×10^{19} cm^{-3} and 0.2 μm-thick layer doped to 1×10^{20} cm^{-3} (top). After epitaxial growth of the p-type anode, sloped mesas were formed for device isolation by fluorine-based reactive ion etching using SiO_2 as an etching mask [45]. In the case of implanted junctions, a 0.8 μm-deep box profile with the dopant concentration of 2×10^{18} cm^{-3} was formed by Al^+ implantation (implant energy: 270–700 keV). Higher-dose Al^+ implantation was carried out to form a 0.2 μm-thick heavily-doped surface layer (dopant concentration: 2×10^{20} cm^{-3}) for improving the contact resistivity. Along the periphery of a diode, a 500 μm-long space-modulated junction termination extension (JTE) structure was formed by Al^+ implantation [13]. All the implanted dopants were activated by annealing at 1650 °C for 20 min with a carbon cap [46]. The Ohmic and Schottky contacts on the anode were Ti/Al sintered at 1000 °C and Ti sintered at 300 °C, respectively. The specific contact resistance of the Ti/Al ohmic contact was determined from a transfer length method. The contact resistance was 1.4×10^{-5} Ωcm^2 on the epitaxial anode and 2.2×10^{-4} Ωcm^2 on the implanted anode. The cathode contact was Ni sintered at 1000 °C. Note that the Schottky area was actually of junction-barrier Schottky (JBS) structure, which was formed by Al^+ implantation (stripe geometry), to reduce the leakage current. The surface was passivated with a thermally grown oxide and a 7 μm-thick polyimide. The widths of the pin-diode and Schottky-areas were both 150 μm, and the active area excluding the JTE region was 3.6×10^{-3} cm^2. This anode geometry and widths were optimized to suppress a "snapback" phenomenon [47], which is often observed in unipolar/bipolar hybrid operation.

The forward characteristics of fabricated diodes were tested with a semiconductor parameter analyzer (4200, Keithley, Solon, OH, USA) without packaging. The high-voltage reverse characteristics were measured with a custom-made high-voltage DC tester (Keithley, Solon, OH, USA) by immersing a diode in Fluorinart to avoid air sparking. The diode temperature was changed by using a heating stage.

5. Conclusions

Performance and potential limitation of SiC bipolar diodes were investigated by simulation and experiments. SiC pin diodes and other bipolar devices are especially attractive in the blocking voltage range of 10–30 kV, owing to the conductivity modulation effect. When the i-layer becomes

very thick to further increase the blocking voltage, however, the conductivity of such a thick i-layer is not fully modulated because of a limited carrier lifetime, leading to higher differential on-resistance. The intrinsic limitation of effective carrier lifetime in SiC originates from band-to-band recombination at the high-injection level. This limitation especially affects the device performance when the blocking voltage exceeds 50–60 kV.

One weak point of SiC pin diodes and other bipolar devices except bipolar junction transistors is the high knee voltage in the on-state. To overcome this issue, unipolar/bipolar hybrid operation is promising, because unipolar devices can carry the current at lower voltage drop when the current density is relatively low. As the first step, an 11 kV SiC MPS diode with an epitaxial anode was experimentally demonstrated. The proposed hybrid devices are attractive in the blocking voltage range of 8–15 kV. However, the advantage of these hybrid devices is almost lost when the blocking voltage is higher than 20 kV especially in the high-temperature operation, where the unipolar on-resistance becomes unacceptably high.

Supplementary Materials: The following are available online at www.mdpi.com/1996-1073/9/11/908/s1, Figure S1: Forward voltage drop at 100 A/cm^2 vs. doping concentration in the p-anode simulated with and without the bandgap narrowing effect in SiC pin diodes. The i-layer thickness is 200 μm. The optimum doping concentration can be determined as 5×10^{20} cm^{-3}, taking account of the bandgap narrowing effect, Figure S2: Forward voltage drop at 100 A/cm^2 vs. carrier lifetime in the i-layer simulated for SiC pin diodes having different i-layer thicknesses. In each case, the forward voltage drop shows saturation when the carrier lifetime is long enough. The saturated voltage drop significantly increases with increasing the i-layer thickness, Figure S3: Forward characteristics of the epitaxial MPS diode, pure pin diode, and pure JBS diode fabricated in this study. The proposed MPS diode exhibited a lower voltage drop than the pin diode at low current density and did than the JBS diode at high current density, Figure S4: Forward characteristics of SiC pin diodes having an i-layer thickness of 200 μm (28 kV class). The carrier lifetime in the i-layer was changed from 1 μs to 100 μs.

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