Article

A Comparison of Modulation Techniques for Modular Multilevel Converters

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Abstract: This work presents a comparison of three different modulation techniques applied to modular multilevel converters (MMCs). The three modulation strategies studied in this paper are the phase-shifted sinusoidal pulse width modulation (PS-SPWM), the space-vector modulation (SVM) and the nearest level modulation (NLM). This paper focuses on analysing the particularities and implementation of each modulation technique. The modulation technique largely defines the generated harmonic content, making this is a key point that must be studied in depth. The paper briefly describes the three modulation techniques and analyses the harmonics generated by each one of the methods. In addition, the paper presents and compares the digital implementation of the three modulation methods in a Field Programmable Gate Array (FPGA). The proposed approaches are validated using a real processing platform and experimentally evaluated in a real high-power six-level MMC.

Keywords: modulation techniques; modular multilevel converter; nearest level modulation; space vector modulation; sinusoidal pulse width modulation

1. Introduction

High-voltage direct current (HVDC) transmission using voltage source converters (VSCs) has been accepted as a feasible solution to connect distantly located renewable sources to large AC network [1,2]. To achieve high-voltage and high-power conversion, conventional VSC-HVDC systems were usually based on two-level or three-level converters with series-connected Insulated Gate Bipolar Transistors (IGBTs), which suffer from high voltage sharing across each power semiconductor device and, in general, poor power quality [3].

Multilevel converters (considering topologies of more than three levels) have received wide attention over the last few decades for various reasons, including their capability to manage high-voltage operation without series-connected switching devices, lower common-mode voltages, higher power quality and efficiency and the simple realization of redundancy [4,5]. The modular multilevel converter (MMC), first proposed by Marquardt [6], has been considered as the converter of choice for HVDC systems [7] and is already commercially used in HVDC projects [8–10]. In comparison with other topologies, MMC offers high modularity and scalability, transformerless operation, reduction of switching power losses and lower output filtering requirements [5,11].

A large number of different multilevel modulation methods have been developed parallel to the evolution of multilevel converters, being classified into two main groups [3]: voltage level-based algorithms and space vector-based algorithms. As number of level and, consequently, the number of power devices to control grow, the complexity of the modulation algorithm increases. The high number of possible switching states provides a wide range of choice in order to improve performance

features but complicates the algorithm to elect the switching pattern and its real-time implementation. The article implements and compares three of the most common modulation techniques: phase-shifted sinusoidal pulse-width modulation (PS-SPWM), space-vector modulation (SVM) and nearest-level modulation (NLM).

PS-SPWM is a popular multicarrier PWM technique for multilevel converters given its easy digital implementation [12]. PS-SPWM is based on introducing a phase shift between the carrier signals of contiguous cells that produces a phase-shifted switching pattern between them and generates a stepped multilevel waveform [4]. The main drawback of this solution is that as the number of levels of the converter increases, the phase shift between carriers become ever smaller, so that the generation of the carriers must be highly accurate.

SVM computes the switching times based on the three-phase space vector representation of the reference voltage and the inverter switching states [4]. The reference voltage is generated as a linear combination of the switching state vectors obtaining an averaged output voltage equal to the reference over one switching period [3]. SVM have attracted much attention because it provides significant flexibility to optimize switching waveforms with the objective of improving DC-bus voltage utilization or reducing the common-mode voltage and it is suitable for being implemented in digital signal processors [12,13]. Several authors have work in the development of SVM techniques for multilevel converters [14–17].

NLM is based on selecting the nearest voltage level that can be generated by the converter to the desired output voltage reference [4]. This method avoids the use of any carrier wave, by directly computing the switching states and duty cycles for each phase of the converter. NLM brings more flexibility and easy digital implementation, even if the number of levels of the converter is large.

The article seeks to provide a set of practical criteria for the choice of a modulation method for MMCs. Despite the fact that the three mentioned modulation strategies have been studied in the scientific literature, the authors have not found an article in which the three methods are compared and, in general, there is a gap about their digital implementation for MMCs. Digital implementation is generally not described. For that purpose, firstly, the three mentioned modulation methods are compared according to their generated harmonic content; secondly, the three modulation algorithms are compared in terms of their digital implementation on a FPGA-based system. The paper is organized as follows: Section 2 presents the MMC topology. The three modulation strategies under study are briefly described in Section 3. Section 4 shows the comparative study of the harmonic content generated by each modulation strategy. Section 5 presents the implementation of the three modulation algorithms on the FPGA-based digital platform and shows the experimental results. Section 6 concludes the paper.

2. Modular Multilevel Converter

Figure 1a shows the structure of a three-phase MMC, which is composed of two arms per phase. Each arm consists of ($n/2$) series-connected submodules (SMs), being n the number of SMs per phase, and an arm inductor, L_{MMC}. The Direct-Current bus (DC-bus) voltage (U_{DC}) is equally distributed between all SMs, being the SM's DC voltages, V_c, equal to:

$$V_c = \frac{U_{DC}}{n/2} \tag{1}$$

SMs of the MMC used in this article are half H-bridges, as shown in Figure 1b. Each SM contains two switches (IGBT and reverse diode) and a DC storage capacitor. The IGBTs are managed with complementary signals, S and $\overline{S}$, existing two possible values of the SM's output voltage, V_{SM}. When $S = 1$, $V_{SM} = V_c$. If $S = 0$, $V_{SM} = 0$ V. Therefore, the converter output voltages can take $n + 1$ voltage levels. Adding a new SM per arm increases in two voltage levels the possible values of the output. Half H-bridge topology is the most common SM [5], although there are other SM topologies that provide more output levels at the price of increasing the number of components, e.g., full H-bridge, multilevel Neutral Point Clamped (NPC) or Flying Capacitors (FC) cells [18].
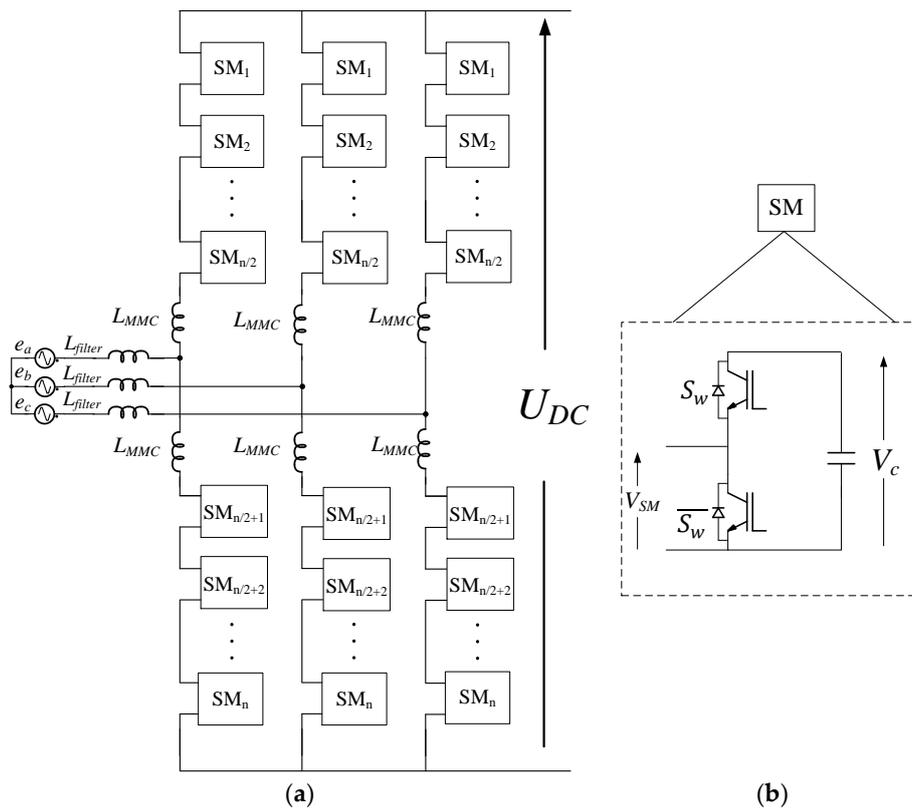
Figure 1. (**a**) Diagram of the modular multilevel converter (MMC); (**b**) Diagram of the half H-bridge submodules (SM).

3. Modulation Strategies under Study

3.1. PS-SPWM

PS-SPWM is an extension for multilevel converters of the popular SPWM [4]. The method is based on using $n/2$ carrier signals shifted between them by a phase shift, θ, given by:

$$\theta = \frac{360}{n/2} \tag{2}$$

In the literature, two modulation techniques for MMCs based on the number of output voltage levels have been described. These modulation techniques are called $N + 1$ and $2N + 1$, being N the number of SMs per arm [19,20].

In $2N + 1$ modulation, each arm modulates independently. Thus, the output voltage depends on the number of SM connected in both the upper and lower arm. This approach generates $2N + 1$ output levels. However due to the number of SM activated at the same time is not constant, it generates large SM voltage unbalances, especially in the case of MMC with low number of SMs as addressed in this paper [21].

In $N + 1$ modulation, the upper and lower phase arms of each phase are inversely commutated. Therefore, $N + 1$ output levels are generated. Despite this technique generates less output levels, it has the advantage of the number of SMs activated is always constant. Consequently, the capacitor voltage oscillations are reduced.

Thus, taking this into account, only $N + 1$ modulation technique has been chosen to be analyzed in this paper. Considering a 6-level MMC, Figure 2 shows the modulation signals, V_x with $x = 1, \ldots, 5$, for a single phase. The phase shift between the five carriers, VC_x, is θ = 72°. The output waveform is the sum of all the signals.
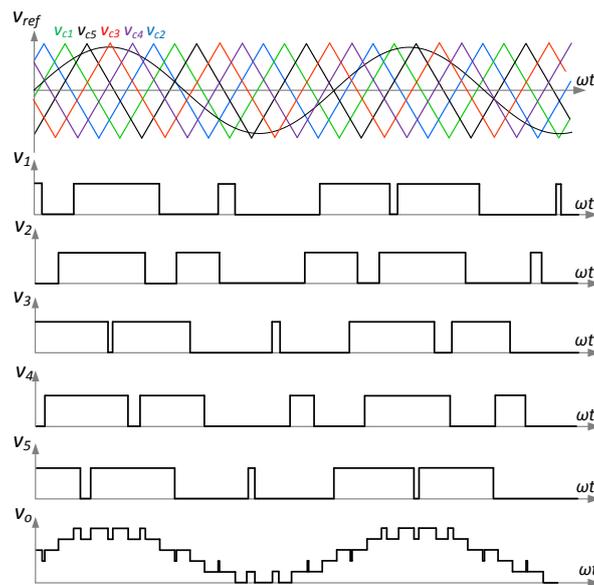
Figure 2. PS-SPWM output waveform generation.

3.2. SVM

SVM can conveniently provide more flexibility to optimize switching waveforms given the existence of redundant switching states and adjustable duty cycles and is suitable to be digitally implemented [22]. The main drawback of applying SVM to multilevel converters is that the complexity of the algorithm highly grows with the number of levels. Thus, it has not yet been well studied when it is applied to MMCs. In a three-phase n-level converter, there are usually n^3 switching states and $6 \times (n-1)^2$ triangles in the space vector diagram [23]. Figure 3 shows the space vector diagram for a six-level converter.
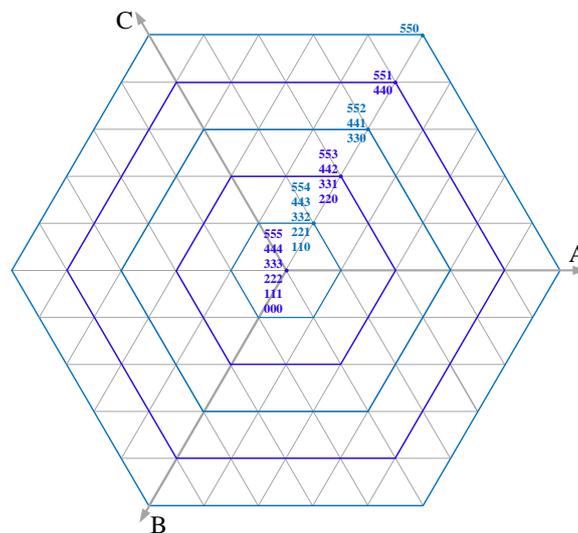

Figure 3. Space vector diagram for a six-level converter.

The algorithm used in this article is based on the fast SVM method presented in [24], which avoids the use of coordinate transformations and allows its adaptation for any *n*-level converter with minimum modifications. The algorithm is based on finding the four closest vectors to the reference voltages, as showed in Figure 4, using the normalized line voltages. The vectors are defined by means of the upper and lower rounded integer values from the normalized V_{ab}^n and V_{bc}^n voltages according to:

$$V_{ul} = \left[\begin{array}{c} \lceil V_{ab}^n \rceil \\ \lfloor V_{bc}^n \rfloor \end{array} \right], V_{lu} = \left[\begin{array}{c} \lfloor V_{ab}^n \rfloor \\ \lceil V_{bc}^n \rceil \end{array} \right], V_{uu} = \left[\begin{array}{c} \lceil V_{ab}^n \rceil \\ \lceil V_{bc}^n \rceil \end{array} \right], V_{ll} = \left[\begin{array}{c} \lfloor V_{ab}^n \rfloor \\ \lfloor V_{bc}^n \rfloor \end{array} \right] \tag{3}$$
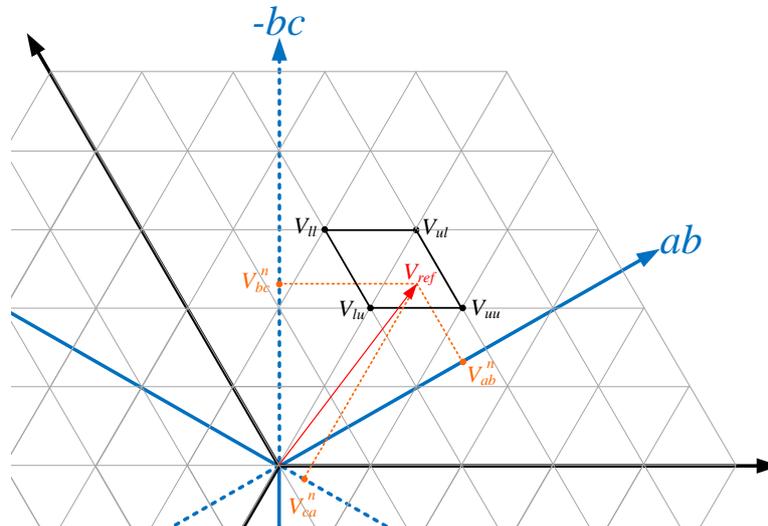
Figure 4. Graphic representation of fast SVM proposed in [14].

V_{ul} and V_{lu} are always two of the three closest vectors. The third vector is chosen according to:

$$\begin{cases} V_{uu} & if \quad V_{ca}^n + \left(\lceil V_{ab}^n \rceil + \lfloor V_{bc}^n \rfloor \right) < 0 \\ V_{ll} & if \quad V_{ca}^n + \left(\lceil V_{ab}^n \rceil + \lfloor V_{bc}^n \rfloor \right) > 0 \end{cases} \tag{4}$$

The duty cycles are obtained according to the third closest vector. If V_{ll}, the duty cycles are computed as:

$$\begin{cases} d_{ul} = V_{ab}^n - \lfloor V_{ab}^n \rfloor \\ d_{lu} = V_{bc}^n - \lfloor V_{bc}^n \rfloor \\ d_{ll} = 1 - d_{ul} - d_{lu} \end{cases} \tag{5}$$

If the third closest vector is V_{uu}, then:

$$\begin{cases} d_{ul} = -(V_{bc}^n - \lceil V_{bc}^n \rceil) \\ d_{lu} = -(V_{ab}^n - \lceil V_{ab}^n \rceil) \\ d_{uu} = 1 - d_{ul} - d_{lu} \end{cases} \tag{6}$$

The selection of the switching states is done after determining the available switching states for each vector by means of using:

$$\left[\begin{array}{c} k \\ k - V(1) \\ k - V(1) - V(2) \end{array} \right] \tag{7}$$

where $k \in [0, \ n - 1]$ and $V(1)$ and $V(2)$ are, respectively, the *ab* and the *bc* components of the corresponding vector (V_{ul}, V_{lu}, V_{uu} or V_{ll}).

3.3. NLM

NLM is a very interesting modulation technique to use when the number of SMs is quite large. Considering that, nowadays, there are MMC which easily exceed 200 SMs [25], the advantage of NLM over PS-SPWM or SVM is clear: PS-SPWM will require 100 carrier signals with a 3.6° shift between

them, which would need a very precise carrier generator, and the many possible switching states in SVM will rise the complexity of the algorithm.

NLM is based on generating the reference voltage by using two different voltage levels. Applying each voltage level during a certain period of time is possible to generate a signal whose mean value is the desired value. Figure 5 shows the operating principle [17].
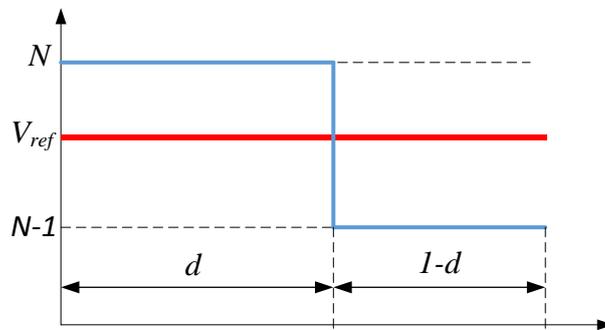

Figure 5. Operation principle of the NLM.

In the MMC the number of voltage levels in which the output signal can be divided depends on the number of SMs, adding a level for each additional SM (see Figure 2). A generalized formula for any level is:

$$V_{ref} = V_N \cdot d + V_{N-1}(1 - d), \tag{8}$$

where V_{ref} is the desired output voltage included between the voltage levels V_N and V_{N-1} and d is the duty cycle. The duty cycle d, of each phase are obtained as:

$$N = \left\lceil V_{ref} \right\rceil, \tag{9}$$

$$d = V_{ref} - \left\lfloor V_{ref} \right\rfloor, \tag{10}$$

Figure 6 illustrates the generation of the arm waveform using NLM for a MMC with five SMs per arm.
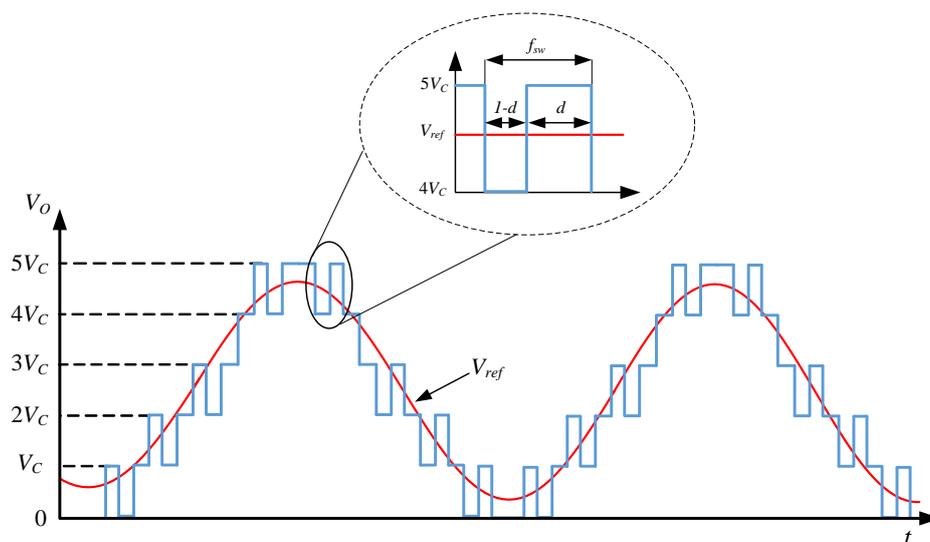

Figure 6. NLM arm waveform ($n = 10$).

3.4. Comparison Simulation Results

The waveform obtained by each modulation technique is shown in Figure 7. The figure shows the output waveform obtained using the three modulation techniques for the same voltage reference. The figure shows that each modulation technique generates different patterns affecting to the output waveform. Thus, the Total Harmonic Distortion (THD) and the harmonic content of each modulation technique differ quite substantially between them.
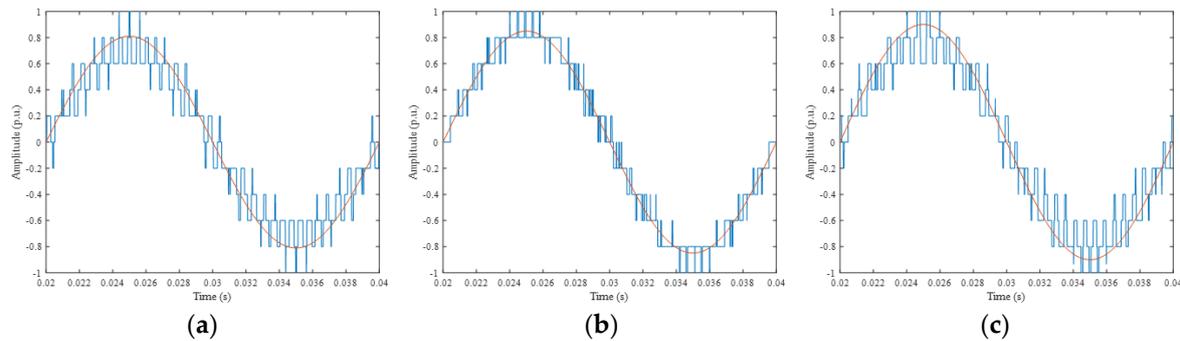

| (a) | (b) | (c) |

Figure 7. (**a**) SPWM waveform; (**b**) SVM waveform; (**c**) NLM waveform. (Blue line: Normalized reference output. Red line: Normalized output waveform).

3.5. SM Voltage

The modulation technique has an impact in the SM voltage ripple and in the circulating current. Thus, in order to minimize the impact in these operating aspects, both capacitor voltage balancing algorithm and a circulating current controller are employed.

The capacitor voltage algorithm used in this paper is proposed in [26]. The algorithm reorganizes the PWM gate signals in order to reduce the SM voltage difference along the arm. The proposed capacitor voltage balancing algorithm balances the capacitor voltages when there is a new switching state or when the difference between the maximum voltage of the capacitors and the minimum voltage of the capacitors is greater than the threshold voltage value $V_{Threshold}$.

The capacitor voltage balancing algorithm is designed to work after the modulation signal and carrier signal are compared. The algorithms modify the PWM signals generated by the PWM generator in function of the capacitor voltages and the current that flows through it. Figure 8 shows the capacitor voltage balancing algorithm operation diagram.
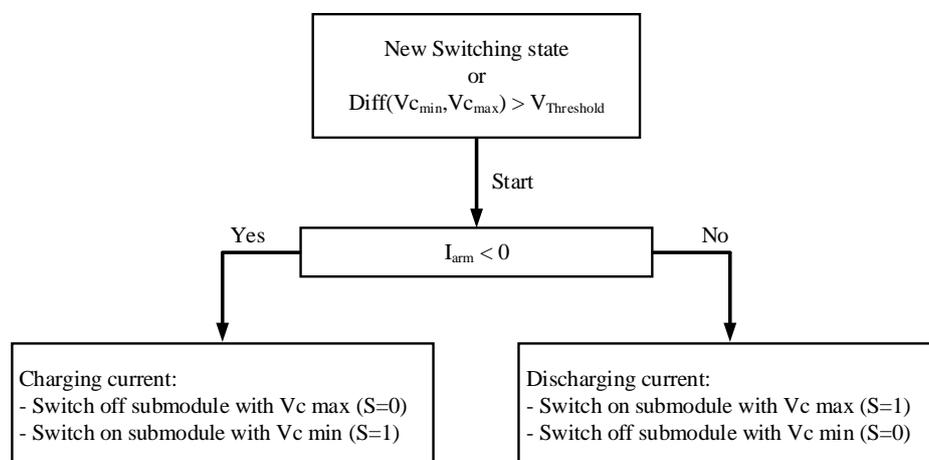

Figure 8. Capacitor voltage balancing algorithm diagram.

3.6. Circulating Current

The circulating current controller used in this paper is based on resonant controllers. It has been proposed in [27]. In order to reduce the circulating current, three resonant controllers are used to control the second ($h = 2$), the fourth ($h = 4$) and the sixth harmonic ($h = 6$) of the circulating current. The resonant controller is based on Second Order Generalized Integrator (SOGI) which has an excellent selectivity. The control scheme used is shown in Figure 9.
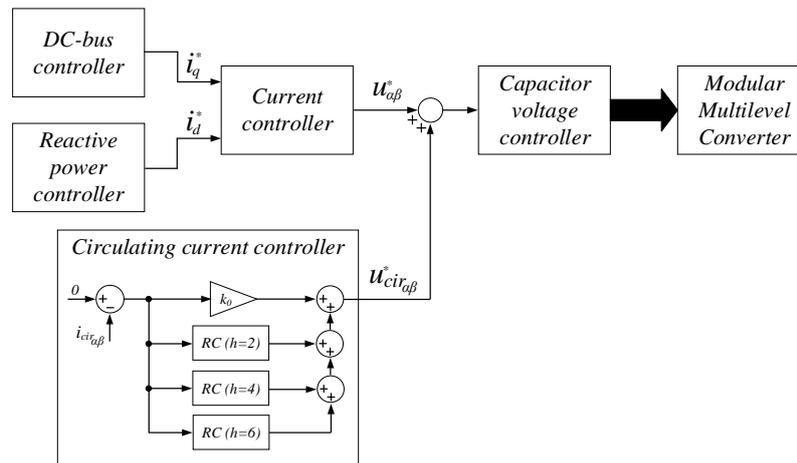

Figure 9. Circulating current control scheme based on resonant controller.

4. Generated Harmonic Content

In this section, the harmonic content generated by each modulation method is analyzed and compared in order to set design criteria in advance. The harmonics content generated by each modulation strategy according to the modulation index is a key point. This study reveals which are the harmonics generated by each modulation technique and facilitates a criterion for choosing the most appropriate modulation technique according to the requirements.

Due to the fact that the modulation methods under study are quite different from each other, the order of the generated harmonics will be different among methods. In order to set a common framework and to facilitate the analysis, some variables are defined below.

The amplitude modulation index, m_a, is defined as the value of the fundamental voltage harmonic, V_{fund}, divided by the value of the reference signal, V_{ref}:

$$m_a = \frac{V_{fund}}{V_{ref}} \tag{11}$$

The other variable is a frequency relationship, r_f. In the case of the PS-SPWM, r_f relates the carrier frequency, f_{cr}, and the frequency of the modulating signal, f_{ref}, as:

$$r_f = \frac{n \cdot f_{cr}}{f_{ref}} \tag{12}$$

In SVM and NLM r_f is defined as the switching frequency, f_{sw}, used to rotate between the three vectors in the SVM or to switch between the two voltage levels in the NLM, divided by the modulating signal frequency, f_{ref}:

$$r_f = \frac{f_{sw}}{f_{ref}} \tag{13}$$

The simulation results obtained for PS-SPWM are shown in Figure 10, which presents the harmonic distribution according to m_a. The harmonics with the highest amplitude are generated at $r_f \pm 2$ and $r_f \pm 4$.
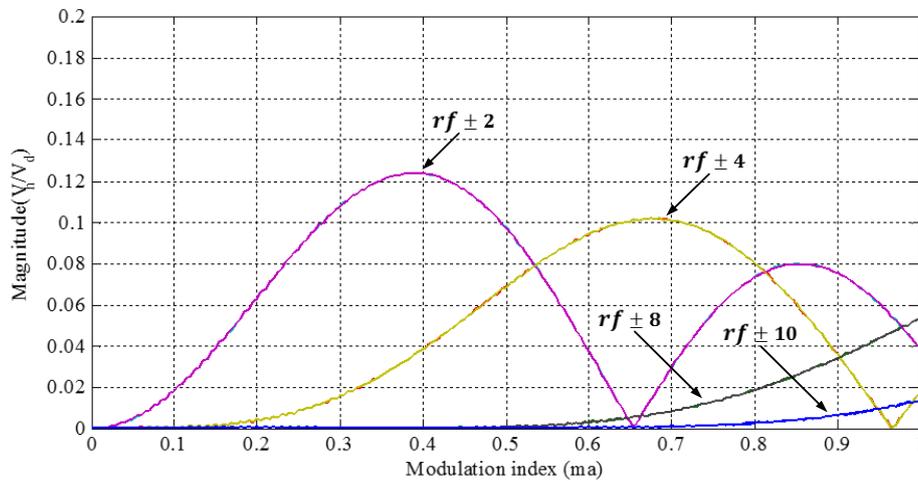

Figure 10. PS-SPWM harmonic distribution according to m_a.

In the SVM technique, the harmonic content is lower compared to PS-SPWM or NLM (see Figure 11). Since there is a high degree of flexibility in this modulation technique, the harmonic distribution largely depends on the chosen vectors.
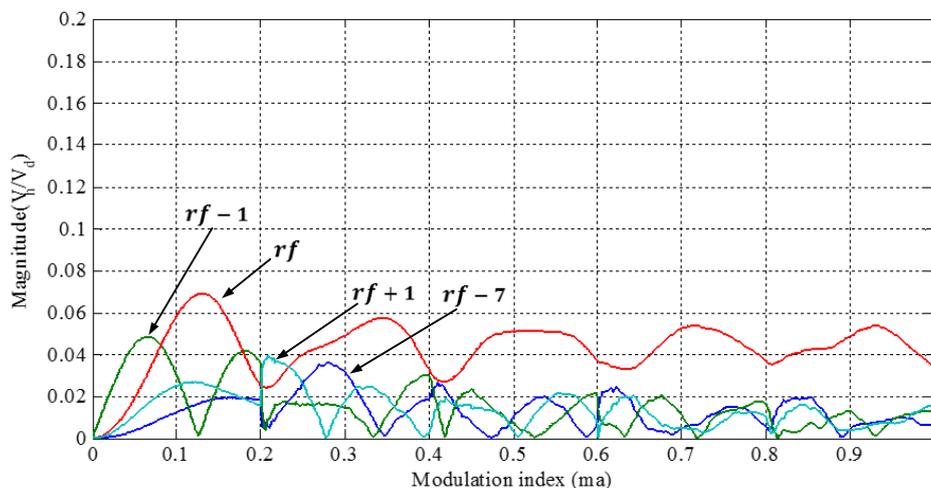

Figure 11. SVM harmonic distribution according to m_a.

The results for NLM are shown in Figure 12. The harmonics in NLM method have less amplitude compared to PS-SPWM but higher than SVM. The THD obtained with each modulation is shown in Figure 13. The figure represents the THD of the line-to-line voltage according to the modulation index. For the purpose of comparing the THD of the three modulation techniques, different frequencies for each modulation have been employed in order to have the same number of transitions per cycle. Thus, The PS-SPWM uses carrier signals at 750 Hz. The SVM and the NLM calculate the duty cycle by means of a frequency of 5.25 kHz and 3.75 kHz, respectively. The figure shows that, in the case of PS-SPWM, the THD is higher than in NLM and SVM methods. However, as m_a increases, the difference between modulation techniques is lower.
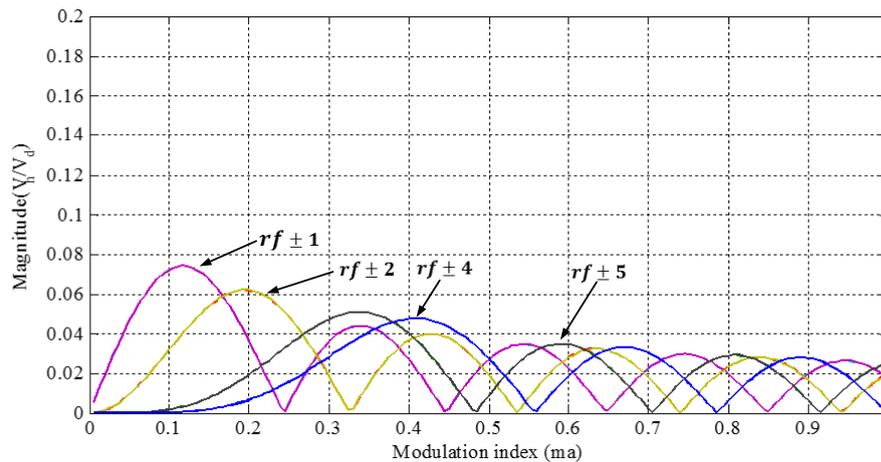
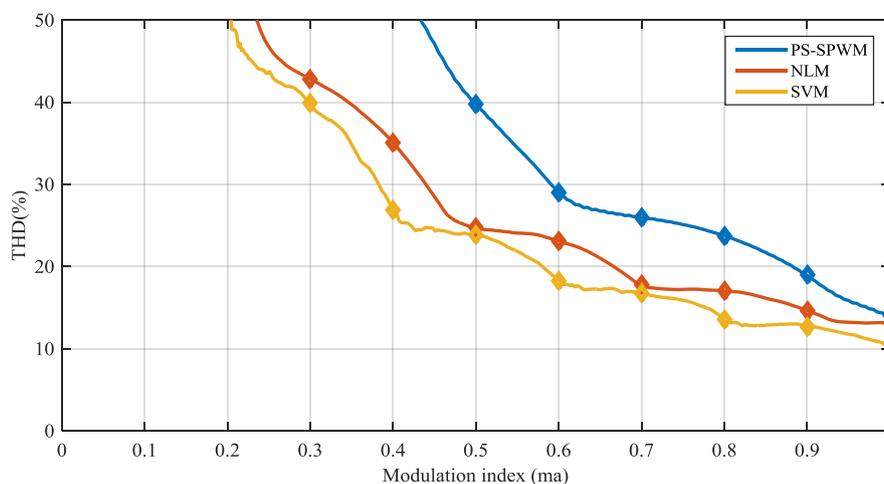**Figure 12.** NLM harmonic distribution according to m_a.

Figure 13. THD of the three modulation methods under study according to m_a.

Table 1 shows a comparative analysis regarding the amount of switching transitions performed by each IGBT during one cycle of the fundamental signal (0.02 s) using the aforementioned switching frequencies. The Table shows that using the proposed implementation, PS-SPWM has the lowest number of switching transitions followed by the SVM. For the same number of output switching transitions, the results show that the NLM requires twice the number of transitions of PS-SPWM.

Table 1. Comparative of switching transitions per IGBT.

Modulation Technique	$N°$ Switching
PS-SPWM	30
SVM	48
NLM	60

5. Experimental Results

The three modulation methods have been validated and evaluated in the real six-level MMC prototype shown in Figure 14. The main parameters of the converter are presented in Table 2. The switching frequency of each modulation technique is the same that in Section 4. The PS-SPWM has been implemented with carriers of 750 Hz. The SVM and the NLM calculates the duty cycle by means of a frequency of 5.25 kHz and 3.75 kHz, respectively.
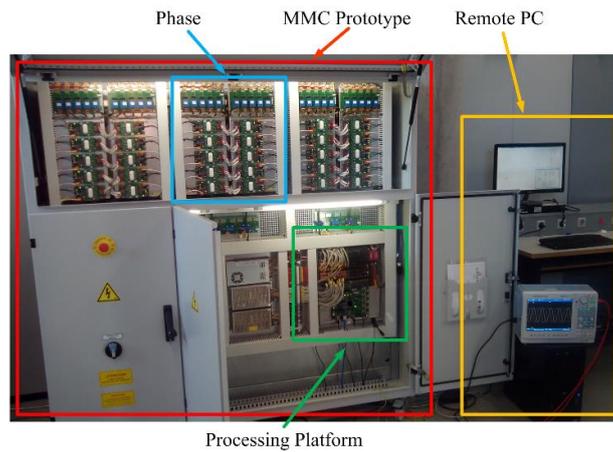
Figure 14. Modular Multilevel Converter Prototype.

Table 2. MMC Prototype Parameters.

Parameter	Value
Nominal Power	50 kVA
Nominal Voltage	400 V
N° submodules per phase	10
Submodule Capacitor	2200 μF
IGBT	SKM145GB066D
IGBT Driver	Skyper 32 R UL
DC-bus voltage	1200 V
MMC inductor	0.5 mH
Grid inductor	5 mH

The three modulation algorithms have been implemented and tested in a control platform designed to be used in large multilevel converters. The control platform consists of two interconnected boards referred as processing board (PB) and interface board (IB). Figure 15 presents the block diagram and a photo of this control platform.
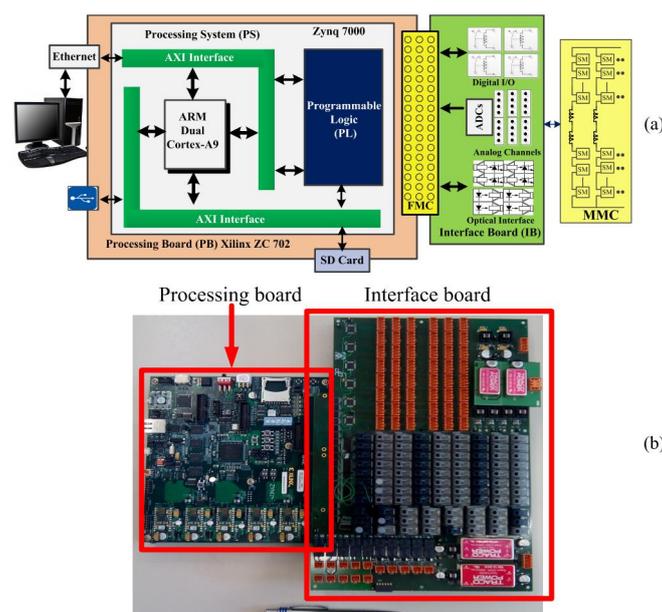

Figure 15. (**a**) Block diagram; (**b**) picture of the control platform.

　　The PB is based on the Xilinx ZC702 Evaluation board (Manufactured by Xilinx, Plano, TX, USA). The ZC702 includes a Zynq-7000 XC7Z020 SoC. This SoC integrates a dual-core ARM Cortex-A9, which constitutes the core of the processing system (PS), and programmable logic (PL) based on an Artix-7 FPGA. The purpose of the PB is twofold: firstly, it implements the bidirectional communication with the host computer through an Ethernet connection and, secondly, it executes all the converter control algorithms [28].

　　The IB has been designed by the authors. It implements the interface between the power converter and the PB and carries out two main functions: (i) it adapts the signals that are exchanged with the converter, mainly sampled voltages and currents and modulation signals: (ii) it implements the acquisition system, which is used to sample the converter signals: the arm and grid currents, and the grid and SM voltages.

　　To the best knowledge of the authors, there are not in-depth studies about the digital implementation in a real processing platform of the three considered modulation techniques. The modulation techniques have been usually implemented in a Digital Signal Processor (DSP) due to the ease implementation [18,27]. However, this approach has several disadvantages such as the increased DSP processing time or a reduced accuracy due to the limited available resources. In this paper, the three modulation techniques have been implemented in a FPGA-based processing platform. Although the FPGA-based approach can increase the implementation complexity, it considerably improves accuracy and performance, meanwhile processing time is greatly reduced.

　　The entire modulation techniques have been implemented in the PL blocks of the PB. The available resources are 85,000 logic cells (LCs), 53,200 look-up tables (LUTs) and 106,400 flip-flops. The modulation methods have been implemented as Intellectual Property (IP) peripheral cores. These cores are connected to the AXI-bus of the FPGA, which interconnects modulation blocks and control loops. The advantage of use such cores is they can be exported to other devices without changes, reducing the development time. In addition, the three modulation techniques are simultaneously implemented and can be selected by the controller at any time. The implementation of each modulation technique is described below.

5.1. PS-SPWM

　　PS-SPWM requires five carrier signals to generate the gate signals of a six-level converter. Figure 16 shows the block diagram of the per-arm implementation of the modulation algorithm. Each carrier signal is generated by the "PWM carrier generation" blocks, which allow programmable phase shift and frequency. The carrier signals are compared with the arm voltage reference and, then, five master gate signals are generated. Figure 17 shows the full control diagram. Six blocks are required (one for each arm) in order to generate the PWM master signals from the six voltage references. These master signals are modified by the capacitor voltage balancing algorithm and then inverted by a dead-time controller which generates the rest of the PWM signals. Finally, the PWMs signals are applied to the SMs' IGBTs.

　　Fixed-point codification is used for the reference signals and carrier signals. The amplitude of the carrier signals is fixed and normalized between -1 and 1. The frequency of the carrier signals is controlled by the step size (n_step) used to increment the signal each period. The phase shifting is controlled by the initial value of the carrier signals ($init_{crs}$).
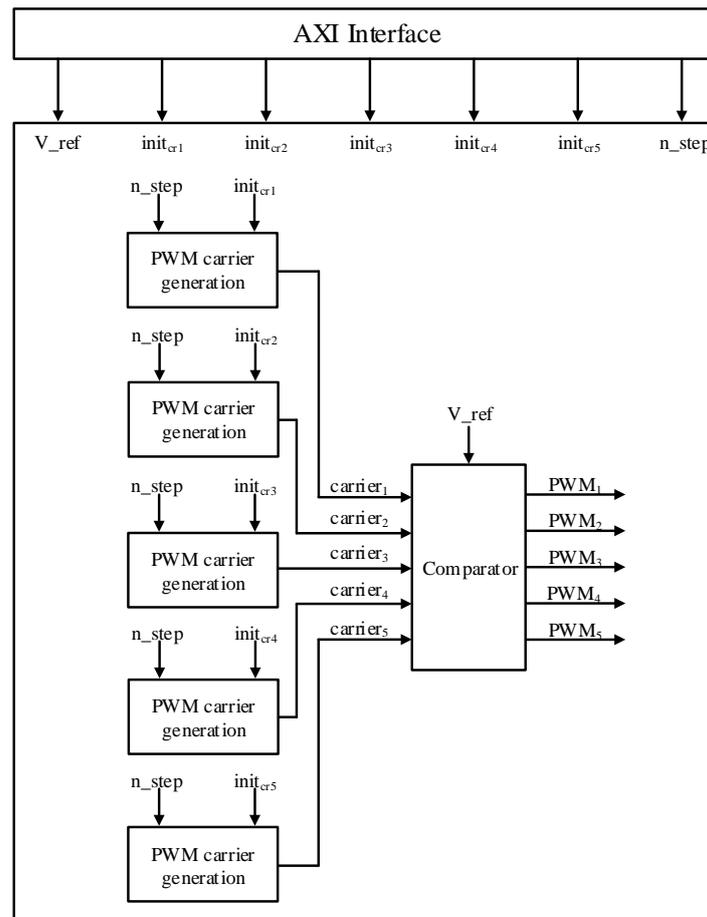
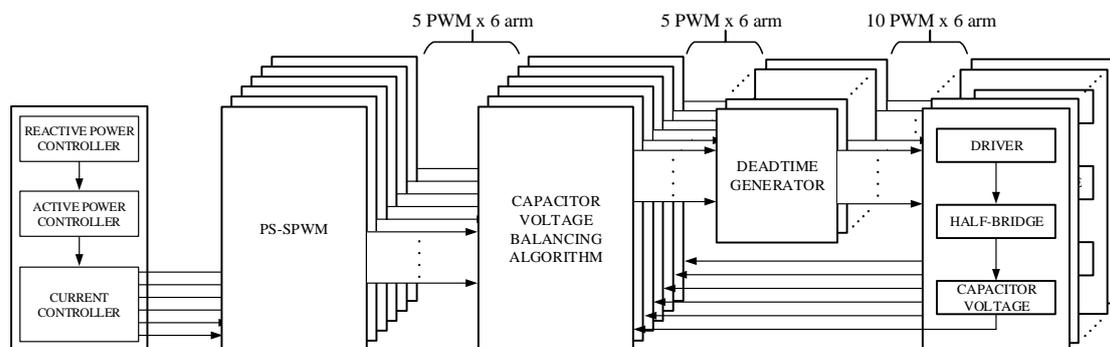**Figure 16.** Block diagram per-arm of the implemented PS-SPWM.

Figure 17. PS-SPWM full control diagram.

5.2. SVM

SVM presents the most complex implementation of the three modulations under study, however it provides more degrees of freedom since the voltage reference can be obtained applying multiple voltage vectors. Unlike PS-SPWM and NLM, in SVM the gate signals of the three phases must be generated in the same block. Figure 18 presents the block diagram of the implemented SVM method.

The core receives the three line voltages and, then, the block namely 'Rounded voltage vector calculation' calculates eight possible rounded vectors according to (3). The third vector, V_{ll} or V_{uu}, is chosen from (4). The duty cycles are obtained using V_{ab} and V_{bc} voltage reference signals and the three aforementioned voltage vectors by using (5) and (6).
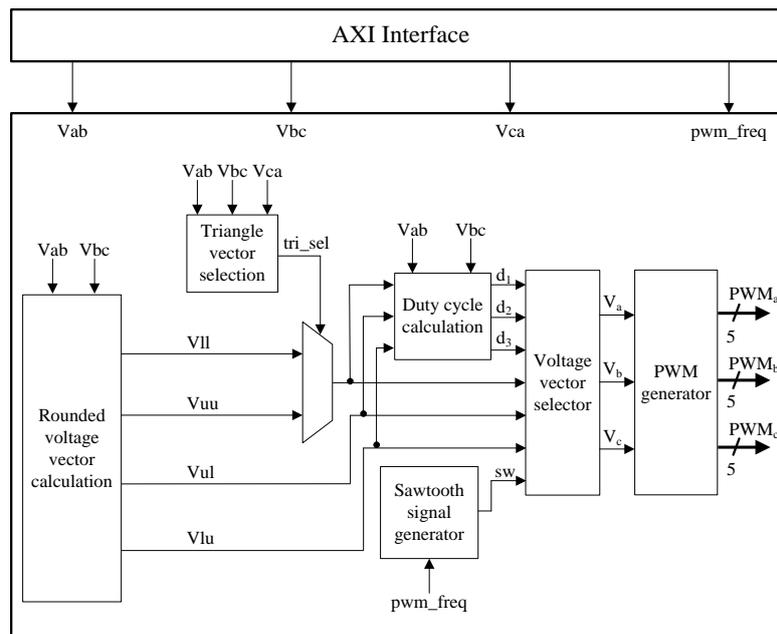
Figure 18. Block diagram of the implemented SVM.

The next step is to calculate the voltage levels of each phase to generate the corresponding output voltage level. The phase voltage is obtained from the three voltage vectors (see Figure 4). The sawtooth signal is used to switch the output between the three voltage vectors using the duty cycles calculated above. Finally, the output voltage reference is applied to a PWM generator in order to generate the gate signals for the IGBTs. The gate signals are generated depending on the amplitude of the voltage reference and a circular array is used to rotate the switching pulses in order to distribute the switching losses. Figure 19 shows the SVM full control diagram. Two blocks are used (one for the upper arm and one for the lower arm) in order to obtain the PWM master signals which then are introduced in the capacitor voltage balancing algorithm with the objective to balance the capacitor voltages. Finally, the remaining PWM gate signals are generated by the dead-time generator.
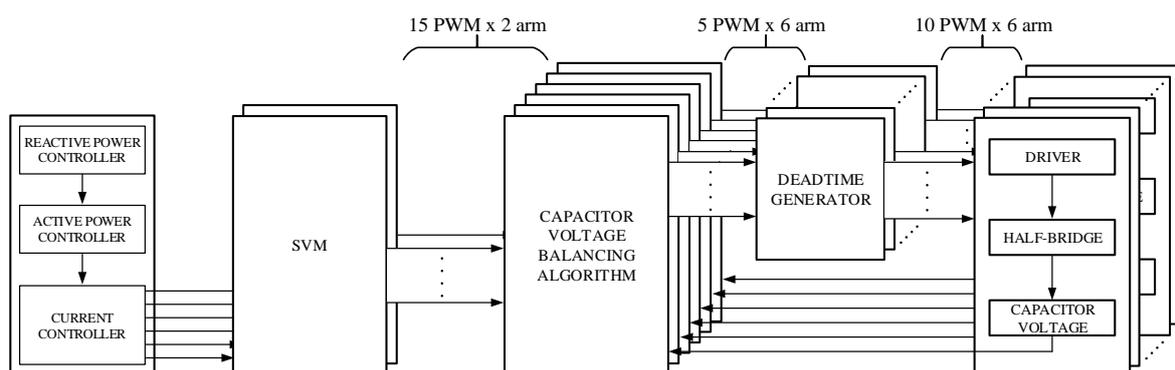

Figure 19. SVM full control diagram.

5.3. NLM

In contrast with PS-SPWM and SVM, the implementation of the NLM method is less complex as Figure 20 demonstrates and, thus, it is a very suitable modulation method for MMC with large numbers of SMs. Only one control variable is required, the switching frequency (*pwm_freq*). The core receives the voltage reference (V_{ref}) which is both upper rounded (V_N) and lower rounded (V_{N-1}) to

the next nearest integer voltage level. The duty cycle is obtained from the voltage reference signal and its rounded value and (10).
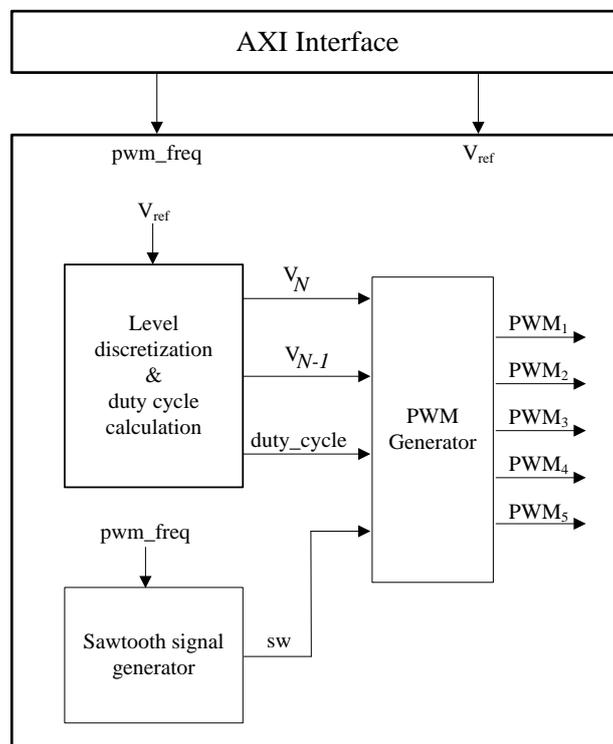

Figure 20. Block diagram per arm of the implemented NLM.

A sawtooth signal with programmable frequency (*pwm_freq*) is used to switch the output between two levels V_N and V_{N-1}. The range of the signal is (0, 1), thus, it can be directly compared with the duty cycle and therefore the right voltage level is generated. Finally, the gate signals are generated depending on the amplitude of V_N and V_{N-1}. As in the previous case, a circular array is also used to distribute the switching losses. Figure 21 illustrates the NLM full control diagram. In the same way as in PS-SPWM, six blocks are necessary to generate the PWM master signals. Then, they are modified by the capacitor voltage balancing algorithm and inverted by the dead-time controller in order to obtain all the PWM signals which are then applied to the IGBTs.
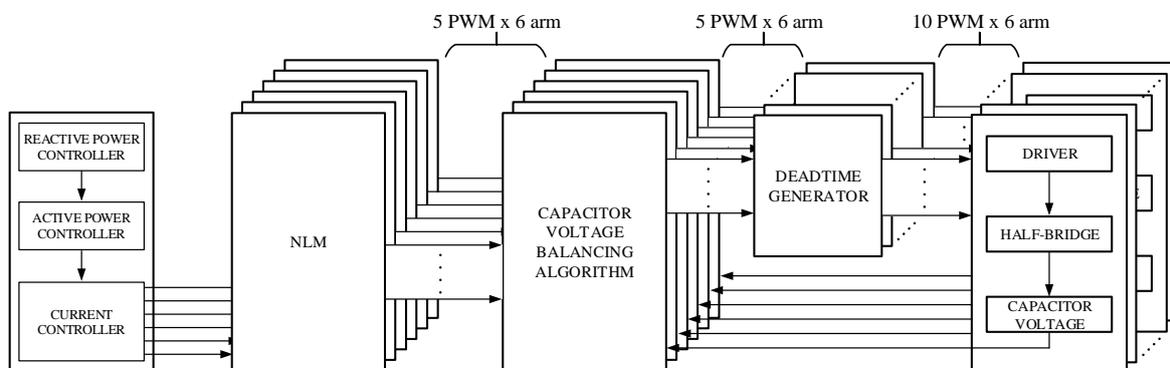

Figure 21. NLM full control diagram.

5.4. Comparison of the Modulation Methods

The FPGA resources used by each modulation technique are shown in Table 3. SVM is the modulation method that requires more resources and PS-SPWM is the algorithm that consumes fewer resources. However, the difference in the number of required resources is very small if considering the large amount of available resources in the control platform.

Table 3. FPGA Resources.

Modulation Technique	Used FPGA Resources			
	LUTs		Flip-Flops	
PS-SPWM	315	0.59%	94	0.08%
SVM	992	1.86%	482	0.45%
NLM	762	1.43%	349	0.32%

Although Table 3 shows that NLM requires more resources than PS-SPWM, the resources used by this modulation technique barely increase when the number of SMs increases. Otherwise, in SPWM and SVM the resources used greatly increase when the SMs increases. In PS-SPWM due to the large number of carrier signals required and in SVM due to the complex operations required. Moreover, the resources used depend on the operation type performed (i.e., multiplication, sum, etc.) and how the code is written.

Two experimental tests have been carried out in the prototype above-mentioned. The first test consists of measuring the output voltages without any connected load. The objective of this test is to measure the output voltages without the influence of inductances that could filter the generated harmonics. Figures 22–24 show the line-to-line output waveform obtained using the PS-SPWM, SVM and NLM respectively. As can be seen, the three modulation techniques properly generate the waveforms.

The second test consists of measuring the output currents and analyzing the harmonic content. To carry out this test, a 2 kW load is connected to the converter output.
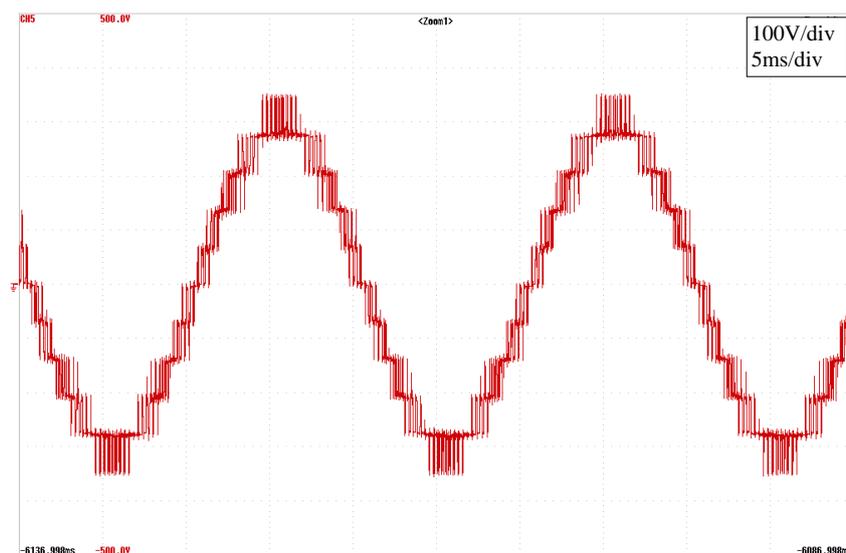

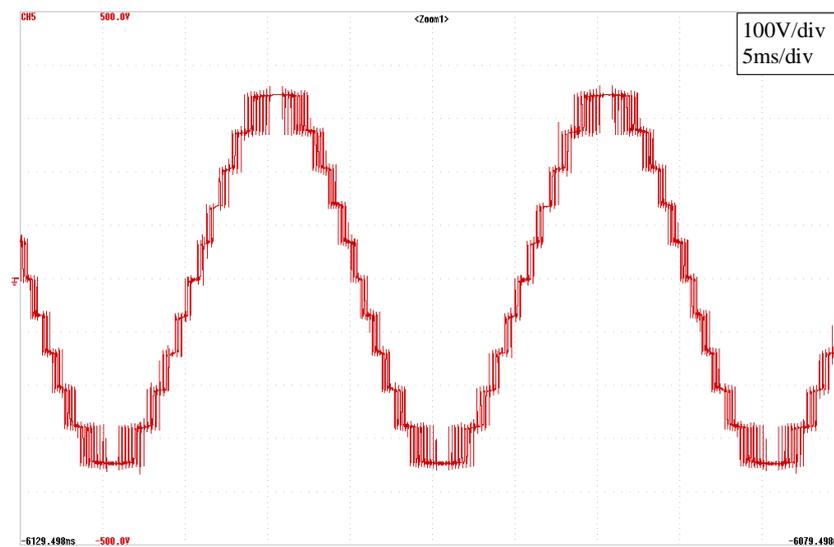**Figure 22.** PS-SPWM line-to-line output waveform without load.

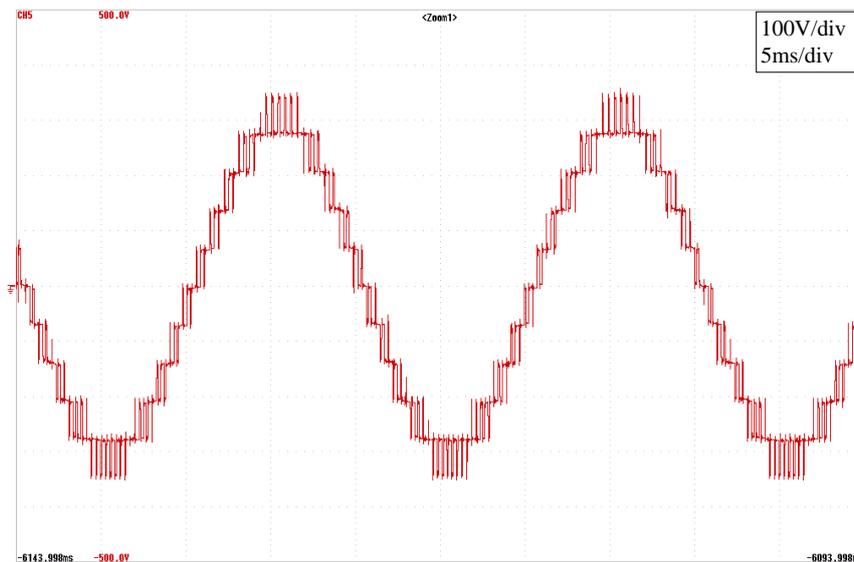**Figure 23.** SVM line-to-line output waveform without load.

Figure 24. NLM line-to-line output waveform without load.

Figures 25–27 show the output current for PS-SPWM, SVM and NLM respectively. In addition, the output current THD for each modulation technique is shown in Table 4. The figures show that the three modulation techniques apparently generate similar output currents. However, if the THD is analyzed, the results shown in Table 4 reveal that PS-SPWM and SVM present a similar THD, while in the NLM case the THD is almost twice.

Table 4. THD output current.

Modulation	THD
PS-SPWM	1.70%
SVM	1.42%
NLM	1.51%

The experimental results validate the proposed digital implementations of the modulation strategies and corroborate the simulation results.
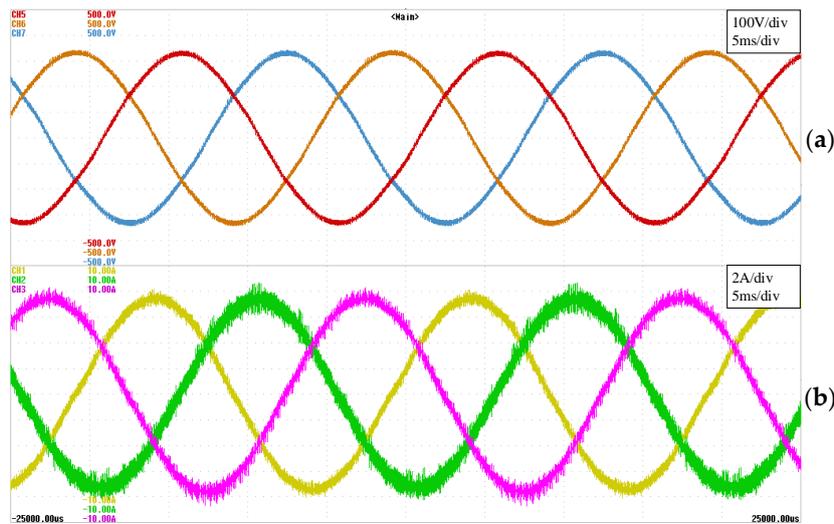
Figure 25. PS-SPWM operation with a 2 kW load. (**a**) line-to-line output voltages and (**b**) output currents.
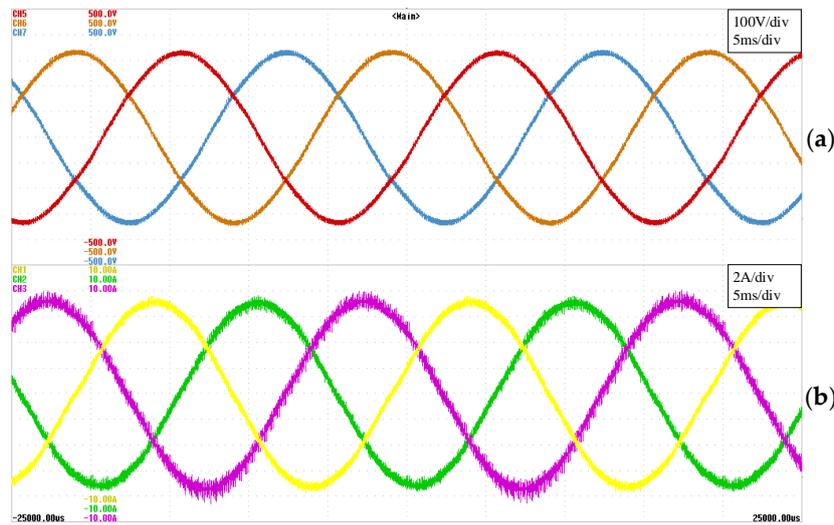

Figure 26. SVM operation with a 2 kW load. (**a**) line-to-line output voltages and (**b**) output currents.
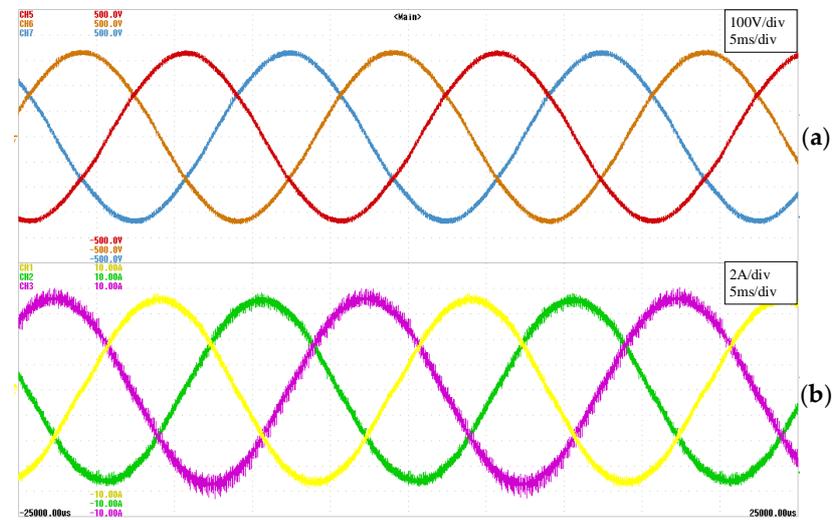

Figure 27. NLM operation with a 2 kW load. (**a**) line-to-line output voltages and (**b**) output currents.

6. Conclusions

In this paper a comparison between different modulation techniques used in MMCs has been presented. Three modulation techniques have been studied: PS-SPWM, SVM and NLM. The paper briefly describes the three modulation strategies and presents how they are implemented in a FPGA-based digital processing platform. The proposed FPGA-based approach achieves high accuracy and reduced computational resources in comparison with a DSP implementation. In addition, the paper presents a comparative study about the harmonic content generated by each modulation technique. The results show that each modulation technique generates different harmonic content, thus, depending on the application, there will be a modulation technique more suitable than others. In MMCs with large number of SMs, the NLM is the most suitable modulation technique due to the flexibility and the facility to scale followed by the SVM which also provides reasonable flexibility. In the case of MMCs with low number of SMs, the SPWM is the best solution due to it is usually implemented in the microcontrollers designed to control power converters. Finally, the proposed implementations have been experimentally evaluated and validated in a real six-level MMC.

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References

1. Flourentzou, N.; Agelidis, V.G.; Demetriades, G.D. VSC-based HVDC power transmission systems: An overview. *IEEE Trans. Power Electron.* **2009**, *24*, 592–602. [CrossRef]
2. Bresesti, P.; Kling, W.L.; Hendriks, R.L.; Vailati, R. HVDC connection of offshore wind farms to the transmission system. *IEEE Trans. Energy Convers.* **2007**, *22*, 37–43. [CrossRef]
3. Franquelo, L.G.; Rodriguez, J.; Leon, J.I.; Kouro, S.; Portillo, R.; Prats, M.A.M. The age of multilevel converters arrives. *IEEE Ind. Electron. Mag.* **2008**, *2*, 28–39. [CrossRef]
4. Rodríguez, J.; Franquelo, L.; Kouro, S.; Leon, J.; Portillo, R.; Prats, M.; Pérez, M. Multilevel Converters: An Enabling Technology for High Power Applications. *Proc. IEEE* **2009**, *97*, 1786–1817. [CrossRef]
5. Perez, M.A.; Bernet, S.; Rodriguez, J.; Kouro, S.; Lizana, R. Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters. *IEEE Trans. Power Electron.* **2015**, *30*, 4–17. [CrossRef]
6. Marquardt, R. Stromrichterschaltungen mit Verteilten Energies-Peichern. German Patent DE201,229,23U1, 24 January 2001.
7. Ahmed, N.; Haider, A.; van Hertem, D.; Zhang, L.; Nee, H.-P. Prospects and challenges of future HVDC SuperGrids with modular multilevel converters. In Proceedings of the 14th Conference on Power Electronics and Applications (EPE 2011), Birmingham, UK, 30 August–1 September 2011; pp. 1–10.
8. Knaak, H.J. Modular multilevel converters and HVDC/FACTS: A success story. In Proceedings of the 14th Conference on Power Electronics and Applications (EPE 2011), Birmingham, UK, 30 August–1 September 2011; pp. 1–6.
9. Kirby, N.M.; MacLeod, N.M.; Stidham, D.; Reynolds, M. Tres Amigas: A flexible gateway for renewable energy exchange between the three asynchronous AC networks in the USA. In Proceedings of the CIGRE, Paris, France, 26–31 August 2012.
10. Breuer, W.; Retzmann, D.; Uecker, K. Highly Efficient Solutions for Smart and Bulk Power Transmission of Green Energy. In Proceedings of the 21th World Energy Congress, Montreal, QC, Canada, 13–16 September 2010; pp. 1–24.
11. Bergna, G.; Garces, A.; Berne, E.; Egrot, P.; Arzande, A.; Vannier, J.-C.; Molinas, M. A Generalized Power Control Approach in ABC Frame for Modular Multilevel Converter HVDC Links Based on Mathematical Optimization. *IEEE Trans. Power Del.* **2014**, *29*, 386–394. [CrossRef]

12.	Hussin, H.; Saparon, A.; Muhamad, M.; Risin, M.D. Sinusoidal Pulse Width Modulation (SPWM) Design and Implementation by Focusing on Reducing Harmonic Content. In Proceedings of the 4th Asia International Conference on Mathematical Modelling and Computer Simulation (AMS 2010), Kota Kinabalu, Malaysia, 26–28 May 2010; pp. 620–623.

13.	Celanovic, N.; Boroyevich, D. A fast space vector modulation algorithm for multilevel three phase converters. *IEEE Trans. Ind. Appl.* **2001**, *37*, 637–641. [CrossRef]

14.	Yao, W.; Hu, H.; Lu, Z. Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter. *IEEE Trans. Power Electron.* **2008**, *23*, 45–51. [CrossRef]

15.	McGrath, B.P.; Holmes, D.G.; Lipo, T. Optimized space-vector switching sequences for multilevel inverters. *IEEE Trans. Power Electron.* **2003**, *18*, 1293–1301. [CrossRef]

16.	Zhou, K.; Wang, D. Relationship between space-vector modulation and three-phase carrier-based PWM: A comprehensive analysis. *IEEE Trans. Ind. Electron.* **2002**, *49*, 186–196. [CrossRef]

17.	Deng, Y.; Harley, R.G. Space-Vector versus Nearest-Level Pulse Width Modulation for Multilevel Converters. *IEEE Trans. Power Electron.* **2015**, *30*, 2962–2974. [CrossRef]

18.	Nami, A.; Jiaqi, L.; Dijkhuizen, F.; Demetriades, G.D. Modular Multilevel Converters for HVDC Applications: Review on Converter Cells and Functionalities. *IEEE Trans. Power Electron.* **2015**, *30*, 18–36. [CrossRef]

19.	Li, B.; Yang, R.; Xu, D.; Wang, G.; Wang, W.; Xu, D. Analysis of the Phase-Shifted Carrier Modulation for Modular Multilevel Converters. *IEEE Trans. Power Electron.* **2015**, *30*, 297–310. [CrossRef]

20.	Gowaid, I.A.; Adam, G.P.; Ahmed, S.; Holliday, D.; Williams, B.W. Analysis and Design of a Modular Multilevel Converter with Trapezoidal Modulation for Medium and High Voltage DC-DC Transformers. *IEEE Trans. Power Electron* **2015**, *30*, 5439–5457. [CrossRef]

21.	Konstantinou, G.; Ciobotaru, M.; Agelidis, V. Selective harmonic elimination pulse-width modulation of modular multilevel converters. *IET Power Electron.* **2013**, *6*, 96–107. [CrossRef]

22.	Gupta, A.K.; Khambadkone, A.M. A Space Vector PWM Scheme for Multilevel Inverters Based on Two-Level Space Vector PWM. *IEEE Trans. Ind. Electron.* **2016**, *53*, 1631–1639. [CrossRef]

23.	Deng, Y.; Teo, K.H.; Duan, C.; Habetler, T.G.; Harley, R.G. A Fast and Generalized Space Vector Modulation Scheme for Multilevel Inverters. *IEEE Trans. Power Electron.* **2014**, *29*, 5204–5217. [CrossRef]

24.	Castro, L.G.; Corréa, M.B.; Jacobina, C.B.; Boroyevich, D. A fast space-vector algorithm for multilevel converters without coordinates transformation. In Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE 2010), Atlanta, GA, USA, 12–16 September 2010; pp. 2543–2547.

25.	Zhou, Y.; Jiang, D.; Hu, P.; Guo, J.; Liang, Y.; Lin, Z. A Prototype of Modular Multilevel Converters. *IEEE Trans. Power Electron.* **2014**, *29*, 3267–3278. [CrossRef]

26.	Moranchel, M.; Bueno, E.J.; Rodriguez, F.J.; Sanz, I. Novel capacitor voltage balancing algorithm for modular multilevel converter. In Proceedings of the 40th Annual Conference of the IEEE Industrial Electronics Society (IECON 2014), Dallas, TX, USA, 29 October–1 November 2014; pp. 4697–4701.

27.	Moranchel, M.; Bueno, E.J.; Rodriguez, F.J.; Sanz, I. Circulating current elimination in Modular Multilevel Converter with resonant controllers. In Proceedings of the 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG 2016), Vancouver, BC, Canada, 27–30 June 2016; pp. 1–6.

28.	Moranchel, M.; Sanchez, F.M.; Bueno, E.J.; Rodriguez, F.J.; Sanz, I. Six-level modular multilevel converter prototype with centralized hardware platform controller. In Proceedings of the 41st Annual Conference of the IEEE Industrial Electronics Society (IECON 2015), Yokohama, Japan, 9–12 November 2015; pp. 3863–3868.