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Modeling and Control of the Distributed Power Converters in a Standalone DC Microgrid

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Abstract: A standalone DC microgrid integrated with distributed renewable energy sources, energy storage devices and loads is analyzed. To mitigate the interaction among distributed power modules, this paper describes a modeling and control design procedure for the distributed converters. The system configuration and steady-state analysis of the standalone DC microgrid under study are discussed first. The dynamic models of the distributed converters are then developed from two aspects corresponding to their two operating modes, device-regulating mode and bus-regulating mode. Average current mode control and linear compensators are designed accordingly for each operating mode. The stability of the designed system is analyzed at last. The operation and control design of the system are verified by simulation results.

Keywords: standalone DC microgrid; dynamic modeling and control; distributed converters; bidirectional buck-boost converter

1. Introduction

With increasing use of renewable energy sources (RES), the standalone DC microgrid is envisioned as one promising technology to integrate distributed RES, energy storage devices (ESD) and varieties of loads in many power management and distribution applications [1–4].

In a generic standalone DC microgrid, distributed RES, ESD and loads are interfaced to the DC bus using power electronics converters. There is no specific line regulator; thus, ESD converters or RES converters have to take charge of the bus regulation. Therefore, power converters in the system can be divided into two groups depending on their respective operating modes, bus-regulating mode and device-regulating mode.

In the design of a DC microgrid integrated with distributed power modules, one of the primary concerns is how to avoid the undesirable interaction among different modules. The interaction may appear as two forms: the non-zero output impedance of bus-regulating converters may interfere with the control loops of device-regulating converters, and the non-resistive input impedance of device-regulating converters may affect the control loops of bus-regulating converters. In most applications, the device-regulating converters have to provide strict output voltage regulation to satisfy the voltage requirement of the devices, which, together with the high efficiency of these converters, causes them to perform like constant power sources/loads to the DC bus. Consequently, when the net power of device-regulating converts is towards/against the DC bus, the total closed-loop input impedance of the device-regulating converts can be approximated as a positive/negative incremental resistance, with the magnitude varying with the net power. It may result in significant stability problems, since the impedance interaction is the root of the instability in a source-load interconnected system [5].

To solve the stability issues caused by impedance interaction, several passive damping methods [6,7] and active stabilization methods [8,9] have been proposed. Passive damping methods use passive components, such as resistors, capacitors and inductors, to improve the system stability. Active stabilization methods, on the other hand, usually use some advanced control methods to change the output impedance of the line regulator, so as to avoid the impedance interaction.

However, in a standalone DC microgrid, the regulation of the DC bus is implemented by distributed RES or ESD converters. They should not only be able to regulate the rest of the system in a stable manner, but also operate their own devices efficiently and provide the required protection, such as current limitation. As a result, simple linear control methods are preferred in the design of distributed power converters. The purpose of this work is to develop dynamic models of the distributed converters in a standalone DC microgrid, by which average current mode control and linear compensators could be employed in the control of these converters, so as to improve the performance and stability of the system.

This paper is organized as follows. The configuration and operation of the standalone DC microgrid under study are provided in Section 2. In Section 3, dynamic models of the distributed power converters are developed from two aspects, device-regulating mode and bus-regulating mode. Necessary transfer functions for compensator design are derived from these models. The stability of the entire system is analyzed at last. In Section 4, the operation and control design of the system are verified by simulation results. Section 5 concludes this paper.

2. System Configuration and Operation

Figure 1a shows a simplified architecture of the standalone DC microgrid studied in this work, which is composed of distributed PV arrays, DC loads and battery packs. The target system is based on a 48-V DC bus. These kinds of low voltage DC microgrids have been widely used in residential applications, remote communication stations and data centers [10–12]. To reduce the development time and cost, as well as to simplify the operation of the system, as shown in Figure 1b, all distributed power sources or loads are interfaced to the DC bus via identical 500-W non-inverting four-switch buck-boost converters, considering their capabilities of bidirectional power flow and voltage step up/down. Very high efficiency over a wide range of operating voltages has already been demonstrated using this topology [13,14].

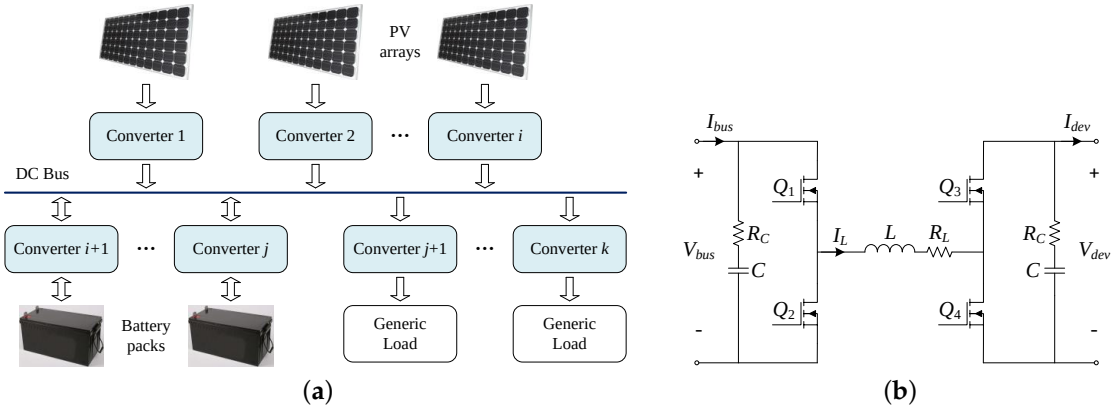

Figure 1. (**a**) Architecture of the standalone DC microgrid. (**b**) Power stage of the adopted bidirectional non-inverting buck-boost converter.

Different operating modes of the standalone DC microgrid are summarized in Table 1. Modes I and II correspond to the case when PV arrays operate in the maximum power point tracking (MPPT) mode, while the DC bus is regulated by the battery packs. Mode III refers to the case when the maximum output power of the PV arrays is greater than the total power demanded by batteries and

loads. In this case, to protect the batteries from overcharging, battery charging current is limited; thus, PV converters have to take over the task of bus regulation. In Mode IV, the demanded load power is greater than the total maximum power of PV arrays and battery packs. At this point, load shedding is required in order to maintain the system stability. A simple load shedding scheme based on voltage thresholds can be seamlessly applied [15]; therefore, Mode IV will not be discussed in this paper.

Table 1. Operating modes of the standalone DC microgrid.

System Mode	PV Mode	Battery Mode	Load Mode
Mode I	MPPT (device)	Discharging (bus)	Normal (device)
Mode II	MPPT (device)	Charging (bus)	Normal (device)
Mode III	Off-MPPT (bus)	Charging (device)	Normal (device)
Mode IV	MPPT (device)	Discharging (bus)	Shedding (device)

From Table 1, it can be concluded that in each operating mode of the standalone DC microgrid, all distributed power converters can be divided into two groups depending on their respective responsibilities: bus-regulating converters and device-regulating converters. PV converters or battery converters take charge of the bus regulation based on the states of the batteries and the voltage level of the DC bus. The rule of the transitions between bus-regulating mode and device-regulating mode is shown in Figure 2. Battery converters switch from the bus-regulating mode to the device-regulating mode when the battery voltage V_{bat} reaches the fully-charged voltage $V_{bat,ref}$, while the charging current I_{charge} is still positive, and switch back to the bus-regulating mode when the bus voltage V_{bus} is less than its reference value $V_{bus,ref}$. In the case of PV converters, they switch from the device-regulating mode to the bus-regulating mode when $V_{bus} \geq 1.1V_{bus,ref}$ and switch back to the device-regulating mode when $V_{bus} \leq 1.05V_{bus,ref}$. It should be noted that there is an intermediate state during the transition when both battery converters and PV converters are working in the device-regulating mode. During that state, V_{bus} keeps changing until the next threshold is reached.

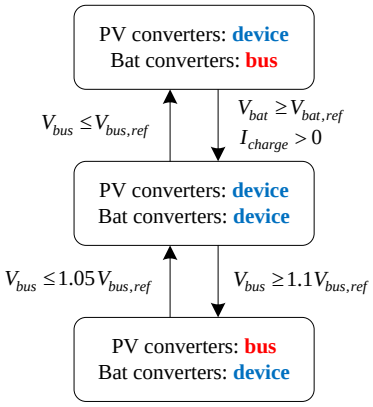

Figure 2. Diagram of the transitions between bus-regulating mode and device-regulating mode.

Based on the above classification, a demonstration circuit diagram of the DC microgrid is shown in Figure 3a, where m converters work in the bus-regulating mode and n converters work in the device-regulating mode. The well-known droop control method [16] is adopted in the bus regulation to guarantee that several distributed converters can operate on the bus simultaneously. Assuming the control loops are well designed in each converter, the bus port of a bus-regulating converter behaves as a voltage source $V_{bus,i}$ in series with a droop resistance $R_{droop,i}$, while the device port of a device-regulating converter behaves as a constant voltage source $V_{dev,j}$. Meanwhile, considering the high efficiency of these converters, the device ports of bus-regulating converters and the bus ports

of device-regulating converters can be regarded as constant power sinks/sources depending on the direction of the power flow.

When only the effect of each converter with respect to the bus is taken into account, an equivalent circuit diagram of the standalone DC microgrid is obtained in Figure 3b. All of the bus-regulating power modules can be represented as a Thevenin equivalent source ($V_{bus,eq}$, $R_{droop,eq}$), where $R_{droop,eq} = R_{droop,1} \parallel \cdots \parallel R_{droop,m}$, and $V_{bus,eq} = R_{droop,eq} \sum_{i=1}^{m} (V_{bus,i}/R_{droop,i})$. All of the device-regulating power modules can be combined into a power source/sink $P_{dev,eq} = \sum_{j=1}^{n} P_{dev,j}$.

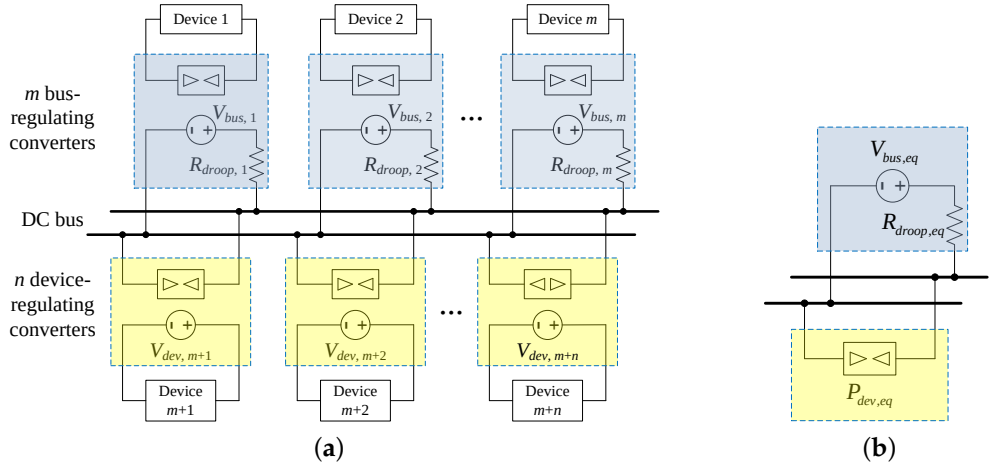

Figure 3. (**a**) Circuit diagram of the DC microgrid where m converters work in the bus-regulating mode and n converters work in the device-regulating mode. (**b**) Equivalent circuit diagram.

3. Dynamic Modeling and Control Design

The modeling and control design of the distributed converters in a standalone DC microgrid will be discussed from two aspects: device-regulating mode and bus-regulating mode.

3.1. Closed-Loop Input Impedance of the Device-Regulating Converters

The small-signal averaged circuit model of a device-regulating converter is shown in Figure 4, where Z_{dev} represents the input impedance of the device. The adopted bidirectional buck-boost converter is supposed to work in the buck mode when $V_{bus} > V_{dev}$ and work in the boost mode when $V_{bus} < V_{dev}$. Only the continuous conduction mode (CCM) is considered here for simplification, since the device-regulating converters work in CCM for most cases. In the circuit model, the output impedance of bus-regulating converters is assumed to be zero, while the effect of the non-zero output impedance of bus-regulating converters on the dynamics of a device-regulating converter will be discussed in Section 3.3.

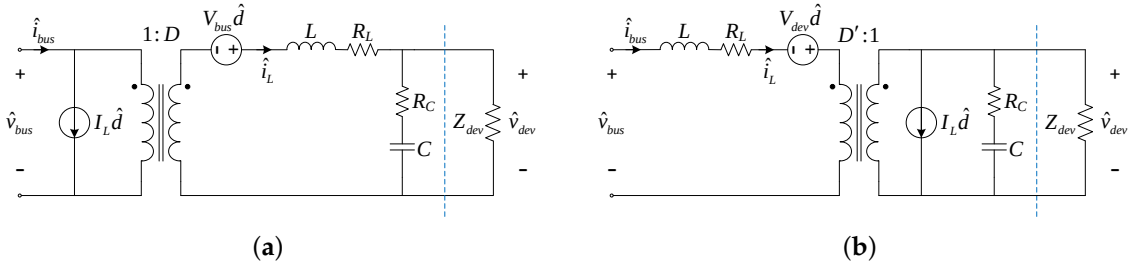

Figure 4. Averaged small-signal circuit of a device-regulating converter when it operates in (**a**) the buck mode or in (**b**) the boost mode.

In the device-regulating converter, the average current mode control method is adopted to simplify the feedback control design, as well as to provide the required current limitation. The small-signal control block diagram of a device-regulating converter is shown in Figure 5. $G_{id}(s)$ and $G_{vd}(s)$ are the transfer functions from control variable $\hat{d}$ to inductor current $\hat{i}_L$ and device voltage $\hat{v}_{dev}$. $G_{ig}(s)$ and $G_{vg}(s)$ are the transfer functions from input voltage $\hat{v}_{bus}$ to inductor current $\hat{i}_L$ and device voltage $\hat{v}_{dev}$. $H_i(s)$ and $H_v(s)$ are the current and the voltage sensing gains. $G_{ci}(s)$ and $G_{co}(s)$ are the compensators of the inner current loop and outer voltage loop, respectively, and G_m is the gain of the pulse width modulator. The derivations of $G_{id}(s)$, $G_{vd}(s)$, $G_{ig}(s)$ and $G_{vg}(s)$ for a device-regulating converter working in the buck mode or boost mode are expressed in Table 2, where $Z_{load} = Z_C \parallel Z_{dev}$, $Z_C = 1/sC + R_C$ and $Z_L = sL + R_L$. In the control design, the target crossover frequency of the inner current loop is $f_{ci} = f_{sw}/10$, while that of the outer voltage loop is $f_{co} = f_{ci}/10$, where f_{sw} is the converter switching frequency. The detailed design of the average current mode control for a device-regulating converter is a classic topic [17,18], so it will not be discussed here.

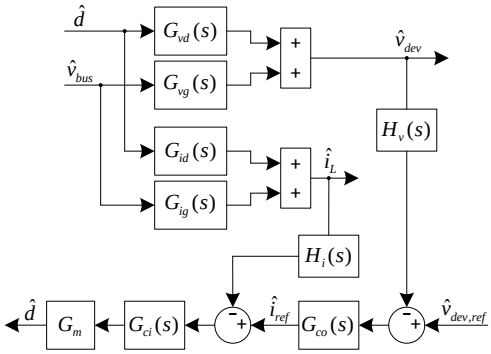

Figure 5. The small-signal control block diagram of a device-regulating converter.

Table 2. The derivations of $G_{id}(s)$, $G_{vd}(s)$, $G_{ig}(s)$ and $G_{vg}(s)$.

Transfer Function	Buck Mode	Boost Mode
$G_{id}(s)$	$\frac{V_{bus}}{Z_L + Z_{load}}$	$\frac{V_{dev} + D' I_L Z_{load}}{Z_L + D'^2 Z_{load}}$
$G_{vd}(s)$	$G_{id}(s) Z_{load}$	$(D' G_{id}(s) - I_L) Z_{load}$
$G_{ig}(s)$	$\frac{D}{Z_L + Z_{load}}$	$\frac{1}{Z_L + D'^2 Z_{load}}$
$G_{vg}(s)$	$G_{ig}(s) Z_{load}$	$G_{ig}(s) D' Z_{load}$

To derive the closed-loop input impedance of a device-regulating converter, the control loops depicted in Figure 5 are expressed as Equation Set 1

$$\begin{cases} \hat{d} G_{vd}(s) + \hat{v}_{bus} G_{vg}(s) = \hat{v}_{dev} \\ \hat{d} G_{id}(s) + \hat{v}_{bus} G_{ig}(s) = \hat{i}_L \\ -\hat{v}_{dev} H_v(s) G_{co}(s) = \hat{i}_{ref} \\ \left(\hat{i}_{ref} - \hat{i}_L H_i(s)\right) G_{ci}(s) G_m = \hat{d} \end{cases} \quad (1)$$

The converter input current $\hat{i}_{bus}$ can be expressed as the linear combination of $\hat{i}_L$ and $\hat{d}$ as below:

$$\hat{i}_{bus} = M \hat{i}_L + j\hat{d} \quad (2)$$

where $M = D, j = I_L$ in the buck mode and $M = 1, j = 0$ in the boost mode. Combining Equations 1 and 2, the closed-loop input impedance of a device-regulating converter is derived as:

$$Z_{in} = \frac{\hat{v}_{bus}}{\hat{i}_{bus}} = \frac{1 + G_{vd}H_vG_{co}G_{ci}G_m + G_{id}H_iG_{ci}G_m}{MG_{ig}(1 + G_{vd}H_vG_{co}G_{ci}G_m) - (j + MG_{id})G_{vg}H_vG_{co}G_{ci}G_m - jG_{ig}H_iG_{ci}G_m} \tag{3}$$

Figure 6 shows a comparison between the derived closed-loop input impedance Z_{in} and the incremental resistance R_{in} of a device-regulating converter when it operates at full power (500 W), where subscripts *buck* and *boost* represent that the converter works in the buck or boost mode. It can be seen that the incremental resistance R_{in} is a good approximation to Z_{in} below the crossover frequency (f_{co} = 1 kHz) of the converter's outer loop. Key parameters of the bidirectional buck-boost converter are shown in Table 3. Other parameters used in this example are $V_{dev,buck}$ = 24 V and $V_{dev,boost}$ = 72 V. The incremental resistance R_{in} is derived based on $R_{in} = -V_{bus}^2/P_{dev}$, which assumes no losses exist in a device-regulating converter, and it behaves as a constant power load/source. P_{dev} is positive when the power is transferred from the DC bus to the device.

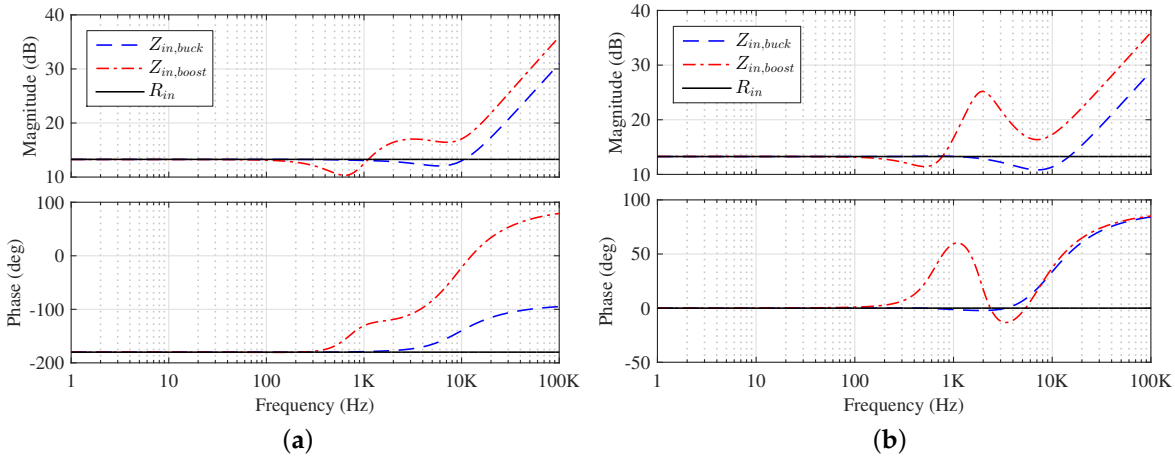

Figure 6. Comparison between the closed-loop input impedance Z_{in} and incremental resistance R_{in} of a device-regulating converter when (**a**) $P_{dev} > 0$ and (**b**) $P_{dev} < 0$.

Table 3. Key parameters of the bidirectional buck-boost converter.

L	R_L	C	R_C	f_{sw}	G_m	$H_{i(s)}$	$H_{v(s)}$
100 μH	10 mΩ	1 mF	150 mΩ	100 kHz	1	$\frac{1}{1+\frac{s}{\pi f_{sw}}}$	$\frac{1}{1+\frac{s}{\pi f_{sw}/5}}$

In a standalone DC microgrid, n device-regulating converters operate on the bus simultaneously. Thus, the total closed-loop input impedance $Z_{in,dev}$ of these converters can be expressed as the parallel combination of their respective input impedance Z_{in}

$$\frac{1}{Z_{in,dev}} = \sum_{j=1}^{n} \frac{1}{Z_{in,j}} \approx \sum_{j=1}^{n} \left(-\frac{P_{dev,j}}{V_{bus}^2} \right) = -\frac{P_{dev,net}}{V_{bus}^2} \tag{4}$$

From Equation 4, it can be concluded that the input impedance $Z_{in,dev}$ is determined by the net power $P_{dev,net}$ of the device-regulating converters. When $P_{dev,net} < 0$, which means the direction of the net power is towards the DC bus, $Z_{in,dev}$ can be approximated as a positive resistance at frequencies below f_{co}. On the contrary, typical negative resistance appears when $P_{dev,net} > 0$.

3.2. Modeling and Control Design of the Bus-Regulating Converters

In a standalone DC microgrid, PV or battery converters work as the bus-regulating converters. Since a relatively low bus voltage of 48 V is chosen in this work, both PV and battery converters can easily be configured working in the buck mode. Figure 7 shows a circuit diagram where m bus-regulating converters and n device-regulating converters are interfaced to the DC bus. $Z_{in,1} - Z_{in,n}$ represent the closed-loop input impedance of device-regulating converters. $Z_{bus,1} - Z_{bus,m+n}$ represent the line impedance.

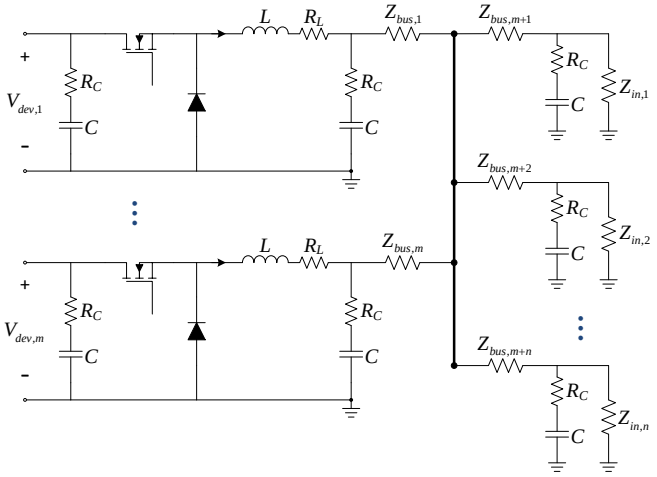

Figure 7. Circuit diagram of the bus-regulating converters.

To develop the dynamic model of a bus-regulating converter, $Z_{in,1} - Z_{in,n}$, $Z_{bus,1} - Z_{bus,m+n}$ and Z_C can be combined into a single impedance $Z_{in,tot}$ to represent their overall dynamics. When bus-regulating Converter 1 is analyzed, $Z_{in,tot}$ can be expressed as:

$$Z_{in,tot} = Z_C \parallel \left(Z_{bus,1} + \frac{1}{\sum_{i=2}^{m} \frac{1}{Z_C + Z_{bus,i}} + \sum_{j=1}^{n} \left(\frac{1}{\frac{Z_C Z_{in,j}}{Z_C + Z_{in,j}} + Z_{bus,m+j}} \right)} \right) \tag{5}$$

Actually, a simplified expression of $Z_{in,tot}$ can be derived as $Z_{in,tot} = Z_{C,tot} \parallel Z_{in,dev}$ if the bus impedance is neglected, where $Z_{C,tot}$ is the total impedance of all bus capacitors.

The averaged small-signal circuit of a bus-regulating converter is depicted in Figure 8; R_{dev} is the equivalent small-signal resistance of the battery pack (R_{bat}) or PV array (R_{pv}). Both the CCM and the discontinuous conduction mode (DCM) are taken into account in the small-signal model, since the power processed by the bus-regulating converters varies with the net power $P_{dev,net}$ of device-regulating converters.

In this work, the small-signal model of the battery pack is represented as a voltage source $\hat{v}_{bat}$ connected in series with its internal resistance R_{bat}. The small-signal model of the PV array is represented as a current source $\hat{i}_{pv}$ paralleled with a resistance R_{pv}, in which R_{pv} is obtained by the linearization of the nonlinear current-voltage curve of the PV array at its steady-state operating point. Values of R_{pv} used in this work are shown in Figure 9, which are obtained from a PV array model consisting of two series-connected Conergy P 175M PV modules.

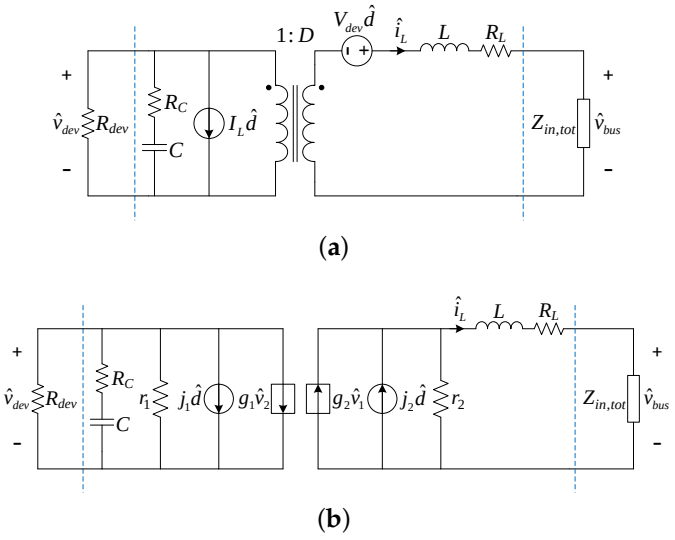

Figure 8. Averaged small-signal circuit of a bus-regulating converter when it works in (**a**) continuous conduction mode (CCM) or in (**b**) discontinuous conduction mode (DCM).

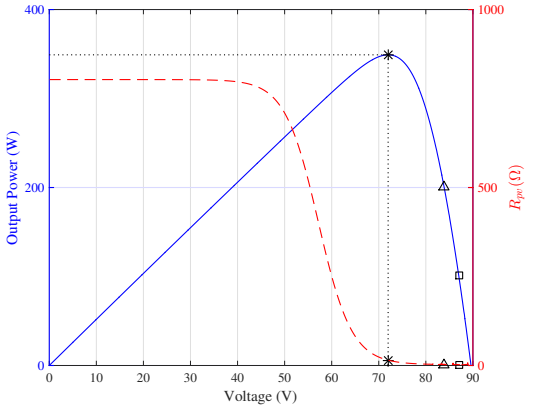

Figure 9. Linearized resistance R_{pv} of a PV array consisting of two series-connected Conergy P 175M PV modules when the solar irradiance is 1000 W/m^2 and the temperature is 25 °C.

When a bus-regulating converter works in CCM, the transfer functions of control to inductor current $G_{id,CCM}(s)$ and inductor current to bus voltage $G_{vi,CCM}(s)$ are derived as follows:

$$G_{id,CCM}(s) = \frac{\hat{i}_L}{\hat{d}} = \frac{V_{dev} - DI_L Z_g}{D^2 Z_g + Z_L + Z_{in,tot}} \tag{6}$$

$$G_{vi,CCM}(s) = \frac{\hat{v}_{bus}}{\hat{i}_L} = Z_{in,tot} \tag{7}$$

where $Z_g = R_{dev} \parallel Z_C$. In DCM, the transfer functions of $G_{id,DCM}(s)$ and $G_{vi,DCM}(s)$ are obtained as follows:

$$G_{id,DCM}(s) = \frac{\hat{i}_L}{\hat{d}} = \frac{j_2 Z_{load} - g_2 j_1 Z_g Z_{load}}{(1 + g_1 g_2 Z_g Z_{load})(Z_L + Z_{in,tot})} \tag{8}$$

$$G_{vi,DCM}(s) = \frac{\hat{v}_{bus}}{\hat{i}_L} = Z_L + Z_{in,tot} \tag{9}$$

where $Z_g = R_{dev} \parallel Z_C \parallel r_1$ and $Z_{load} = r_2 \parallel (Z_L + Z_{in,tot})$. The parameters used in DCM are shown in Table 4, where $R_e = [(2/M - 1)^2 - 1]R/4$, and M is the voltage conversion ratio [19].

Table 4. Parameters of the small-signal DCM model for the buck converter.

g_1	j_1	r_1	g_2	j_2	r_2
$\frac{1}{R_e}$	$\frac{2(1-M)V_{dev}}{DR_e}$	R_e	$\frac{2-M}{MR_e}$	$\frac{2(1-M)V_{dev}}{DMR_e}$	M^2R_e

The control block diagram of the bus-regulating converters is shown in Figure 10. To provide the required current limitation, average current mode control is also tried in the bus-regulating converters. The droop control method is adopted in the outer control loop for the purpose of current sharing.

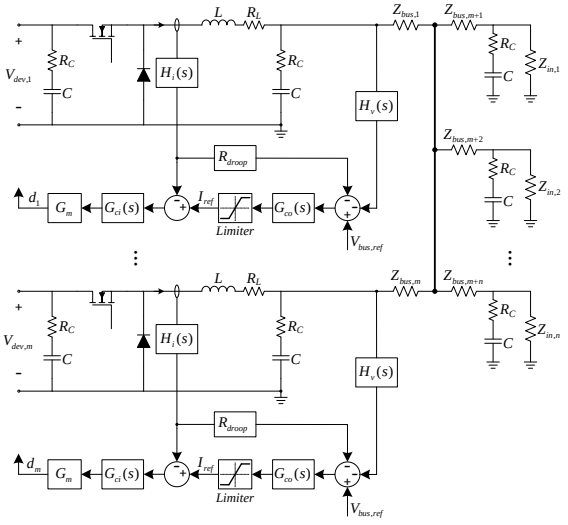

Figure 10. The control block diagram of bus-regulating converters.

The resulting expressions for the inner current-loop gain $T_i(s)$ and outer voltage-loop gain $T_v(s)$ are shown below:

$$T_i(s) = G_{id}(s)H_i(s)G_{ci}(s)G_m \tag{10}$$

$$T_v(s) = \frac{T_i(s)/H_i(s)}{1 + T_i(s)}\Big(G_{vi}(s)H_v(s) + H_i(s)R_{droop}\Big)G_{co}(s) \tag{11}$$

where $G_{ci}(s)$ and $G_{co}(s)$ are the compensators for the inner current loop and outer voltage loop, respectively. To achieve the desired crossover frequency and phase margin, different inner compensators $G_{ci,CCM}(s)$ and $G_{ci,DCM}(s)$ are designed according to the conduction mode of the inductor current. Whereas, the outer loop $T_v(s)$ is compensated using the same $G_{co}(s)$. The detection of the conduction mode is implemented using the method in [20].

It is a common practice to assume a resistive load in the control design of switching regulators. In this work, control loops $T_i(s)$ and $T_v(s)$ are designed based on $Z_{in,dev}$ when the net power $P_{dev,net}$ of device-regulating converters is negative, since in this case, the total closed-loop input impedance $Z_{in,dev}$ of device-regulating converters behaves as a positive resistance at low frequencies. Bode plots of $T_i(s)$ and $T_v(s)$ of a bus-regulating converter when it operates at -300 W (CCM) and -20 W (DCM) are shown in Figure 11, where $G_{ci,CCM}(s)$, $G_{ci,DCM}(s)$ and $G_{co}(s)$ are realized by PI compensators. Key parameters used in this example are m = 2, n = 6, V_{dev} = 60 V, R_{dev} = 20 mΩ, Z_{bus} = 10 mΩ and R_{droop} = 25 mΩ. It can be seen that no right half-plane (RHP) zeroes or poles appear in the loop gains, so the

stability and dynamic behavior of the converter could be analyzed using the Bode plots. As shown in the figure, the inner-loop crossover frequency f_{ci} is 10 kHz, and the outer-loop crossover frequency f_{co} is 1 kHz, which all meet the design requirements, $f_{ci} = f_{sw}/10$ and $f_{co} = f_{ci}/10$. The phase margins of $T_{i,CCM}$ and $T_{i,DCM}$ are 65° and 88°, while the phase margins of $T_{v,CCM}$ and $T_{v,DCM}$ are 70° and 64°, respectively.

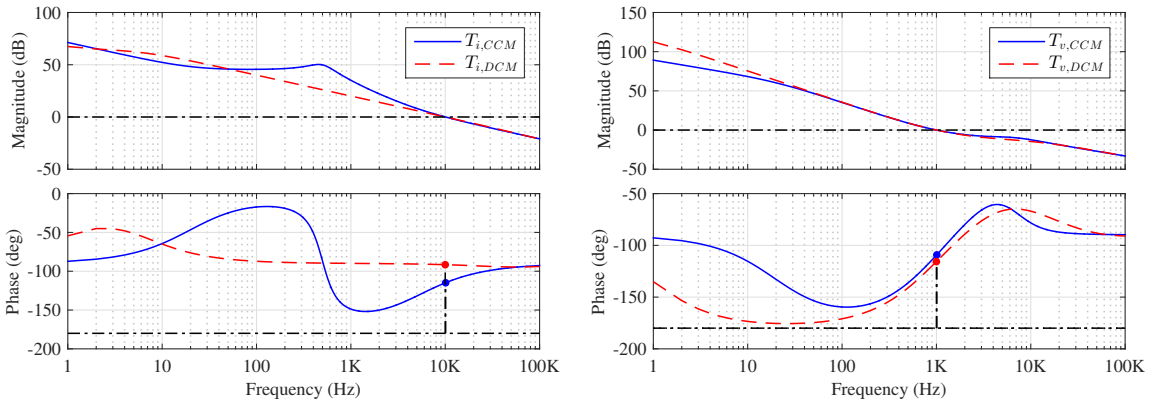

Figure 11. Bode plots of (**a**) $T_i(s)$ and (**b**) $T_v(s)$ when $P_{dev,net} < 0$.

However, when $P_{dev,net}$ is positive, $Z_{in,dev}$ behaves as a negative resistance at low frequencies, which results in one RHP zero in $T_i(s)$ and one RHP pole in $T_v(s)$. The RHP zero and pole could be calculated numerically, and the effects of the RHP zeroes (circles) and poles (stars) can be observed in the Bode plots shown in Figure 12. In this figure, $T_i(s)$ and $T_v(s)$ are calculated when the bus-regulating converter operates at 300 W (CCM) and 20 W (DCM), and the PI compensators designed above are still employed in the control loops.

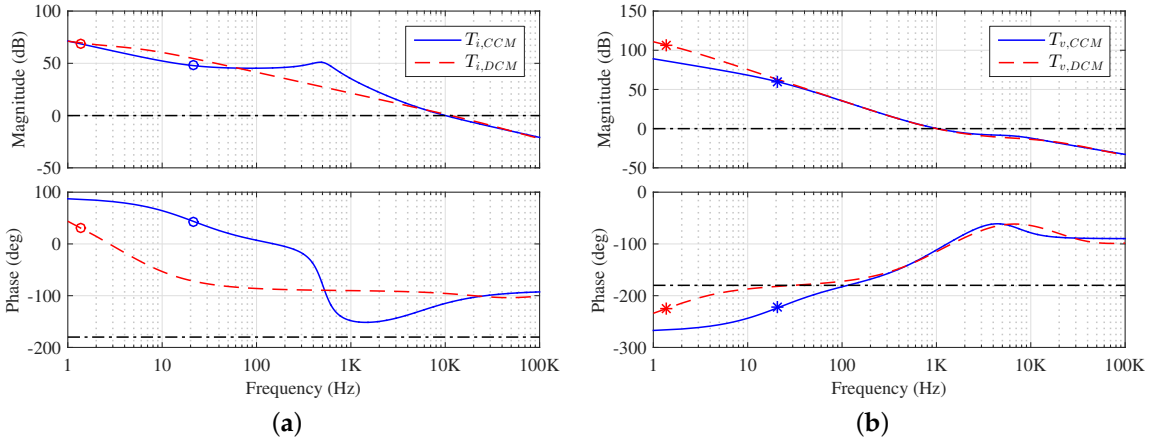

Figure 12. Bode plots of (**a**) $T_i(s)$ and (**b**) $T_v(s)$ when $P_{dev,net} > 0$.

So far, it has been demonstrated that loop gains $T_i(s)$ and $T_v(s)$ of a bus-regulating converter when $P_{dev,net} > 0$ differ substantially from those when $P_{dev,net} < 0$. When $P_{dev,net} > 0$, Bode plots are no longer applicable to the stability analysis, since the RHP zero or pole appears. In order to analyze the stability of the bus-regulating converter, the Nyquist criterion has to be adopted. Actually, it is not difficult to find that the inner current loop $T_i(s)$ is no longer stable when $P_{dev,net} > 0$ by using the Nyquist criterion. However, the stability of a multi-loop controlled converter is not determined by each loop alone, but by both loops working together. For the stability analysis of a bus-regulating

converter, two loop gains $T_1(s)$ and $T_2(s)$ are measured, as shown in Figure 13. Loop gain $T_1(s) = \hat{e}_{y1}/\hat{e}_{x1}$ is measured at Point "1", while loop gain $T_2(s) = \hat{e}_{y2}/\hat{e}_{x2}$ is measured at Point "2", where $\hat{e}_{x1}$ and $\hat{e}_{x2}$ are the small-signal perturbations injected for the measurement of the loop gain and $\hat{e}_{y1}$ and $\hat{e}_{y2}$ are their corresponding responses, respectively. These two loop gains have been verified regarding their importance in the stability analysis of a multi-loop controlled converter in [21].

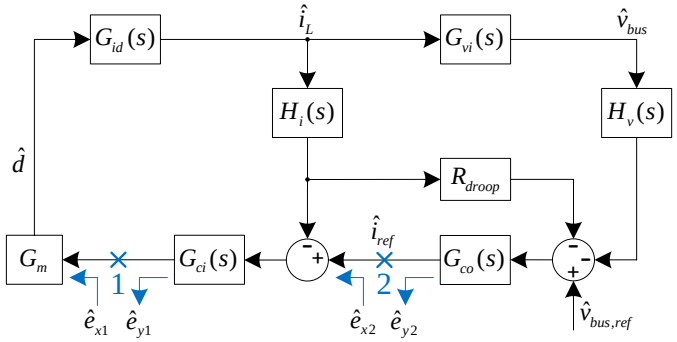

Figure 13. Measurement of the loop gains $T_1(s)$ and $T_2(s)$.

Loop gains $T_1(s)$ and $T_2(s)$ are expressed as follows:

$$T_1(s) = T_i(s) + G_m G_{id}(s)(G_{vi}(s)H_v(s) + H_i(s)R_{droop})G_{co}(s)G_{ci}(s) \tag{12}$$

$$T_2(s) = \frac{T_i(s)/H_i(s)}{1 + T_i(s)}(G_{vi}(s)H_v(s) + H_i(s)R_{droop})G_{co}(s) \tag{13}$$

It is easy to find that actually $T_2(s)$ equals $T_v(s)$; thus, one RHP pole exists in $T_2(s)$. As for $T_1(s)$, second-order poles appear at the original one due to the cascading of PI compensators. The statement of the Nyquist stability criterion for a continuous system is $Z = P - N$, where Z is the number of unstable closed-loop poles, P is the number of unstable open-loop poles and N is the number of counter-clockwise encirclements that the Nyquist plot of the loop gain makes around the $(-1, j0)$ point. Nyquist plots of $T_1(s)$ and $T_2(s)$ are shown in Figure 14. Both $T_1(s)$ and $T_2(s)$ encircle the $(-1, j0)$ point counter-clockwise exactly once $(N = 1)$. As one unstable pole exists in both $T_1(s)$ and $T_2(s)$ $(P = 1)$, the closed-loop system is proven to be stable $(Z = 0)$ when $P_{dev,net}$ is positive.

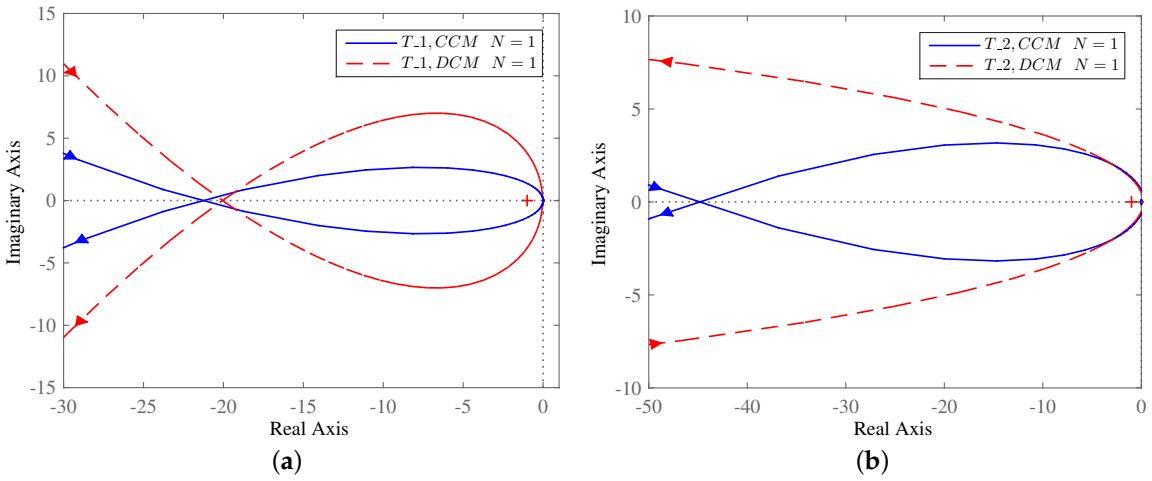

Figure 14. Nyquist plots of (**a**) $T_1(s)$ and (**b**) $T_2(s)$ when $P_{dev,net} > 0$.

While the bus-regulating converter is proven to be stable when $P_{dev,net} > 0$, knowledge of the system relative stability is still necessary for us. As a result, gain and phase margins of $T_1(s)$ and $T_2(s)$ that are defined by the above Nyquist plots are translated into the Bode plots in Figure 15. It can be seen that the control bandwidth of the inner loop is around 10 kHz, while that of the outer loop is 1 kHz, as desired. Fortunately, good system performance can be ensured by the gain and phase margins.

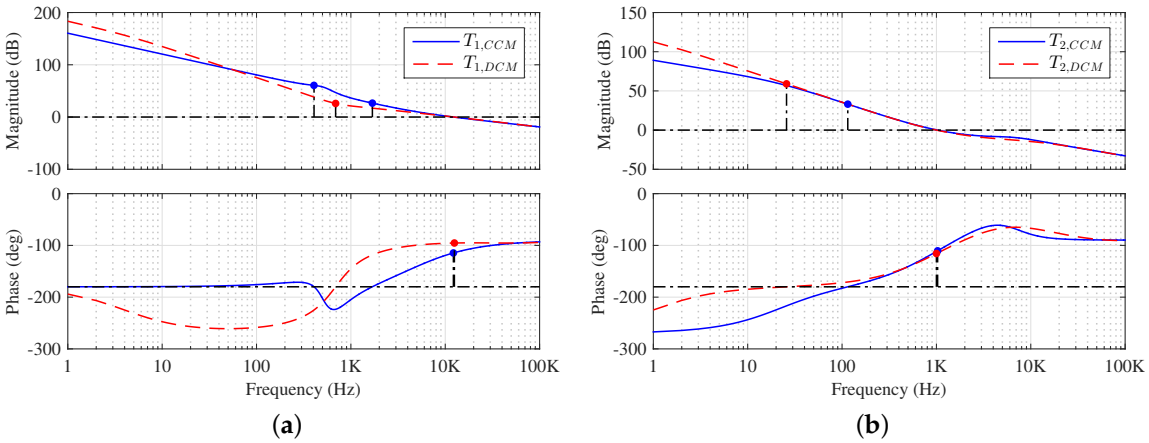

Figure 15. Bode plots of (**a**) $T_1(s)$ and (**b**) $T_2(s)$ with gain and phase margins when $P_{dev,net} > 0$.

Furthermore, to regulate the DC bus voltage, battery and PV converters have to work over a wide range of operating conditions. To guarantee the performance of the bus-regulating converters, loop gains $T_1(s)$ and $T_2(s)$ are evaluated under several representative operating conditions. Three power levels (100 W, 200 W and 350 W) are picked out for the PV converters when the solar irradiance is 1000 W/m^2 and the temperature is 25 °C. The PV output voltages V_{pv} and the small-signal linearized resistances R_{pv} corresponding to the three power levels are marked in squares (100 W), triangles (200 W) and stars (350 W) in Figure 9. Three power levels (100 W, 300 W and 500 W) are also picked out for the battery converters. The battery voltage V_{bat} and its internal series resistance R_{bat} are assumed to be constant (V_{bat} = 60 V, R_{bat} = 20 mΩ) when different power is processed, since their variations are much less compared to the PV array.

Bode plots of $T_1(s)$ and $T_2(s)$ corresponding to the representative operating conditions are shown in Figure 16. It should be appreciated that neither the gain nor the phase changes significantly over the power levels, device voltages or small-signal device resistances, especially at the crossover frequency. Similar results could also be obtained under other operating conditions, which allows one to conclude that the simple PI compensators designed for the bus-regulating control loops can be implemented under different operating conditions within a reasonable range.

3.3. Stability Analysis of the DC Microgrid

Based on the control loops designed in the above subsection (Figure 13), the closed-loop output impedance Z_{out} of a bus-regulating converter can be derived as follows:

$$\begin{cases} -\left(\hat{i}_L H_i(s) R_{droop} + \hat{v}_{bus} H_v(s)\right) G_{co}(s) = \hat{i}_{ref} \\ \left(\hat{i}_{ref} - \hat{i}_L H_i(s)\right) G_{ci}(s) G_m = \hat{d} \\ \hat{d} G_{id}(s) G_{vi}(s) = \hat{v}_{bus} \end{cases} \tag{14}$$

$$Z_{out} = -\frac{\hat{v}_{bus}}{\hat{i}_L} = \frac{H_i(R_{droop} G_{co} + 1) G_{ci} G_m G_{id} G_{vi}}{1 + H_v G_{co} G_{ci} G_m G_{id} G_{vi}} \tag{15}$$

Actually, the magnitude of Z_{out} is verified to be quite close to R_{droop} due to the adoption of the droop control method and average current mode control.

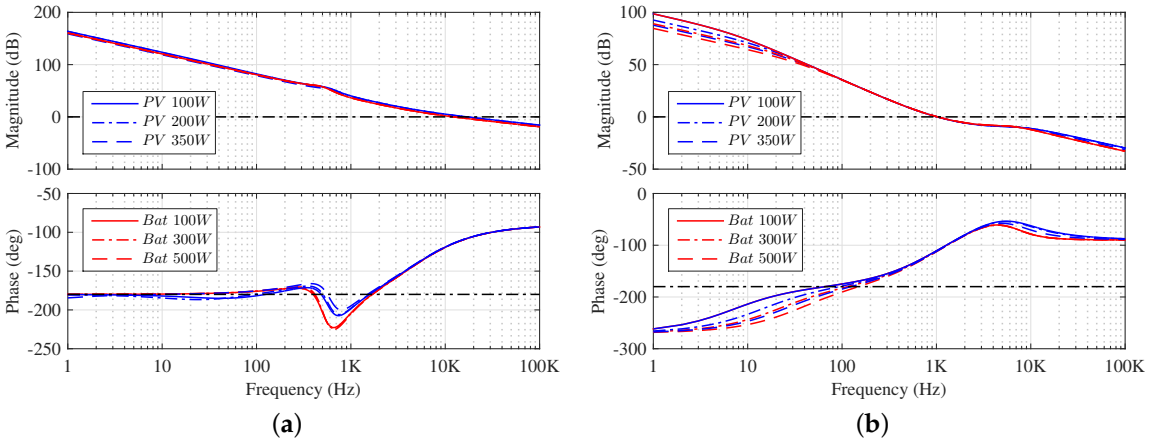

Figure 16. Bode plots of (**a**) $T_1(s)$ and (**b**) $T_2(s)$ when the bus-regulating converter works at different steady-state operating points.

A small-signal equivalent circuit of the standalone DC microgrid can then be obtained in Figure 17, where m converters work in the bus-regulating mode and n converters work in the device-regulating mode. Small-signal Thevenin sources ($\hat{v}_{bus,i}$, $Z_{out,i}$) are used to model the closed-loop dynamics of the bus-regulating converters.

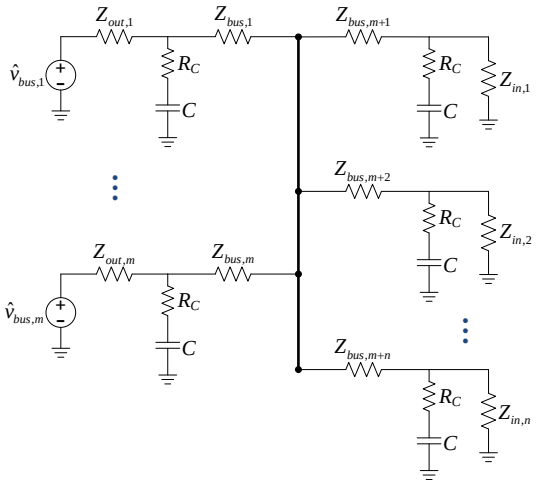

Figure 17. Small-signal equivalent circuit of the standalone DC microgrid.

However, when the closed-loop input impedance $Z_{in,1} - Z_{in,n}$ is derived in Subsection *3.1*, it is assumed that the output impedance $Z_{out,1} - Z_{out,m}$ of bus-regulating converters is zero. Therefore, it needs to be determined that whether the transfer functions ($G_{id}(s)$, $G_{vd}(s)$) that were used to derive $Z_{in,1} - Z_{in,n}$ in Subsection *3.1* are modified by the none-zero output impedance $Z_{out,1} - Z_{out,m}$. Middlebrook's extra element theorem (EET) [5,19] is employed here to determine how the addition of $Z_{out,1} - Z_{out,m}$ alters these transfer functions. Take $G_{vd}(s)$ as an example. The modified transfer function can be expressed as follows:

$$G_{vd}(s) = \left(G_{vd}(s)\big|_{Z_{out,tot}=0}\right)\frac{1+\frac{Z_{out,tot}}{Z_N}}{1+\frac{Z_{out,tot}}{Z_D}} \tag{16}$$

where $G_{vd}(s)|_{Z_{out,tot}=0}$ is the transfer function $G_{vd}(s)$ derived in Section 3.1 and $Z_{out,tot}$ is the combination of $Z_{out,1} - Z_{out,m}$, $Z_{bus,1} - Z_{bus,m+n}$ and Z_C. When device-regulating Converter 1 is analyzed, $Z_{out,tot}$ can be expressed as below:

$$Z_{out,tot} = Z_C \parallel \left(Z_{bus,m+1} + \frac{1}{\sum_{i=1}^{m} \frac{1}{\frac{Z_C Z_{out,i}}{Z_C + Z_{out,i}} + Z_{bus,i}} + \sum_{j=2}^{n} \left(\frac{1}{Z_C + Z_{bus,m+j}} \right)} \right) \tag{17}$$

Additionally, a simplified expression of $Z_{out,tot}$ is derived as below if the bus impedance is neglected:

$$\frac{1}{Z_{out,tot}} = \sum_{i=1}^{m} \frac{1}{Z_{out,i}} + \frac{1}{Z_{C,tot}} \tag{18}$$

The definition and derivation of the impedance Z_N and Z_D for a device-regulating converter are described in Table 5.

Table 5. Definition and derivation of Z_N and Z_D for a device-regulating converter.

	Z_N	Z_D
Definition	$\frac{\hat{v}_{bus}}{\hat{i}_{bus}}\Big\|_{\hat{v}_{dev}\to 0}$	$\frac{\hat{v}_{bus}}{\hat{i}_{bus}}\Big\|_{\hat{d}=0}$
Buck mode	$-\frac{V_{bus}}{DI_L}$	$\frac{1}{D^2}\left(Z_L + \frac{Z_{dev}Z_C}{Z_{dev}+Z_C}\right)$
Boost mode	$Z_L - \frac{V_{dev}D'}{I_L}$	$Z_L + D'^2\frac{Z_C Z_{dev}}{Z_C + Z_{dev}}$

From Equation 16, it can be easily obtained that when the inequalities of $\|Z_{out,tot}\| \ll \|Z_N\|$ and $\|Z_{out,tot}\| \ll \|Z_D\|$ are satisfied, $G_{vd}(s) \approx G_{vd}(s)|_{Z_{out,tot}=0}$, which means the control loops of the device-regulating converter are not interfered with obviously. Therefore, the comparison between $\|Z_{out,tot}\|$ and $\|Z_N\|$, $\|Z_D\|$ needs to be implemented. A standalone DC microgrid, which consists of eight distributed power modules, is taken as an example, where two battery converters work in the bus-regulating mode; three PV converters and three load converters work in the device-regulating mode. The power processed by each converter is listed as follows: P_{bat} = 300 W, P_{pv} = 300 W and P_{load} = 500 W. The comparison result is shown in Figure 18, where both the load converter (buck mode) and the PV converter (boost mode) are analyzed. It can be concluded that the control loops of the device-regulating converter are not affected significantly by the non-zero output impedance of the bus-regulating converters, since a wide separation can be observed between $\|Z_{out,tot}\|$ and $\|Z_N\|$, $\|Z_D\|$. Therefore, the closed-loop input impedance $Z_{in,1} - Z_{in,n}$ derived in Subsection *3.1* is proven to be a good approximation to the value when $\|Z_{out,tot}\|$ is taken into account.

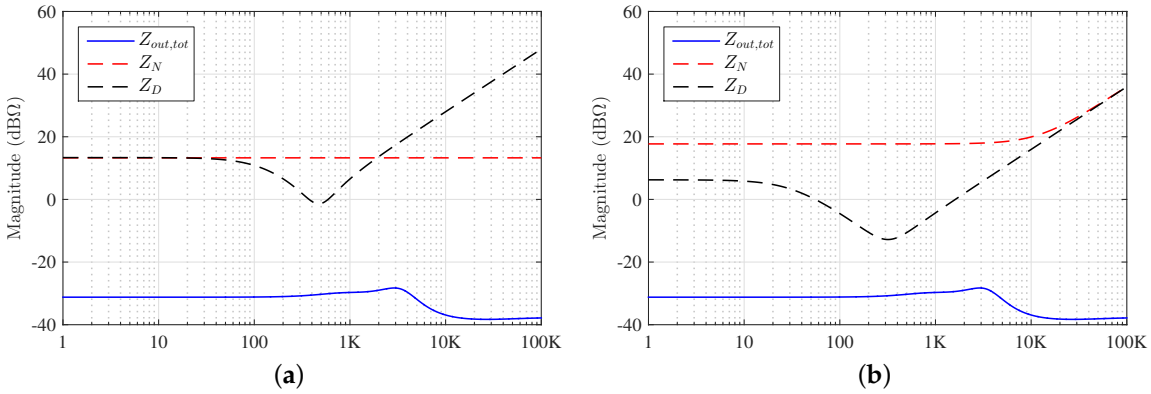

Figure 18. Comparison between $\|Z_{out,tot}\|$ and $\|Z_N\|$, $\|Z_D\|$ when (**a**) the load converter or (**b**) the PV converter is analyzed.

Since it has already been verified in Section 3.2 that the stability and performance of the designed bus-regulating control loops are not affected considerably by the input impedance of device-regulating converters, a low degree of interaction among the distributed converters can be predicted in the designed standalone DC microgrid, and the system is stable.

4. Simulation Results

In order to verify the control design of distributed power converters in a standalone DC microgrid integrated with distributed PV arrays and battery packs, system simulations have been carried out using SimPowerSystems/Simulink. A schematic diagram of the simulated standalone DC microgrid is shown in Figure 19. The simulated system consists of three distributed PV arrays, two battery packs and three resistive loads. All of these distributed devices are connected to a 48-V DC bus via identical 500-W bidirectional buck-boost converters.

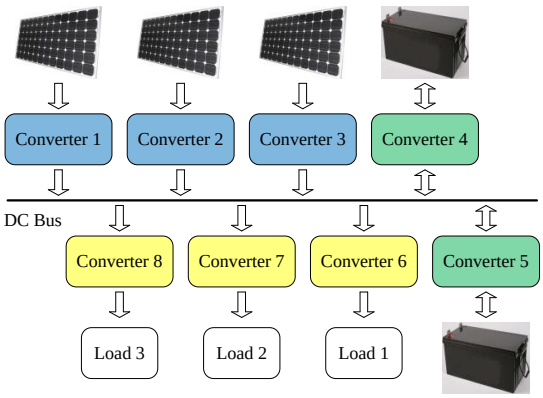

Figure 19. Schematic diagram of the simulated standalone DC microgrid.

The configuration of the simulated standalone DC microgrid is shown in Table 6. For the consideration of a stable operation of the system, the maximum discharging power of the battery packs, as well as the maximum output power of the PV arrays, is greater than the total power demand of the loads. In this simulation, a PV array model is chosen from the library of SimPowerSystems, which is composed of two Conergy P 175M modules connected in series. To emulate the fully-charged status of the battery in a short time, a simple model of the battery pack is adopted, which consists of an ideal voltage source in series with a constant internal resistance.

Table 6. Configuration of the standalone DC microgrid in simulation.

	Type	**Conergy P 175M**
PV array	Configuration	$N_p = 1, N_s = 2$
	Open-circuit voltage V_{oc}	89.6 V
	Short-circuit current I_{sc}	5.17 A
	MPP voltage V_{mpp}	72 V
	MPP current I_{mpp}	4.86 A
	Maximum power P_{mpp}	350 W
Battery Pack	Nominal voltage	60 V
	Fully charged voltage $V_{bat,ref}$	65 V
	Internal Resistance R_{bat}	100 mΩ
Load	Rating of Load 1	12 V, 200 W
	Rating of Load 2	72 V, 300 W
	Rating of Load 3	24 V, 400 W

In the simulation, operation events of the distributed devices over a time span of 1 s are scheduled in Table 7. During this time, a sequence of events takes place, emulating different operating modes (Mode I to III) of the standalone DC microgrid, as mentioned in Table 1, and possible transitions between these modes. Since this work is focused on the dynamic modeling and control, to facilitate the observation of the dynamic responses of the system, all of the operation events are scheduled in a short time span of 1 s, which is made possible since the control bandwidth of every distributed converter is designed to be 1 kHz.

Table 7. Operation events scheduled in the simulation.

Time (s)	**Solar Irradiance**
0 to 0.3	gradually increases from 100 W/m^2 to 900 W/m^2
0.3	Steps from 900 W/m^2 to 1000 W/m^2
0.3 to 0.5	keeps constant at 1000 W/m^2
0.5 to 0.7	gradually decreases from 1000 W/m^2 to 0
0.7 to 1	keeps constant at 0
	Battery Open-circuit Voltage
0 to 0.2	keeps constant at 60 V
0.2 to 0.4	gradually increases from 60 V to 64.8 V
0.4 to 1	keeps constant at 64.8 V
	Loads
0	Loads 1, 2 and 3 are all on
0.1	Load 2 is switched off
0.5	Load 3 is switched off
0.8	Loads 2 and 3 are switched on

Simulation results are shown in Figure 20, where several variables of interest are sampled at the frequency of 100 kHz.

1. From t = 0 to t = 0.395 s: DC bus voltage V_{bus} is regulated by the battery converters, while PV converters work in the MPPT mode. During this time, solar irradiance increases from 100 W/m^2 to 1000 W/m^2. Correspondingly, the simulated DC microgrid works in Mode I from 0 to 0.178 s, but switch to Mode II at 0.178 s. A smooth transition can be observed in Figure 20c thanks to the separate control designs for the CCM and DCM. Besides, smooth responses can be seen in Figure 20b and Figure 20c when step disturbances of the load off and solar irradiance variation occur at the time instants of 0.1 s and 0.3 s, respectively.

2. From t = 0.395 s to t = 0.408 s: To observe the transition from Mode II to Mode III, the battery open-circuit voltage is increased gradually from 60 V to 64.8 V during 0.2 s to 0.4 s. At t = 0.395 s, battery converters detect that V_{bat} reaches the fully-charged voltage $V_{bat,ref}$ and, thus, switch to the device-regulating mode to protect the batteries from overcharging. During this interval, PV converters still work in the MPPT mode. As a consequence, V_{bus} increases steadily.
3. From t = 0.408 s to t = 0.659 s: PV converters switch to the bus-regulating mode when V_{bus} reaches $1.1V_{bus,ref}$ at t = 0.408 s. Smooth responses can be seen in Figure 20e and Figure 20f when the step disturbance of the load off occurs at 0.5 s. Solar irradiance starts to decrease from t = 0.5 s. From t = 0.653 s, the total maximum power generated by the PV arrays starts to be less than the power demand of the device-regulating converters. Consequently, V_{bus} starts to drop. At t = 0.657 s, V_{bus} drops down to $1.05V_{bus,ref}$; PV converter switch back to the MPPT mode accordingly. At t = 0.659 s, V_{bus} drops down to $V_{bus,ref}$; the regulation of V_{bus} is taken over by the battery converters again.
4. From t = 0.659 s to t = 1 s: Loads 2 and 3 are switched on simultaneously at 0.8 s. Smooth step responses can be observed in Figure 20b and Figure 20c.

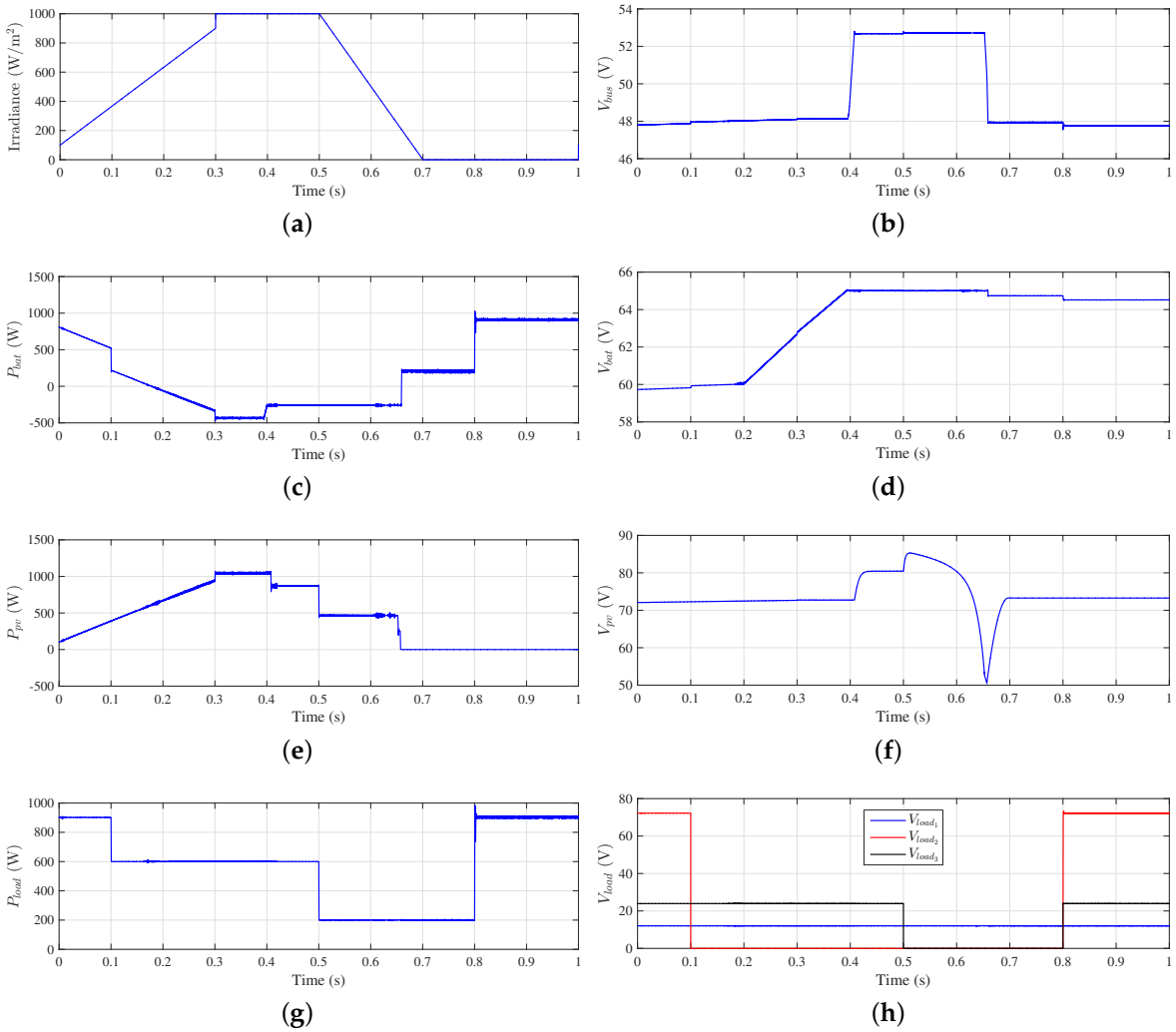

Figure 20. Simulation results. (**a**) Solar irradiance variation. (**b**) DC bus voltage V_{bus}. (**c**) Total charging/discharging power P_{bat} of the two battery packs. (**d**) Battery voltage V_{bat}. (**e**) Total power generation P_{pv} of the three PV arrays. (**f**) PV array voltage V_{pv}. (**g**) Total load power P_{load}. (**h**) Voltages $V_{load_{1,2,3}}$ at three load points.

5. Conclusions

To mitigate the interaction among distributed power modules in a standalone DC microgrid, a modeling and control design procedure for the distributed converters was proposed in this work. First, the system configuration and steady-state analysis of the standalone DC microgrid under study were discussed. Next, the dynamic model of the distributed converters was developed from two aspects, which correspond to their two operating modes, device-regulating mode and bus-regulating mode. Average current mode control and linear compensators were then designed for each corresponding operating mode. The stability of the designed system was analyzed at last. The operation and control design of the system were demonstrated by simulation results using SimPowerSystems/Simulink.

Author Contributions: Xiaodong Lu carried out the main research work and wrote the full manuscript. Jiangwen Wan provided constructive comments in the analysis and modeling. All authors have read and approved this manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

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