All-Aluminum Thin Film Transistor Fabrication at Room Temperature

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Abstract: Bottom-gate all-aluminum thin film transistors with multi conductor/insulator nanometer heterojunction were investigated in this article. Alumina (Al_2O_3) insulating layer was deposited on the surface of aluminum doping zinc oxide (AZO) conductive layer, as one AZO/Al_2O_3 heterojunction unit. The measurements of transmittance electronic microscopy (TEM) and X-ray reflectivity (XRR) revealed the smooth interfaces between ~2.2-nm-thick Al_2O_3 layers and ~2.7-nm-thick AZO layers. The devices were entirely composited by aluminiferous materials, that is, their gate and source/drain electrodes were respectively fabricated by aluminum neodymium alloy (Al:Nd) and pure Al, with Al_2O_3/AZO multilayered channel and AlO_x:Nd gate dielectric layer. As a result, the all-aluminum TFT with two Al_2O_3/AZO heterojunction units exhibited a mobility of 2.47 cm^2/V·s and an I_{on}/I_{off} ratio of 10^6. All processes were carried out at room temperature, which created new possibilities for green displays industry by allowing for the devices fabricated on plastic-like substrates or papers, mainly using no toxic/rare materials.

Keywords: thin film transistor; conductor/insulator heterojunction; all-aluminum; room temperature

1. Introduction

Metal oxide semiconductors (MOSs) are supposed to be promising materials for thin film transistor (TFT) in displays, which have many favorable properties including high mobility, good uniformity, and electrical stability [1,2]. Furthermore, it is expected that MOS-based devices at room temperature process are compatible with flexible plastic or paper substrate devices [3,4]. Theoretically, MOS-based devices can overcome many obstacles and limitations of the conventional silicon devices, such as a complex process and high cost.

Recently, the attention of researchers has been focused on the novel design devices of nanoscale-stacked materials, which are formed by sequentially depositing different materials in the nanometer scale [5–8]. However, most of the nanoscale stacked oxide thin film transistors reported a required annealing process to improve the electrical properties. The key issue is the ability to surmount potential barrier from the heterojunction interface scattering carriers. Recently, researches

on the semiconductor/insulator multilayers like ZnO/HfO_2 [9] and ZnO/Al_2O_3 [10] used to confine electrons in the potential wells were reported. However, the thermal treatments were still required due to the nature of semiconductors [11] and multilayered structures. Obviously, the thermal treating process is harmful for extending flexible substrates [12], especially for the papers. To solve these problems, we selected aluminum doping zinc oxide (AZO) conductive thin film as one of channel materials, which provided sufficient carriers and helped improving the mobility of the devices without thermal treatment, with the characteristics of high carrier concentration [13], non-toxic [14] and inexpensive [15]. On the contrary, indium gallium zinc oxide (IGZO) [16], indium zinc oxide (IZO) [17], and indium tin zirconium oxide (ITZO) [18], as channel materials for thin film transistors, contain indium element, which is known being toxic and rare in the earth. Moreover, it was reported that the pulsed laser deposition (PLD) produced a flux of energetic ions, which leads to local heating right at the film growth region, playing a similar effect of heat treatment, without imposing a large heat load to the substrate [19].

In this work, we designed three different types of multilayered thin film transistors with AZO conductive layers and Al_2O_3 insulating layers to investigate the stacked structure effect of channel layers. We found that the saturation mobility of multilayered TFT rose rapidly when the number of stacked layers increased to four. However, the stacked structure also made the density of defect states increase.

2. Experiments

Figure 1 shows the TFT devices with different channel structures: (i) AZO-TFT, referred as "S1"; (ii) AZO/Al_2O_3-TFT, referred as "S2"; and (iii) $AZO/Al_2O_3/AZO/Al_2O_3$-TFT, referred as "S3". A 300-nm-thick Al:Nd alloy (3 wt % of Nd) as gate electrode was deposited on glass substrate by DC magnetron sputtering and patterned by conventional photolithography at room temperature. Subsequently, the gate metal was immersed into the anodizing electrolyte, applied with a voltage of 90 V, forming a 200-nm-thick layer of AlO_x:Nd on the gate surface. AZO and Al_2O_3 channel layers were prepared by pulsed laser deposition at room temperature with a basic pressure of 2.0×10^{-4} Pa, an O_2 flow rate of 10 sccm, a pulsing energy of 100 mJ, a repeating rate of 5 Hz, a pulse duration of 10 ns, and a KrF laser wavelength of 248 nm, patterned through the shadow mask. AZO films were all composed of 2 wt % Al_2O_3 and 98 wt % ZnO. Al source/drain electrodes with thicknesses of 200 nm were evaporated by Edward evaporation at room temperature. No annealing treatment was adopted during the whole process, and the devices were entirely composed of aluminiferous materials.
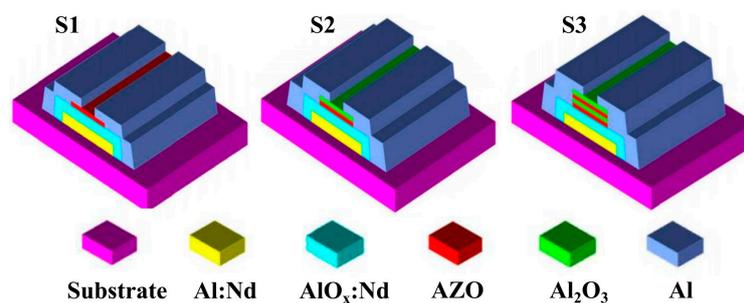

Figure 1. Schematic cross-sectional images of Devices S1, S2, and S3 with different types of channel layer structures.

The electrical characteristics of TFTs were measured by a semiconductor parameter analyzer (Agilent 4155 C, Santa Clara, CA, USA) under ambient condition.

3. Results and Discussion

As shown in Figure 2a, in the AZO/Al_2O_3 heterojunction structure, because of the high conduction band offset between AZO and Al_2O_3, electrons can be accumulated in a potential well of AZO [7]. Thus, along the in-plane direction, the high electron movement was expected to be induced by the AZO/Al_2O_3 multilayers, due to the two dimension electron transfer formed in the interfaces between AZO and Al_2O_3. Moreover, the channel current in the multilayered structure was formed through both in-plane and out-of-plane directions. The out-of-plane current strongly depends on the thickness of the barrier layers since the carriers can migrate along the vertical direction in the multi-structures through direct tunneling, which requires that the Al_2O_3 barrier layers should be ultrathin. The tested curves and simulated curves of the X-ray reflectivity (XRR, EMPYREAN, PANalytical, Almelo, The Netherlands) measurement are shown in Figure 2b. The result shows that the thickness of AZO films is between 2.6 and 3.8 nm, with a roughness of 0.57–0.92 nm; and the thickness of Al_2O_3 films ranges from 2.1 to 2.6 nm, with a roughness from 0.41 to 0.83 nm. The experiment indicated has acquired smooth and ultrathin nano-multilayers.
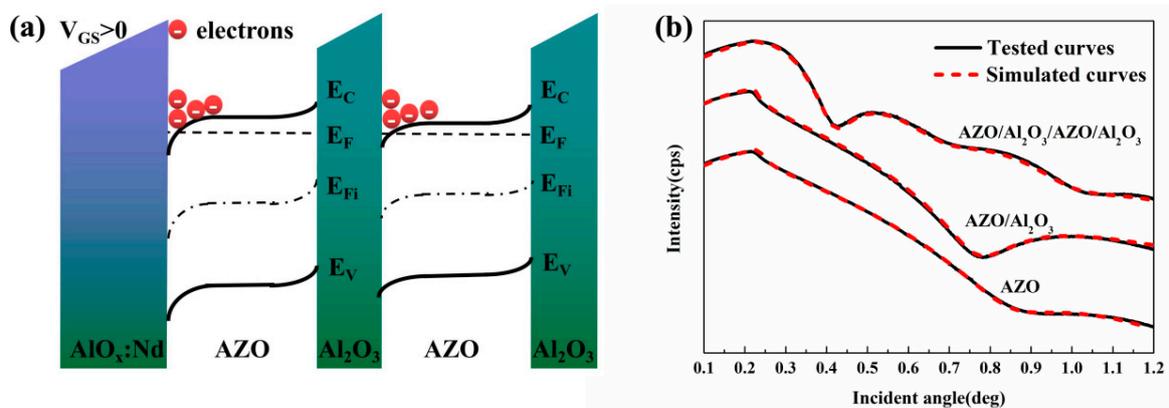

Figure 2. (**a**) Energy band structure and electrical effect of AZO/Al_2O_3/AZO/Al_2O_3 stacked channel layers; (**b**) X-ray reflectivity (XRR) measurements obtained from AZO single layer, AZO/Al_2O_3 bilayer, and AZO/Al_2O_3/AZO/Al_2O_3 multilayers.

Figure 3a shows the cross-sectional high-resolution transmission electron microscopy *(*HRTEM, JEM-2100F, JEOL, Akishima, Tokyo, Japan) image of AZO/Al_2O_3/AZO/Al_2O_3 channel layers in Device S3, and smooth interfaces between ~2.7-nm-thick AZO and ~2.2-nm-thick Al_2O_3 layers can be observed, consistent with the XRR results. It indicates that the ultrathin multilayers were well-deposited by the PLD method. In addition, the electron diffraction patterns of AZO/Al_2O_3 multilayers manifested the structure of crystalline/amorphous. Both AZO layers grown on the anodized AlO_x:Nd gate insulator and PLD prepared Al_2O_3 layer showed the similar diffraction plane of (002) (common in as-deposited PLD grown AZO or ZnO as reported [20,21]), suggesting that the AZO/Al_2O_3 heterojunction unit can be well repeated by PLD method without the effect of different underlayers. Moreover, there were no obvious structural differences between the anodized AlO_x:Nd gate insulator and PLD grown Al_2O_3 layers.

The results of Al, Zn, O distribution detected by energy-dispersive X-ray spectroscope (EDS, Bruker, Adlershof, Berlin, Germany) mapping scan are shown in Figure 3b. Through EDS mapping scan, an obvious diffusion of Zn element from AZO layers into Al_2O_3 layers was found, while which was rare in the anodized AlO_x:Nd gate insulator. It was verified by the results of time of flight secondary ion mass spectrometry (TOF-SIMS, PHI TRIFT-II, Physical Electronics, Minneapolis and Saint Paul, MN, USA), which is shown in Figure 3c. This phenomenon was possibly caused by the strong adsorption of Zn atoms in the Al_2O_3 layers, because of the high content of oxygen vacancies, enlarging the pore mouth of the ultrathin Al_2O_3 film and increasing the adsorption ability. As shown

by the X-ray photoelectron spectra (XPS, ESCALAB 250Xi, Thermo Fisher Scientific, Waltham, MA, USA) for O1s region in Figure 3d,e, the content of oxygen vacancies of PLD grown Al_2O_3 layer is much higher than the anodized AlO_x:Nd gate insulator, which can explain their different degrees of Zn diffusion. Meanwhile, in Figure 3c, we can also observe a strong and sharp peak of Al^{3+} in Region III, which implies an inward gathering of Al^{3+} ions in the Al_2O_3 layers. It may be due to the positive charge repulsion by Zn^{2+} ions as they diffused from both sides of Region II and Region IV.
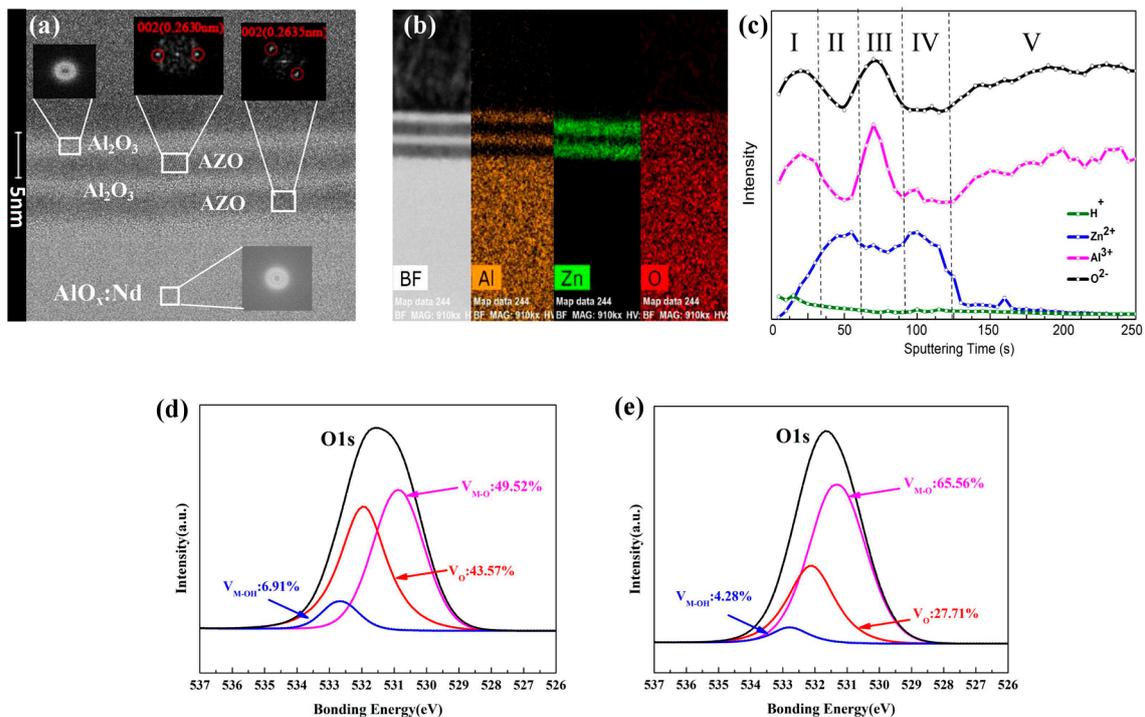

Figure 3. (**a**) Cross-sectional high-resolution transmission electron microscopy (HRTEM) image of $AZO/Al_2O_3/AZO/Al_2O_3$ channel layers in Device S3 and (**b**) the results of Al, Zn, O distribution detected by energy-dispersive X-ray spectroscope (EDS) mapping scan; (**c**) Time of flight secondary ion mass spectrometry (TOF-SIMS) results of H^+, Zn^{2+}, Al^{3+}, and O^{2-} ions for Device S3: Region I and III corresponds with Al_2O_3 layers, Region II and IV corresponds with AZO layers, and Region V corresponds with the anodized AlO_x:Nd gate insulator. X-ray photoelectron spectra (XPS) for the O1s region of (**d**) the PLD grown Al_2O_3 layer and (**e**) the anodized AlO_x:Nd gate insulator.

Figure 4a–f shows the output and transfer characteristics of the three devices with different structures of channel layers and the relevant data is listed in Table 1. The channel width/length (W/L) of all the devices was 1000/300 μm and the capacitance used to calculate mobility was 38 nF/cm^2. Compared with Device S1, Device S2 with an ultrathin Al_2O_3 barrier layer exhibited higher saturation mobility (μ_{sat}) and on-state current (I_{on}), which indicates that the AZO/Al_2O_3 stacked structure can improve the electrical performance of devices. It showed a similar tendency compared with other passivated TFTs from the literature [22–24]. However, in those researches, the passivation layers were thick (100–300 nm) and required heat treatment for preparation, which were unfavorable for ultrathin and flexible displays. Moreover, it is worth noticing that the saturation mobility of Device S3 is one order higher than Device S2, which was significantly promoted by the increase of channel paths [25].
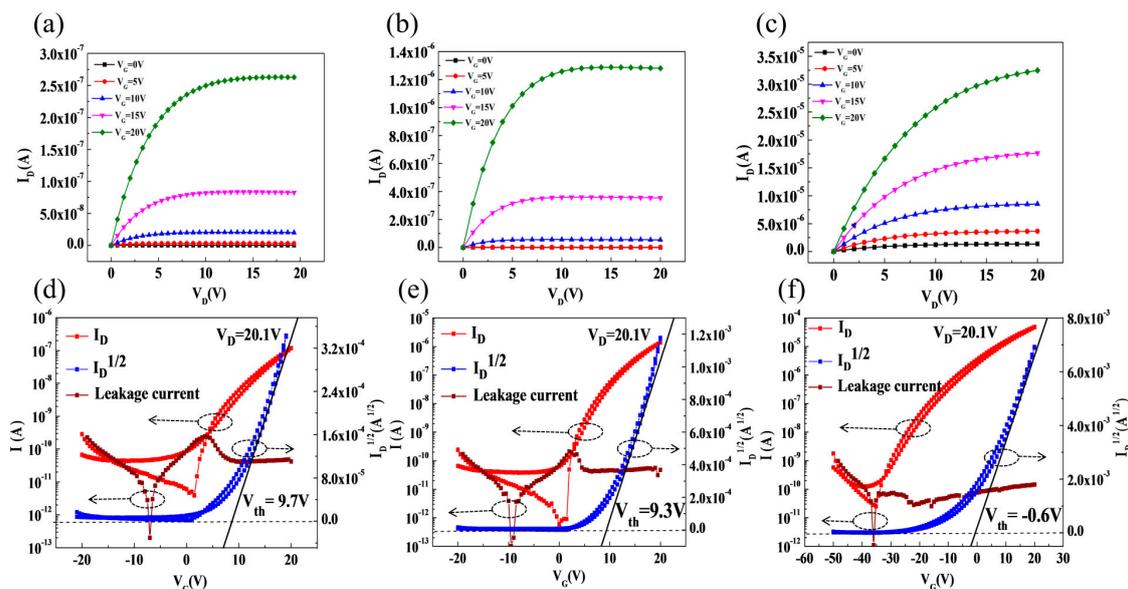
Figure 4. Output characteristics (**a**–**c**) and transfer characteristics (**d**–**f**) of devices: (**a**,**d**) for S1; (**b**,**e**) for S2 and (**c**,**f**) for S3.

Table 1. Device parameters extracted from the transfer curves in Figure 2, including on-to-off current ratio (I_{on}/I_{off}), sub-threshold swing (SS), saturation mobility (μ_{sat}), and threshold voltage (V_{th}).

Device	I_{on}/I_{off}	SS (V/Decade)	μ_{sat} (cm^2/V·s)	V_{th} (V)
S1	3.02×10^4	0.86	0.04	9.7
S2	7.47×10^4	1.53	0.50	9.3
S3	1.92×10^6	2.34	2.47	−0.6

The sub-threshold swing (SS) value is related to the total defect density from the bulk channel layer and the interface between the channel and dielectric layers [26]. The SS value is defined at the minimum value of $(d\log(I_{DS})/dV_{GS})^{-1}$. With the increasing number of stacked layers, the SS value elevated, according to Table 1. It indicates that stacked structure caused the increase of defects in the interfaces or bulk of channel layers [27], which was possibly attributed to the diffusion of Zn in the ultrathin Al_2O_3 barrier layers, as shown by the results of HRTEM and TOF-SIMS in Figure 3b,c. As the number of interfaces increased, the effect of Zn diffusion became more significant, which should be well concerned. Additionally, the serious negative V_{on} in S3 was possibly due to the great number of conduction electrons trapped in the interfaces between the layers, which were increased by the ion bombardment on the surfaces of underlayers during the PLD process as well. This phenomenon should be worked out in our further research.

Generally, the positive V_{th} shift of oxide TFTs is considered related to the charge trapping mechanism and extra negative charge capture by the adsorption of oxygen molecules in the back channel [28]. As shown in Figure 4, both devices S1 and S2 suffered a large positive shift in V_{th} with ΔV_{th} of 9.7 and 9.3 V, respectively. However, the ΔV_{th} of Device S3 reduced significantly to −0.6 V. It could be due to the higher carrier concentration with the increasing number of channel paths, and the increase of defect sites like oxygen vacancies in the interface between the upper AZO layer and under Al_2O_3 layer, as well. In addition, the reduction of ΔV_{th} in the devices with an increasing number of stacked layers also indicates that the barrier layers are able to help restrain the back channel effect to some degree [29].

4. Conclusions

In summary, three different types of all-aluminum thin film transistors were fabricated at room temperature. The smooth interfaces between ~2.7-nm-thick AZO layers and ~2.2-nm-thick Al_2O_3 layers were observed through the HRTEM images, consistent with the XRR results. The device with $AZO/Al_2O_3/AZO/Al_2O_3$ multilayered channels showed a saturation mobility of 2.47 $cm^2/V \cdot s$ and an on-to-off current ratio of 1.92×10^6. Ultrathin alumina (Al_2O_3) insulating layer deposited on the surface of aluminum doping zinc oxide (AZO) conductive layers can effectively confine the electron in potential well of AZO. The parallel channel paths can significantly increase the channel current and improve mobility.

It is worth mentioning that all processes were carried out at room temperature, which allows for the devices fabricated on plastic-like substrates or papers. Therefore, it is expected that the all-aluminum TFT with multilayered structure will create a new opportunity for an eco-friendly industry of flexible and wearable displays.

Author Contributions: Rihui Yao, Honglong Ning, Zeke Zheng and Yong Zeng designed the research; Zeke Zheng and Yong Zeng carried out the experiments; Rihui Yao, Honglong Ning and Zeke Zheng analyzed the data; Xianzhe Liu, Shiben Hu, Ruiqiang Tao, Jianqiu Chen, Wei Cai, Miao Xu, Lei Wang, Linfeng Lan and Junbiao Peng provided valuable discussions and suggestions; Rihui Yao, Honglong Ning and Zeke Zheng wrote the paper.

Conflicts of Interest: The authors declare no conflict of interest.

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