


Article

# Study of Resistive-Type Superconducting Fault Current Limiters for a Hybrid High Voltage Direct Current System

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**Abstract:** In this paper, a hybrid high voltage direct current transmission system containing a line commutated converter and a voltage source converter is developed. To enhance the robustness of the hybrid transmission system against direct current short-circuit faults, resistive-type superconducting fault current limiters are applied, and the effectiveness of this approach is assessed. Related mathematical models are built, and the theoretical functions of the proposed approach are expounded. According to the transient simulations in MATLAB software, the results demonstrate that: (i) The superconducting fault current limiter at the voltage source converter station enables to very efficiently mitigate the fault transients, and owns an enhanced current-limiting ability for handling the short-line faults. (ii) The superconducting fault current limiter at the line commutated converter station is able to mildly limit the fault current and alleviate the voltage drop, and its working performance has a low sensitivity to the fault location. At the end of the study, a brief scheme design of the resistive-type superconducting fault current limiters is achieved. In conclusion, the application feasibility of the proposed approach is well confirmed.

**Keywords:** hybrid high voltage direct current transmission system; resistive-type superconducting fault current limiter; scheme design; short-circuit fault; Yttrium barium copper oxide materials; transient simulation

## 1. Introduction

In recent years, hybrid high voltage direct voltage (HVDC) technology has received continuously increasing attention, and it is known as an advanced option for long distance as well as large-scale power transmission [1,2]. In principle, a hybrid HVDC transmission system contains a line commutated converter (LCC) and a voltage source converter (VSC). The LCC serves as a rectifier station to save the capital cost, and the VSC acts as an inverter station to strengthen the operational flexibility. Due to integrating the merits of the LCC and VSC, the hybrid HVDC owns the following technical characteristics: (i) inexistence of commutation failure, (ii) enhanced competence to support weak/passive networks, (iii) flexible control of active and reactive power.

For promoting the development of hybrid HVDC technology, scholars have conducted some fundamental researches, which focus on the measure of alternating current (AC) system strength and the small-signal dynamics [3,4]. However, there are little studies on enhancing the robustness of a hybrid HVDC transmission system against DC short-circuit faults. In a sense, the hybrid HVDC may have a complex fault issue, since the DC fault currents of the LCC and VSC stations have essential differences with each other. For the DC fault current of the LCC station, it could be properly adjusted by the firing angle controller, and applying an additional current-limiting solution is able to bring a better fault suppression effect. Concerning the DC fault current of the VSC station, it rises very fast and cannot be removed even though the power electronic switches are blocked, while the anti-parallel diodes act as a freewheeling bridge circuit to feed the fault current [5]. Thus, it becomes an urgent and inevitable requirement to introduce an efficient current-limiting approach in the VSC station.

In this study, our research group suggests using superconducting fault current limiters (SFCLs) to solve the DC fault issue in the hybrid HVDC, and it is because SFCL is a very competitive current-limiting device with excellent performance superiorities, such as automatic trigger and rapid response [6–10]. Based on a comprehensive literature review, Table 1 lists a summary of the studies of SFCLs in different HVDC networks. Technically speaking, the current studies are mainly concerned about a pure LCC-HVDC or VSC-HVDC network.

In [11], a flux-coupling-type SFCL is applied to address the commutation failure in a pure LCC-HVDC grid. In light of different fault types and fault resistances, this SFCL's impacts on reducing the duration of the commutation failure and accelerating the fault recovery are confirmed. In [12,13], the performance behaviors of the resistive type SFCL on mitigating the commutation failure of a LCC-HVDC grid are studied. Different installation sites of the SFCL for the HVDC network are assessed, and a suitable optimal method of the SFCL resistance is investigated.

In [14–17], the SFCLs such as resistive-type, saturated iron-core-type, and hybrid-type are selected to inhibit the DC fault current of a pure VSC-HVDC network. A few helpful contributions regarding the parameter optimization and techno-economic evolution of the SFCLs for the VSC-HVDC network protection are obtained. In addition, some scholars preliminarily explore the influences of the resistive and inductive SFCLs on improving the operation reliability [18], and strengthening the fault ride-through (FRT) of wind plants connected to the VSC-HVDC network [19].

**Table 1.** Summary of the studies of superconducting fault current limiters (SFCLs) in different high voltage direct voltage (HVDC) networks. LCC: line commutated converter; VSC: voltage source converter.

Type of SFCL	Type of HVDC	Voltage Class	Research Object	Evaluation Method	Country, Report Year
Flux-coupling-type	LCC HVDC	230 kV	Commutation failure and fault recovery	MATLAB Simulation	China, 2015 [11]
Resistive type	LCC HVDC	180 kV [12] 500 kV [13]	Commutation failure and position analysis	PSCAD Simulation	Korea, 2016 [12] China, 2017 [13]
Hybrid-type	VSC HVDC	160 kV	Principle verification and scheme design	MATLAB Simulation	China, 2017 [14]
Resistive type	VSC HVDC	320 kV [15,19] 100 kV [16] 200 kV [18]	Techno-economic evolution and resistance varying behaviors	PSCAD [15,19] MATLAB [16,18]	France, 2017 [15] Korea, 2018 [16] China, 2017 [18] UAE, 2017 [19]
Inductive type	VSC HVDC	100 kV	Current limitation and recovery	MATLAB Simulation	Korea, 2018 [16]
Saturated iron-core-type	VSC HVDC	100 kV	Modeling, voltage analysis and energy dissipation	MATLAB Simulation	Korea, 2018 [16] China, 2018 [17]

To the best of our knowledge, there are no related reports about the systematic application of resistive SFCLs in a hybrid 500 kV HVDC network. When two resistive SFCLs are respectively

installed at the LCC and VSC stations to withstand the DC fault, it is crucial to investigate how the two SFCLs can protect a hybrid HVDC network subject to the change of current-limiting parameters, fault resistances, and fault locations. In addition, it is critical to clarify the performance differences between the two SFCLs and lay a foundation for the scheme design of superconducting devices.

Aiming at the aforementioned tasks, this paper is devoted to studying and assessing the application feasibility of resistive SFCLs in a 500 kV hybrid HVDC network. The paper is arranged as follows. Section 2 states the analytical model of the hybrid HVDC including the SFCLs, and discusses the theoretical functions of the SFCLs to the DC fault behaviors. Section 3 conducts the simulation analyses and performance comparison, where different current-limiting parameters, fault severity levels and fault locations are taken into consideration. In Section 4, a brief scheme design of the SFCLs basing YBCO material is given. Section 5 recaps the main conclusions and suggests improvements in the future.

## 2. Theoretical Analysis

### 2.1. Analytical Model of the Hybrid HVDC Including the SFCLs

Figure 1 indicates the schematic connection of the hybrid HVDC system including two resistive SFCLs. The system is a 500 kV bipolar hybrid LCC-VSC HVDC link (only positive pole is denoted here), and the two SFCLs are installed at the LCC station (rectifier side) and the VSC station (inverter side), respectively. For the analytical model of the hybrid HVDC system, this study mainly considers the following factors: (i) The two AC grids are represented by equivalent AC voltage sources with series impedances [20]. (ii) The DC transmission line is represented by an equivalent “resistance-inductance (R-L)” model. (iii) The LCC station adopts a constant DC current control to generate the firing angle, and the VSC station uses a direct current control mode [21]. Detailed modeling information as well as mathematical equations can be found in Appendices A.1–A.3.

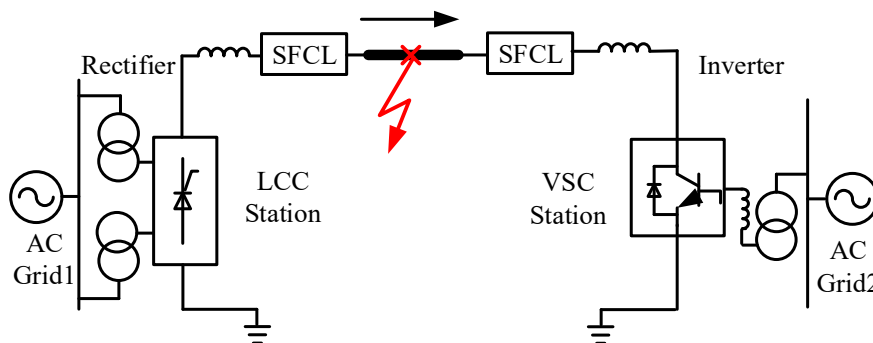


Figure 1. Allocation of the resistive SFCLs in a hybrid HVDC system with the LCC and VSC station.

Based on the second generation Yttrium barium copper oxide (YBCO) material, Figure 2 describes the equivalent modeling of a resistive SFCL at different time-scales [16,22,23], and the change rule of the SFCL resistance is written as:

$$R(t) = \begin{cases} 0 & (t < t_0) \\ R_{SC}[1 - \exp(-\frac{t-t_0}{\tau})]^{\frac{1}{2}} & (t_0 \leq t < t_1) \\ a_1(t - t_1) + b_1 & (t_1 \leq t < t_2) \\ a_2(t - t_2) + b_2 & (t_2 \leq t < t_3) \end{cases} \quad (1)$$

where  $t$  is the time constant;  $R_{SC}$  is denoted as the normal-state resistance of the SFCL. From Equation (1), the SFCL’s equivalent model is explained as: (i)  $t_0$  is the quench-starting time;  $t_1$  is the first-stage recovery-starting time;  $t_2$  is the secondary-stage recovery-starting time;  $t_3$  is the completed recovery time. (ii)  $a_1, a_2, b_1,$  and  $b_2$  are expressed as the model coefficients, respectively.

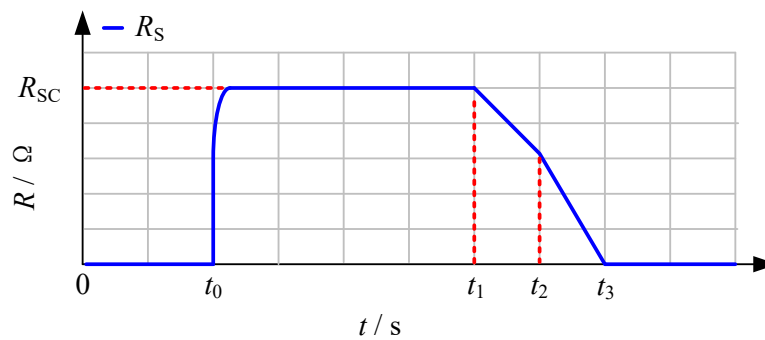


Figure 2. The simplified mathematical model of the resistive SFCL.

From the literature, the modeling of the two-stage recovery time is mainly based on the experimental studies for superconducting elements, and the temperature effect could be the potential reason. When the SFCL starts to recover to the superconducting state, the accumulated joule heat under the current-limiting operation leads to the temperature rising and make the SFCL resistance have a constrained variation trend, and it is defined as the first-stage recovery process. After the heat is dissipated, the lowering of temperature will make the SFCL resistance have a faster drop to zero, and it is defined as the two-stage recovery process. As for a precise resistive SFCL model on account of the “power-law” equation, this equivalent SFCL model has multiple operational segments, and it is still valid to reflect the transient properties of the resistive SFCL.

### 2.2. Impacts of the SFCLs on the DC Fault Currents

In this section, the impacts of the SFCLs on the DC fault currents of the LCC and VSC stations are discussed. As shown in Figure 3, it indicates the equivalent circuit of the DC-link.  $U_{dcr}$ ,  $I_{dcr}$  and  $U_{dci}$ ,  $I_{dci}$  are represented as the DC voltage and current of the LCC and VSC stations, respectively;  $X_{smr}$  and  $X_{smi}$  are marked as the smoothing reactors installed at the LCC and VSC stations, respectively;  $C_{VSC}$  is the DC capacitor of the VSC station.

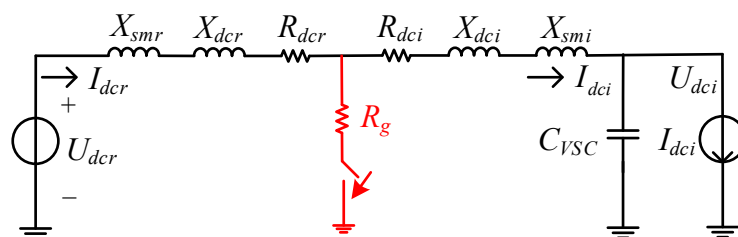


Figure 3. The equivalent circuit of the DC-link.

It is assumed that the fault resistance is  $R_g$  and the residual voltage at the fault location is  $U_g$ . Herein,  $R_{dcr}$ ,  $X_{dcr}$ , and  $R_{dci}$ ,  $X_{dci}$  are represented as the resistance and reactance of the DC line of the LCC and VSC stations, respectively. As the SFCL resistance  $R_{SFCLr}$  is connected in series with the LCC station, the dynamics of the DC fault current  $I_{dcr-f}$  can be expressed as:

$$(L_{smr} + L_{dcr})\dot{I}_{dcr-f} = U_{dcr} - U_g - I_{dcr-f}(R_{SFCLr} + R_{dcr}) \tag{2}$$

If the DC voltage  $U_{dcr}$  is represented by the function of firing angle, AC voltage and transformer leakage reactance, Equation (2) will be rewritten as:

$$\begin{cases} (L_{smr} + L_{dcr})\dot{I}_{dcr-f} = U_{dcr} - U_g - I_{dcr-f}(R_{SFCLr} + R_{dcr}) \\ U_{dcr} = 2\left(\frac{3\sqrt{2}V_{LCCm}}{\pi T} \cos\alpha - I_{dcr-f} \frac{3X_{T1}}{\pi}\right) \end{cases} \quad (3)$$

$$\Rightarrow (L_{smr} + L_{dcr})\dot{I}_{dcr-f} = \frac{6\sqrt{2}U_{LCCm}}{\pi T} \cos\alpha - U_g - I_{dcr-f}(R_{SFCLr} + R_{dcr} + \frac{6X_{T1}}{\pi})$$

where  $U_{LCCm}$  is the root-mean-square (RMS) AC voltage over the LCC station;  $T$  is the transformer turn-ratio. As compared to the case of without SFCL, introducing  $R_{SFCLr}$  is able to increase the resistance of the DC circuit, and it is helpful to reduce the peak value of the fault current. Considering the function of the firing angle controller, the working status of the LCC station will be changed from the rectifying mode to the inverting mode. Thus, the DC fault current will be enforcedly down to zero.

Note that, the residual voltage  $U_g$  in Equation (2) can be calculated by:

$$U_g = R_g(I_{dcr-f} + I_{dci-f}) \quad (4)$$

where  $I_{dci-f}$  is the DC fault current of the VSC station. It can be inferred that, when the ground resistance  $R_g$  is not equal to zero and has a relatively large resistance value, the DC fault current of the LCC station might be potentially affected by that of the VSC station.

By referring to [24–26], the fault process of a VSC-HVDC station has three stages, which are DC-link capacitor discharging (stage 1), diodes freewheeling (stage 2) and grid-side current feeding (stage 3), respectively. Before the DC voltage drops to zero, all the free-wheel diodes are blocked due to the reverse voltage, and thus the DC link will be insulated from the AC grid 2. In a sense, stage 1 (capacitor discharging) is the key stage for the SFCL to suppress the DC fault current and mitigate the DC voltage decline.

Herein, stage 1 conducts the system response before the dc voltage drops to zero, and Figure 4 shows the fault analysis diagram. The circuit equation is modeled as:

$$\begin{cases} (L_{smr} + L_{dcr})\dot{I}_{dci-f} = U_{dci} - U_g - I_{dci-f}(R_{SFCLi} + R_{dci}) \\ I_{dci-f} = -I_{Cap} = -C_{VSC}\dot{U}_{dci} \end{cases} \quad (5)$$

$$\Rightarrow -(L_{smr} + L_{dcr})C_{VSC}\ddot{U}_{dci} = U_{dci} - U_g + C_{VSC}\dot{U}_{dci}(R_{SFCLi} + R_{dci})$$

$$\Rightarrow (L_{smr} + L_{dcr})C_{VSC}\ddot{U}_{dci} + C_{VSC}\dot{U}_{dci}(R_{SFCLi} + R_{dci}) + U_{dci} - U_g = 0$$

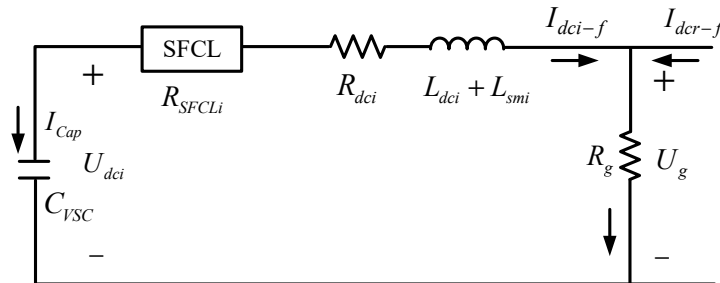


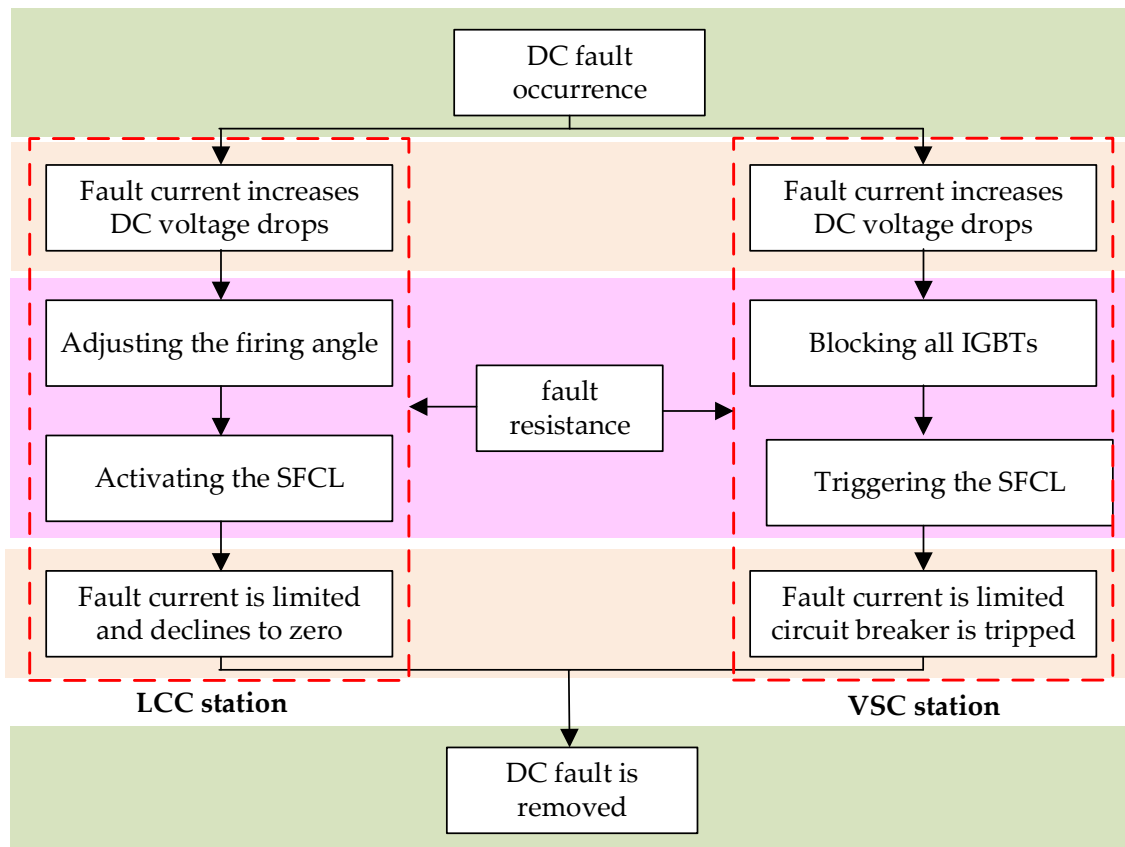
Figure 4. Fault analysis of the VSC-station with the SFCL (capacitor discharging stage).

By substituting Equation (4) into Equation (5), the equation will be rewritten as:

$$(L_{smr} + L_{dcr})C_{VSC}\ddot{U}_{dci} + C_{VSC}\dot{U}_{dci}(R_{SFCLi} + R_{dci} + R_g) + U_{dci} - R_g I_{dcr-f} = 0 \quad (6)$$

Regarding the solution method of Equation (6), details are analyzed in Appendix ???. In theory, introducing  $R_{SFCLi}$  will closely affect the VSC-HVDC link's electrical properties, and it means that the current-limiting resistance  $R_{SFCLi}$  can not only reduce the fault current level in the DC line, but also change the oscillation characteristic of the DC capacitor voltage. When increasing  $R_{SFCLi}$  leads to an over-damped state, the capacitor voltage  $U_{dci}$  will not decline to zero, and the subsequent two stages may not happen [27,28]. Owing to that all-diodes-conducting phenomenon is avoided, the SFCL's contributions in reducing the currents in the AC side and the converter may become more obvious.

According to the above theoretical analysis, the flowchart of the integrated process of the proposed approach can be shown in Figure 5.



**Figure 5.** Flowchart of the integrated process of the proposed approach. IGBT: Insulated Gate Bipolar Translator.

### 3. Simulation Study

To evaluate the effectiveness of the SFCLs in the hybrid HVDC system, a detailed simulation model is built in the MATLAB software (R2017b, MathWorks, Natick, MA, USA), and the electromagnetic transient (EMT) type simulations are done in a 64-b personal computer with Intel i7-7700 QuadCore 2.8-GHz processor and 8-GB RAM (DELL, Round Rock, TX, USA). The EMT simulations use the discrete solver, and the simulation time step is set as  $5 \times 10^{-5}$  s.

The main parameters are summarized in Table 2, and the modeling information is depicted as: (i) The AC grid model is simulated by an AC voltage source in series with the equivalent resistance and inductance. (ii) The resistive SFCL model is based on the controlled voltage source [29]. (iii) The VSC and LCC adopt detailed models (detailed representation of power electronic converters), and the models are able to precisely show the dynamic performance over relatively short periods of times.

During the simulations, different SFCL resistances are taken into consideration [30,31], so as to validate how the change of the SFCL resistance affects the fault characteristics of the hybrid HVDC

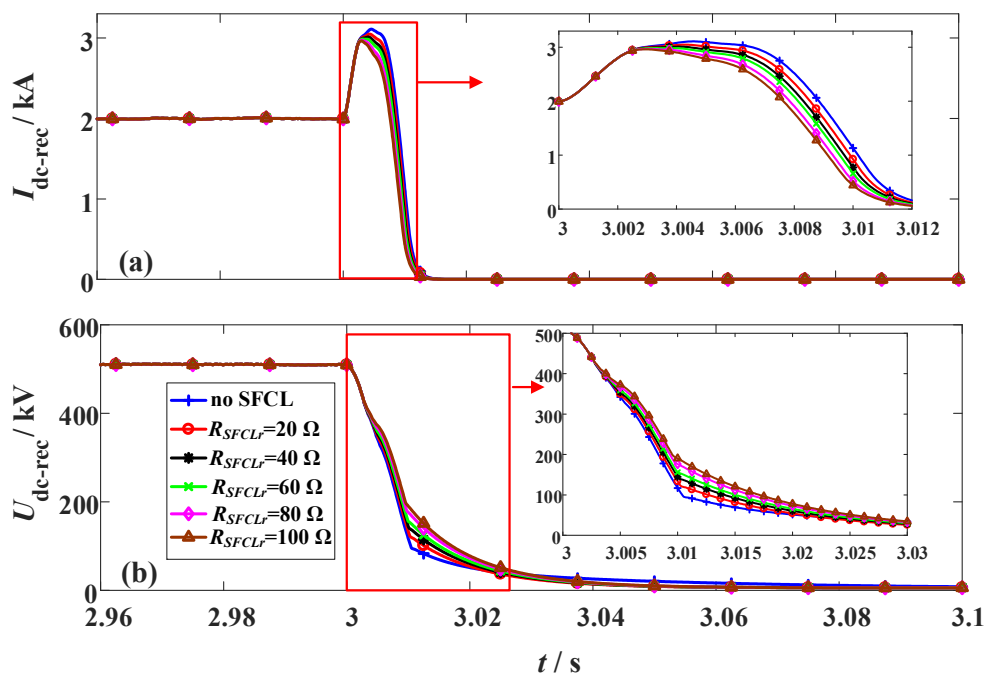
system. The estimated recovery time of the SFCL is about 4 s. For the resistance of  $R_{SFCL} = 30 \Omega$ , the coefficients of  $a_1, a_2, b_1, b_2$  are set as  $a_1 = 9.52, a_2 = 15.87, b_1 = 30, b_2 = 19$ , respectively.

**Table 2.** Main parameters of the simulation model.

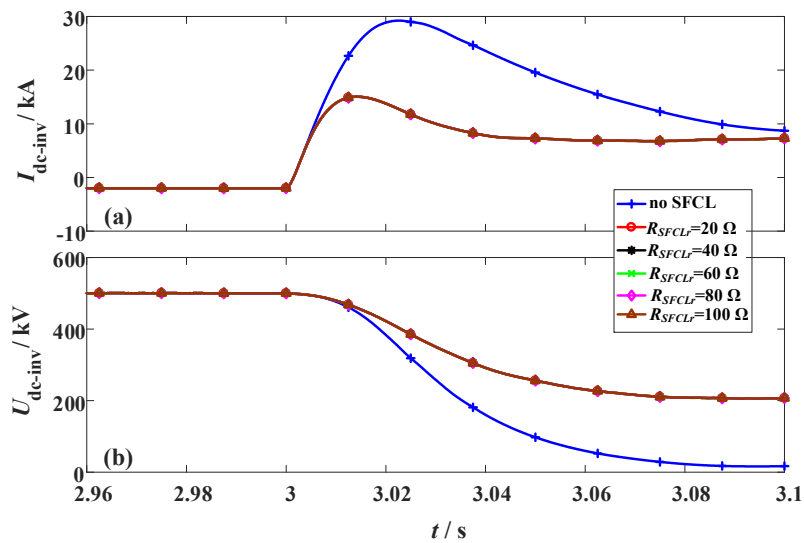
Superconducting Fault Current Limiters	
Superconducting coil $R_{sc}$ at the LCC/VSC	20 $\Omega$ –100 $\Omega$ /10 $\Omega$ –50 $\Omega$
<b>LCC Station</b>	
Rated voltage/frequency	380 kV/50 Hz
Short-circuit ratio	3.076
DC current controller	$K_{pldc} = 1, K_{ildc} = 90$
<b>DC Link</b>	
Rated voltage/current	500kV/2 kA
Length of DC transmission line	500 km
Smoothing reactor of LCC/VSC	0.3 H/0.01 H
<b>VSC Station</b>	
Rated voltage/frequency	220 kV/50 Hz
Short-circuit ratio	3.34
AC current controller ( $K_{pVac}, K_{iVac}$ )	$K_{pVac} = 0.6, K_{iVac} = 10$
DC voltage controller ( $K_{pVdc}, K_{iVdc}$ )	$K_{pVdc} = 8, K_{iVdc} = 20$

### 3.1. Changing the SFCL Resistance in the LCC Station

The simulation conditions of the DC short-circuit fault are defined as: (i) The fault occurs in the middle of the DC line at  $t_0 = 3$  s. (ii) The fault resistance and duration are 1  $\Omega$  and 100 ms. (iii) The SFCL at the LCC station ( $R_{SFCLr}$ ) changes from 20  $\Omega$  to 100  $\Omega$ , and the SFCL at the VSC station ( $R_{SFCLi}$ ) has the constant of 30  $\Omega$ . As shown in Figures 6 and 7, they indicate the transient behaviors of the hybrid HVDC system subject to the change of  $R_{SFCLr}$ .



**Figure 6.** Behaviors of the LCC station considering the change of the SFCL resistance  $R_{SFCLr}$ . (a) DC current and (b) DC voltage.

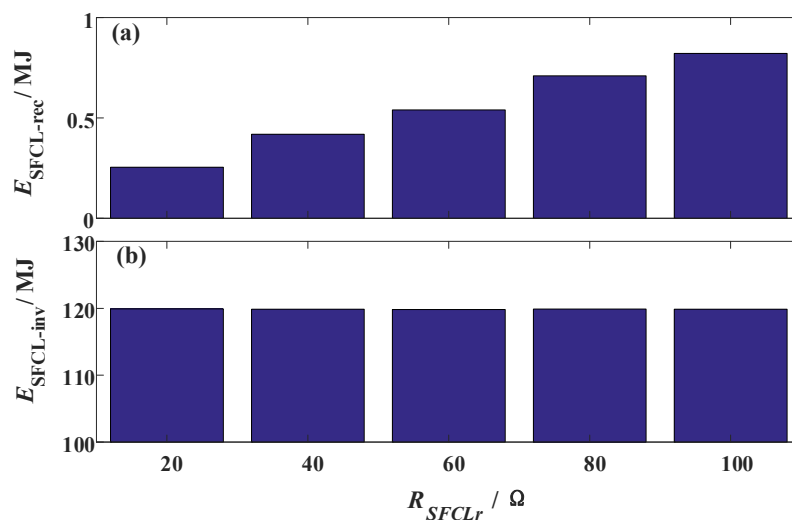


**Figure 7.** Behaviors of the VSC station considering the change of the SFCL resistance  $R_{SFCLr}$ . (a) DC current and (b) DC voltage.

In the LCC station, the peak value of the DC fault current is about 1.5 times of the rated level, and the reduction of the DC fault current is mainly conducted by adjusting the firing angle. Herein, the LCC station will switch to the inverting mode to make the DC fault current decline to zero. In the case of with the SFCL, it can mildly limit the fault current and alleviate the voltage drop. During the process of the fault feeding, the firing angle controller and the SFCL will serve as the primary and secondary factors to combinedly affect the fault transients.

It is observed that augmenting  $R_{SFCLr}$  has almost no effect on the VSC station, where the activation of  $R_{SFCLi}$  will undertake the crucial roles of current-limitation and voltage compensation. For the VSC station, installing the SFCL ( $R_{SFCLi} = 30 \Omega$ ) is able to limit the DC fault current from 29.2 kA to 15.1 kA, and improve the DC voltage from 16 kV to 197 kV.

Figure 8 shows the energy dissipation of the two SFCLs, where the calculation time is from the fault occurring to the fault being removed (the duration is 100 ms). When  $R_{SFCLr}$  is designed as 20  $\Omega$ , 40  $\Omega$ , 60  $\Omega$ , 80  $\Omega$ , and 100  $\Omega$ , respectively, its dissipated energy at the LCC station will be 0.27 MJ, 0.44 MJ, 0.56 MJ, 0.73 MJ, and 0.85 MJ, respectively. A rising trend is obviously found, but the caused energy dissipation effect is still limitable. In the VSC station, its relevant SFCL has a steady and efficient energy dissipation with the level of 119.9 MJ.



**Figure 8.** Energy dissipation of the two SFCLs subject to the change of the SFCL resistance  $R_{SFCLr}$ .



### 3.2. Changing the SFCL Resistance in the VSC Station

In this subsection, the original fault parameters are unchanged, and it is designed that  $R_{SFCLr}$  owns a constant of  $20 \Omega$  and  $R_{SFCLi}$  varies from  $10 \Omega$  to  $50 \Omega$ .

Figures 9 and 10 show the characteristics of the hybrid HVDC system subject to the change of  $R_{SFCLi}$ . According to the results, changing  $R_{SFCLi}$  will obviously influence the transient fluctuations in the VSC station, but have a negligible effect on the DC current and voltage of the LCC station. In addition, it is found that a moderate increase of the SFCL resistance  $R_{SFCLi}$  can bring better contributions. Nevertheless, it is not recommended to excessively increasing the resistance  $R_{SFCLi}$ , since the current-limiting ratio of the SFCL seems to achieve the saturated level. When  $R_{SFCLi}$  increases from  $10 \Omega$  to  $20 \Omega$ , the current-limiting ratio has an expected improvement of 14.3%, but when  $R_{SFCLi}$  rises from  $40 \Omega$  to  $50 \Omega$ , the obtained improvement is just 4.8%. As shown in Table 3, it lists a detailed performance comparison.

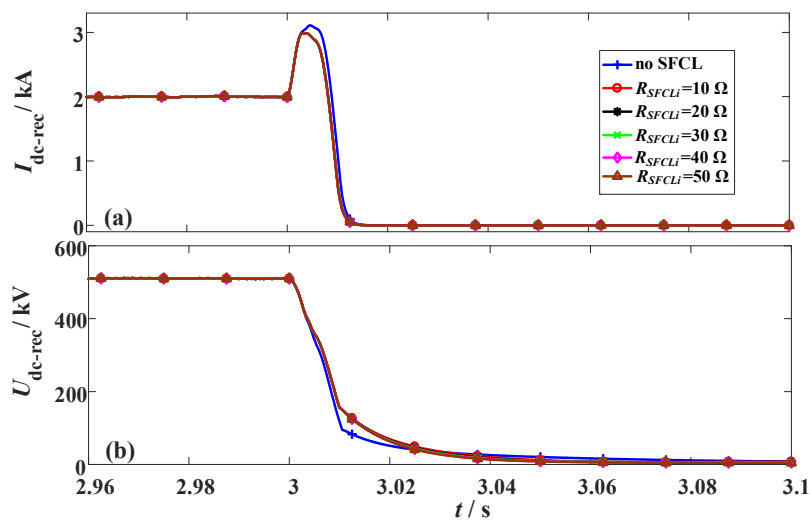


Figure 9. Behaviors of the LCC station considering the change of the SFCL resistance  $R_{SFCLi}$ . (a) DC current and (b) DC voltage.

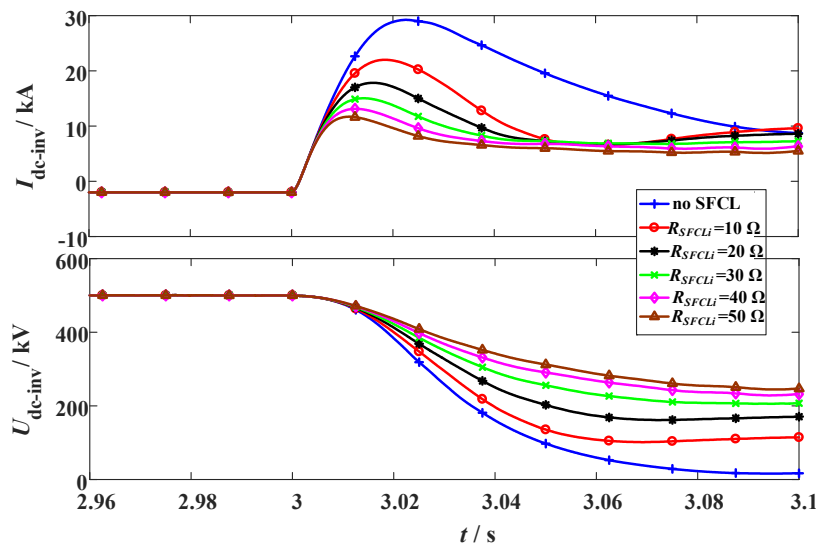
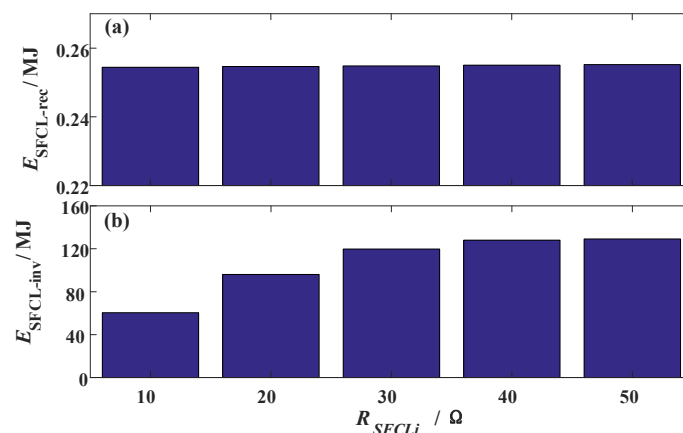


Figure 10. Behaviors of the VSC station considering the change of the SFCL resistance  $R_{SFCLi}$ . (a) DC current and (b) DC voltage.

**Table 3.** Performance of the SFCL at the VSC station under different parameters.

Items	Effects of the SFCL on the VSC Station	
	DC Fault Current/Current-Limiting Ratio	DC Voltage/Calculated Drop Rate
$R_{SFCLi} = 10 \Omega$	22.1 kA/24.7%	101.5 kV/79.7%
$R_{SFCLi} = 20 \Omega$	17.8 kA/39%	160.1 kV/67.9%
$R_{SFCLi} = 30 \Omega$	15.1 kA/48.5%	196.9 kV/60.6%
$R_{SFCLi} = 40 \Omega$	13.2 kA/55.1%	223.8 kV/55.2%
$R_{SFCLi} = 50 \Omega$	11.7 kA/59.9%	241.3 kV/51.7%

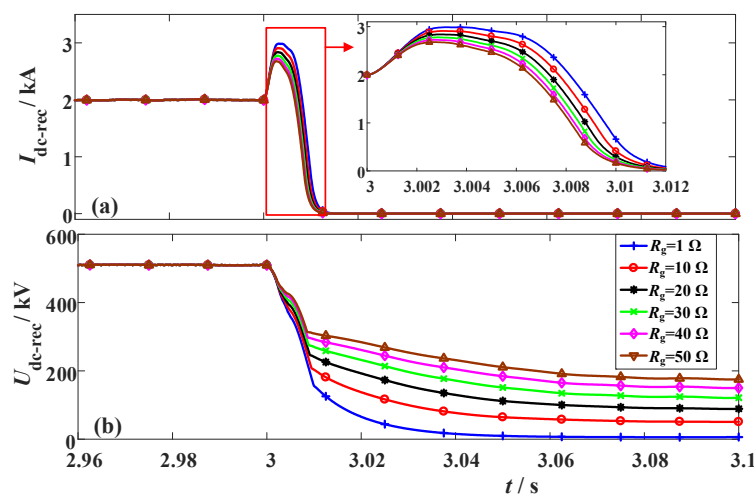
Figure 11 shows the energy dissipation of the two SFCLs. Concerning that  $R_{SFCLi}$  is set as 10  $\Omega$ , 20  $\Omega$ , 30  $\Omega$ , 40  $\Omega$ , and 50  $\Omega$ , respectively, the dissipated energy of the SFCL at the VSC station will be 60.5 MJ, 96.1 MJ, 119.9 MJ, 128.0 MJ, and 129.3 MJ, respectively. Regarding the LCC station, its relevant SFCL has a steady energy dissipation with the level of 0.27 MJ.



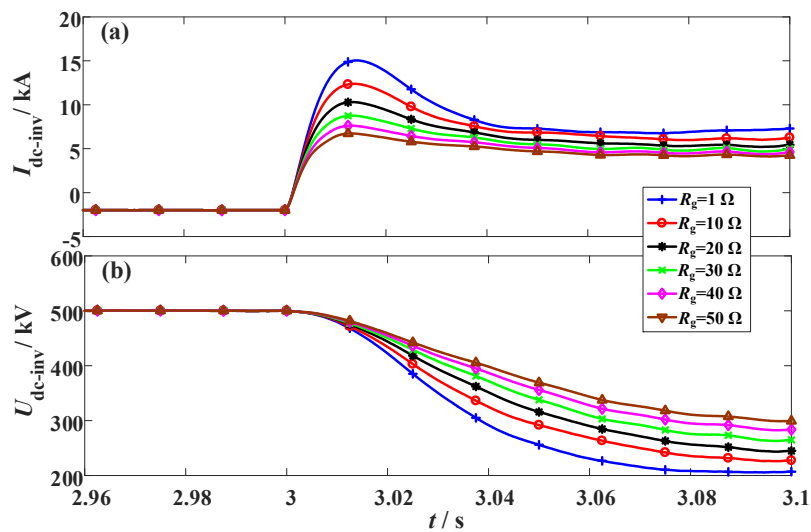
**Figure 11.** Energy dissipation of the two SFCLs subject to the change of the SFCL resistance  $R_{SFCLi}$ .

### 3.3. Changing the Fault Resistance of the Hybrid HVDC

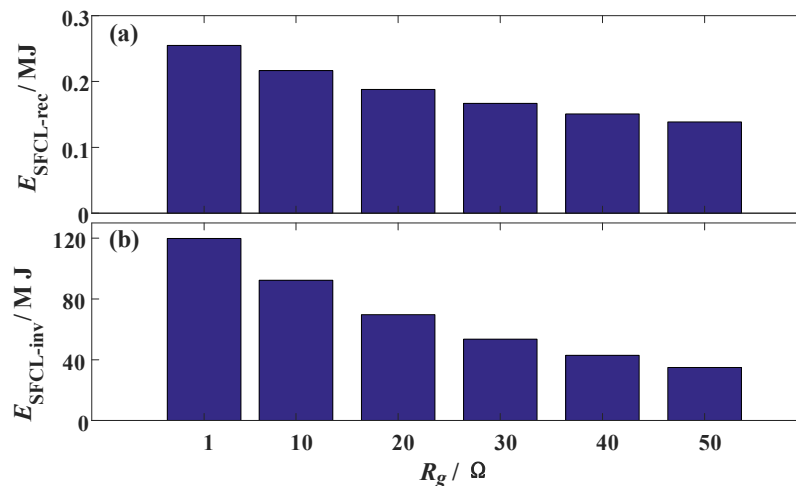
As the fault resistance is a critical factor to evaluate the fault severity level and the behavioral interaction between the LCC and VSC stations, different fault resistances are simulated. The parameters of  $R_{SFCLr} = 20 \Omega$  and  $R_{SFCLi} = 30 \Omega$  are adopted, and the settings of the fault time and fault location are unchanged. The simulation waveforms are shown in Figures 12–14.



**Figure 12.** Properties of the LCC station considering the change of the fault resistance  $R_g$ . (a) DC current and (b) DC voltage.



**Figure 13.** Properties of the VSC station considering the change of the fault resistance  $R_g$ . (a) DC current and (b) DC voltage.



**Figure 14.** Energy dissipation of the two SFCLs subject to the change of the fault resistance  $R_g$ .

From Figure 12, the main contribution of augmenting the fault resistance for the LCC station is to mitigate the DC voltage drop. The DC fault current still decreases to zero, but the DC voltage can be properly kept owing to the voltage support over the fault resistance. In the case of that the fault resistance is set as 10  $\Omega$ , 20  $\Omega$ , 30  $\Omega$ , 40  $\Omega$ , and 50  $\Omega$ , respectively, the DC voltage will reach to 50.8 kV, 88.6 kV, 119.2 kV, 143.1 kV, and 164.7 kV, respectively.

From Figure 13, the DC current and voltage of the VSC station will be both affected by the fault resistance, and a detailed performance comparison is given in Table 4.

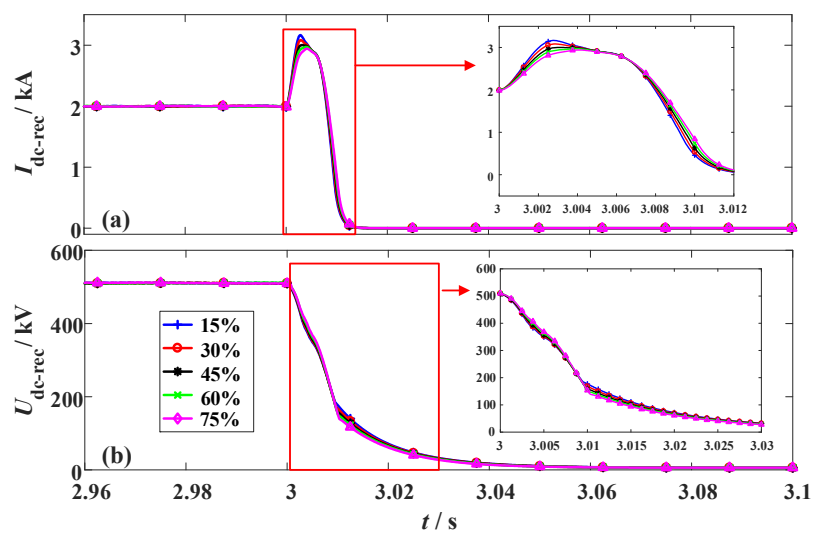
**Table 4.** Influence of the fault resistance on the VSC station.

Items	DC Fault Current		DC Voltage	
	No SFCL	With SFCL/Current-Limiting Ratio	No SFCL	With SFCL
$R_g = 10 \Omega$	21.2 kA	12.4 kA/41.7%	99.1 kV	222.2 kV
$R_g = 20 \Omega$	16.1 kA	10.3 kA/36.1%	159.1 kV	239.8 kV
$R_g = 30 \Omega$	12.8 kA	8.76 kA/31.7%	196.9 kV	252.1 kV
$R_g = 40 \Omega$	10.6 kA	7.62 kA/28.3 %	221.5 kV	261.8 kV
$R_g = 50 \Omega$	9.03 kA	6.74 kA/25.4%	239.9 kV	271.9 kV

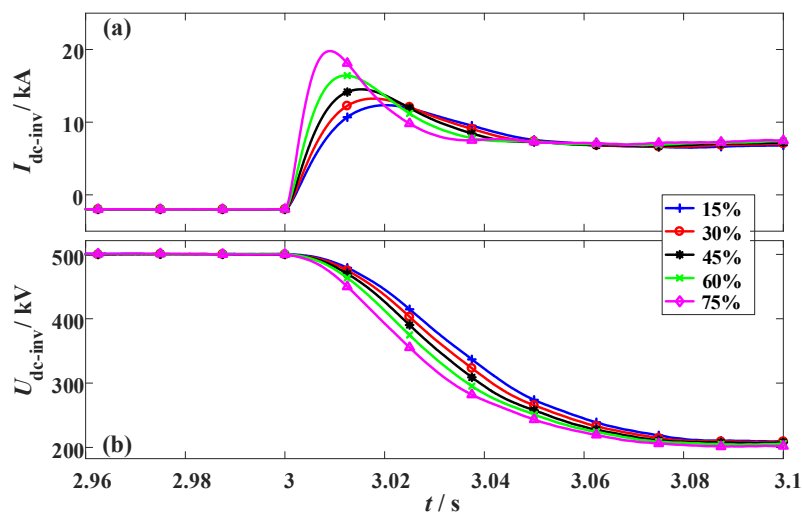
Owing to the increase of the fault resistance, the dissipated energies in the two SFCLs are both reduced. Especially for the SFCL at the VSC station, an evident downswing is observed. For that  $R_g$  is set as 10  $\Omega$ , 20  $\Omega$ , 30  $\Omega$ , 40  $\Omega$ , and 50  $\Omega$ , respectively, the dissipated energy of the SFCL at the VSC station will be 92.3 MJ, 69.7 MJ, 53.6 MJ, 42.9 MJ, and 34.9 MJ, respectively.

### 3.4. Changing the Fault Location of the Hybrid HVDC

To analyze how the fault location could affect the performance of the SFCLs, different fault sites are simulated. The fault location ratio is used to describe the relative position of the fault site in the whole DC line. When the fault location ratio increases, it means the fault site is farther away from the LCC station and closer to the VSC station. The two SFCLs still adopt  $R_{SFCLr} = 20 \Omega$  and  $R_{SFCLi} = 30 \Omega$ ; the fault time and fault resistance are set as  $t_0 = 3 \text{ s}$  and  $R_g = 1 \Omega$ , respectively. The simulation waveforms are shown in Figures 15–17.



**Figure 15.** Simulation waveforms of the LCC station considering the change of the fault location. (a) DC current and (b) DC voltage.



**Figure 16.** Simulation waveforms of the VSC station considering the change of the fault location. (a) DC current and (b) DC voltage.

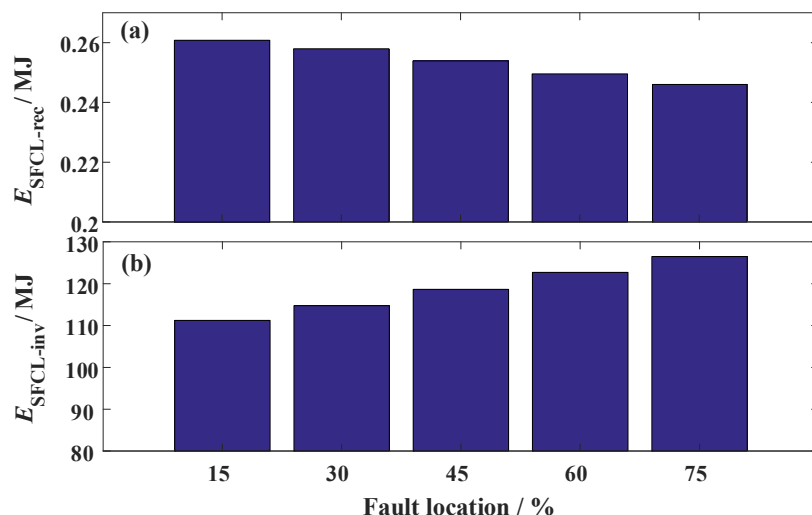


Figure 17. Energy dissipation of the two SFCLs subject to the change of the fault location.

When the fault location ratio changes from 15% to 75%, the peak value of the DC fault current in the LCC station just changes from 3.11 kA to 2.97 kA. Considering that the expected reduction is just 0.14 kA, the SFCL at the LCC station has a low sensitivity to the fault location. In comparison, the DC fault current of the VSC station is more sensitive to the fault site. When the fault location ratio is 15%, 30%, 45%, 60%, and 75%, respectively, the corresponding current-limiting ratio will be about 44.9%, 46.5%, 47.9%, 49.3%, and 50.4%, respectively. It is proven that the SFCL at the VSC station has an enhanced current-limiting ability for handling the short-line faults.

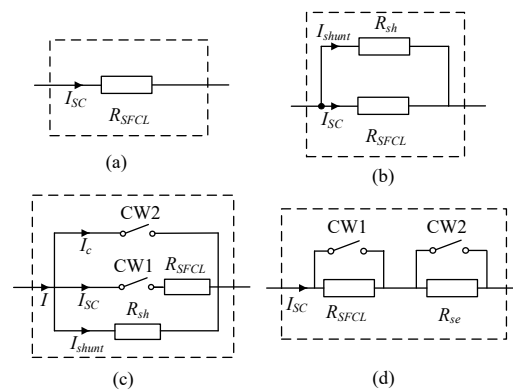
Based on Figure 17, Table 5 shows the simulation data of the two SFCLs' energy dissipation, whose changing trends are opposite with each other.

Table 5. Influence of the fault location on the energy dissipation of the two SFCLs.

Fault Location Ratio	Energy Dissipation	
	SFCL at the LCC Station	SFCL at the VSC Station
15%	0.265 MJ	111.2 MJ
30%	0.258 MJ	114.8 MJ
45%	0.252 MJ	118.7 MJ
60%	0.247 MJ	122.7 MJ
75%	0.243 MJ	126.5 MJ

#### 4. Scheme Design

In this section, the SFCL scheme design is conducted. Firstly, the candidates for the structure of the resistive SFCL used in the HVDC networks are discussed. Figure 18a shows a general structure, which represents a pure resistive SFCL without an external resistor in parallel. Some scholars have applied this structure in [15,18], where the scholars consider the coordination of a high-speed direct-current circuit breaker (DCCB) and the SFCL. As the DCCB cuts off the DC fault current within 2–5 ms, the current-limiting time of the resistive SFCL can be controlled as 20 ms–50 ms. In light of a relatively short current-limiting time, the quench heat dissipation could be acceptable to a certain extent.



**Figure 18.** Candidates for the structure of the resistive SFCL used in the HVDC networks. (a) Pure resistive SFCL; (b) Resistive SFCL with external resistor in parallel; (c) Resistive SFCL with switches and external resistor in parallel; (d) Resistive SFCL with external resistor in series.

Figure 18b,c show two possible structures for the resistive SFCL with an external resistor in parallel [13,16,32]. In a sense, the scholars adopt a conservative and safe method, and the objective of introducing the external resistor is to avoid that the recovery process of the SFCL is too long. In addition, Figure 18d shows the structure of the resistive SFCL with an external resistor in series. The rating of the external resistor is the same as that of the resistive SFCL. When CW1 is closed and CW2 is opened, the external resistor will replace the SFCL to mitigate the fault transients. Hence, the current-limiting time of the resistive SFCL can be flexibly adjusted to ensure the safety and reliability of superconducting materials.

In this study, our research group prefers to use the general structure in Figure 18a. In case of this structure does not fully meet the requirement that the recovery time of the SFCL is about 4 s, the structure in Figure 18d can be regarded as an alternative solution. It should be noted that, the alternative structure may have the same current-limiting resistance as the preferred structure, and it does not affect the above simulation results of the DC current and voltage. In the following, the parameter selection is discussed.

For the LCC station, this study suggests installing the resistive SFCL with a lower quench resistance (no more than 20  $\Omega$ ). On the one hand, it may cooperate with the firing angle controller to combinedly handle the DC fault issue. On the other hand, it may assist the SFCL at the VSC station to more powerfully handle the AC fault when the fault location is near the AC grid 1.

For the VSC station, this study recommends applying the resistive SFCL with  $R_{SFCLi} = 30 \Omega$ , which is sufficient to alleviate the DC voltage-current fluctuations and dissipate the active power. As shown in Figure 19, the power response of the AC systems is demonstrated, and here the fault resistance is  $R_g = 1 \Omega$ ; the fault location is the middle of the DC transmission line.

Note that, it is not suggested to augment the SFCL resistance in excess. There might be a critical resistance value to depict the tradeoff among the SFCL cost, the fault current reduction and the inhibition of the voltage fluctuation [33]. Since detailed optimization and calculation are out of the scope of this paper, and will be presented in another report, a reasonable choice of  $R_{SFCLi} = 30 \Omega$  is adopted to implement the SFCL's scheme design.

On basis of [34,35], a non-inductive unit coil for the SFCL is designed, and the coil parameters are listed in Table 6. To construct the SFCL at the VSC station, the normal current in the SFCL is 2 kA, and thus 15 pieces of coils connected in parallel are served as a coil group, which can meet the requirements of current capacity and safety margin. Further, 160 coil-groups connected in series is to obtain the quench resistance of 30  $\Omega$ .

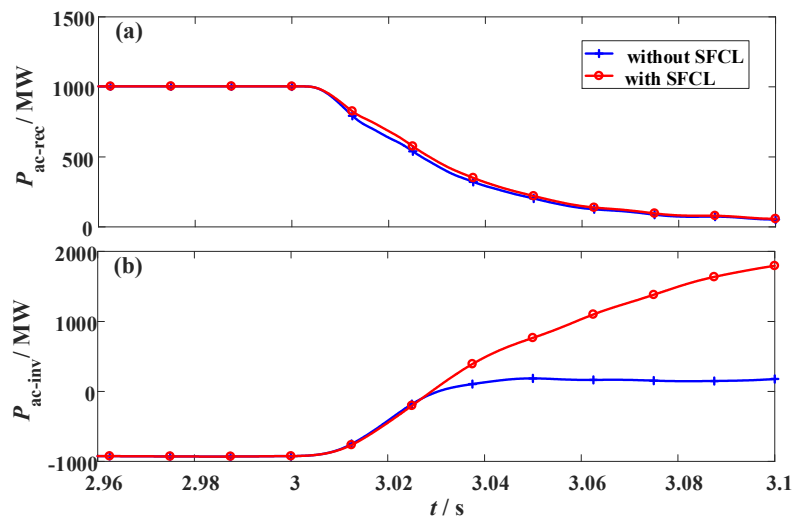


Figure 19. Power response of the AC systems under the fault. (a) AC grid 1 and (b) AC grid 2.

Table 6. Parameters of a non-inductive coil unit.

Parameter	Value
Length of YBCO tape (m)	54
Inner diameter (mm)	200
Outer diameter (mm)	870
Interturn gap (mm)	5
Resistance ( $\Omega$ )	1.28 $\Omega$ @ 100 K
Resistance ( $\Omega$ )	2.98 $\Omega$ @ 300 K
N Value ( $\mu V/cm$ )	38.6
Rated voltage (kV)	3
Break-down voltage (kV)	15
Rated current (A)	200
Peak current (A, with a duration of 100 ms)	900
Safety temperature limit (K)	300

## 5. Conclusions

In this paper, the application feasibility of resistive-type superconducting fault current limiters in a hybrid high voltage direct current transmission system is verified. The main conclusions are as follows:

1. The superconducting fault current limiter at the voltage source converter station enables to very efficiently mitigate the fault transients, and owns an enhanced current-limiting ability for handling the short-line faults. A moderate increase of the current-limiting resistance can bring better contributions, but an excessive increase may make the current-limiting ratio come up to the saturated level.
2. The superconducting fault current limiter at the line commutated converter station is able to mildly limit the fault current and alleviate the voltage drop, and its working performance has a low sensitivity to the fault location. As for the primary and secondary factors, the firing angle controller and the superconducting fault current limiter will combinedly handle the fault transients.

Concerning our future tasks, the optimization design, and economic evaluation of the superconducting fault current limiters will be done. Besides, the effects of the superconducting fault current limiters on the integration of large-scale renewable power sources into the hybrid system will be explored. These mentioned studies will be presented in the follow-up reports.

**Author Contributions:** L.C. helped design the study and write the manuscript; H.H. helped analyze the data; G.L. helped build the simulation model; H.C. helped conduct the study; L.W. helped analyze the HVDC model; X.C. helped conduct the device scheme; X.T. helped draw the figure; Y.X. helped conduct the simulation analysis; L.R. helped conduct the superconductor parameters; Y.T. helped edit the manuscript.

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**Conflicts of Interest:** The authors declare no conflict of interest.

## Nomenclature

LCC	Line commutated converter
VSC	Voltage source converter
RMS	Root mean square
FRT	Fault ride-through
HVDC	High voltage direct current
SFCL	Superconducting fault current limiter
YBCO	Yttrium barium copper oxide
VOCOL	Voltage-dependent current order limiter

## Symbols

$I$	Current [A]	$R$	Resistance [ $\Omega$ ]
$X$	Reactance [ $\Omega$ ]	$U$	Voltage [V]
$P$	Power [W]	$\alpha$	Firing angle [Degree]
$M$	Modulation ratio [-]	$L$	Inductance [H]
$C$	Capacitance [F]		

## Subscripts

$c$	Commutation	$f$	Fault
$T$	Transformer	$r$	Rectifier side
$i$	Inverter side	$g$	Ground
$ac$	Alternating current	$dc$	Direct current
$sm$	Smoothing reactor	$min$	Minimum

## Appendix A

### Appendix A.1. LCC Station Modeling

Figure A1 shows the connection diagram and equivalent circuit of the LCC station.  $U_{ac1}$  and  $X_{ac1}$  are the equivalent voltage and reactance of the AC grid coupled to the LCC station, respectively;  $X_{T1}$  is the transformer leakage reactance;  $I_{LCC}$  and  $U_{dcr}$  indicate the equivalent AC current and DC voltage sources of the LCC station.

The switching functions of the AC current and the DC voltage are  $S_{LCC-abc}$  ( $S_{LCC-ai}$ ,  $S_{LCC-bi}$ ,  $S_{LCC-ci}$ ) and  $S_{LCC-abcu}$  ( $S_{LCC-au}$ ,  $S_{LCC-bu}$ ,  $S_{LCC-cu}$ ), respectively. The mathematical equations are obtained as follows:

$$\begin{bmatrix} i_{LCC-a} \\ i_{LCC-b} \\ i_{LCC-c} \end{bmatrix} = \begin{bmatrix} S_{LCC-ai} \\ S_{LCC-bi} \\ S_{LCC-ci} \end{bmatrix} I_{dcr} \quad (A1)$$

$$\begin{bmatrix} U_{LCC-a} \\ U_{LCC-b} \\ U_{LCC-c} \end{bmatrix} = [ S_{LCC-au} \quad S_{LCC-bu} \quad S_{LCC-cu} ]^{-1} U_{dcr} \quad (A2)$$



where  $I_{dcr}$  is the DC current of the LCC station;  $U_{LCC}$  is the voltage over the equivalent AC current source.

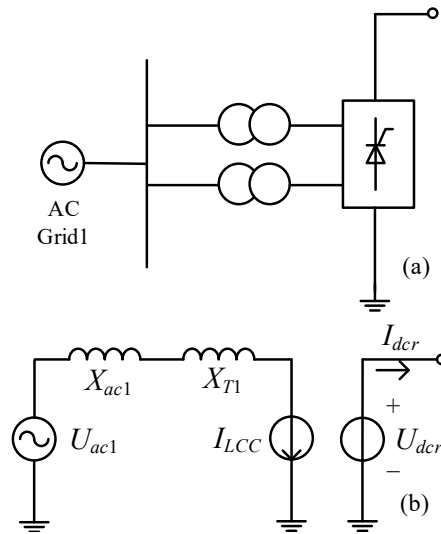


Figure A1. LCC station. (a) Connection diagram, (b) equivalent circuit.

Appendix A.2. VSC Station Modeling

Figure A2 shows the connection diagram and equivalent circuit of the VSC station.  $U_{ac2}$  and  $X_{ac2}$  are the equivalent voltage and reactance of the AC grid coupled to the VSC station, respectively;  $X_{T2}$  is the leakage reactance of the converter transformer;  $X_{VSC}$  is the series reactance of the VSC;  $U_{VSC}$  and  $I_{dci}$  are the equivalent AC voltage and DC current sources of the VSC station.

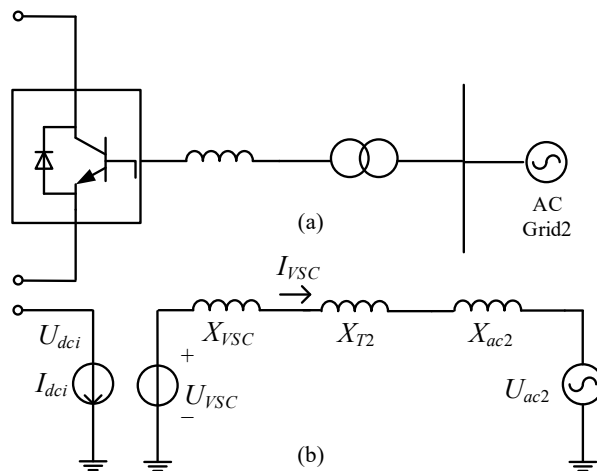


Figure A2. VSC station. (a) Connection diagram, (b) equivalent circuit.

The equations of voltage and current can be modeled as:

$$\begin{bmatrix} U_{VSC-a} \\ U_{VSC-b} \\ U_{VSC-c} \end{bmatrix} = \begin{bmatrix} S_{VSC-au} \\ S_{VSC-bu} \\ S_{VSC-cu} \end{bmatrix} U_{dci} \tag{A3}$$

$$\begin{bmatrix} I_{VSC-a} \\ I_{VSC-b} \\ I_{VSC-c} \end{bmatrix} = [ S_{VSC-ai} \quad S_{VSC-bi} \quad S_{VSC-ci} ]^{-1} I_{dci} \tag{A4}$$

Appendix A.3. Control Modeling

Figure A3 shows the basic control curves of the hybrid HVDC system. For the LCC station (rectifier side), it configures a constant dc current controller and a voltage-dependent current order limiter (VDCOL). For the VSC

station (inverter side), it adopts a direct current control mode, including an outer-loop voltage/reactive power controller and an inner-loop current controller.

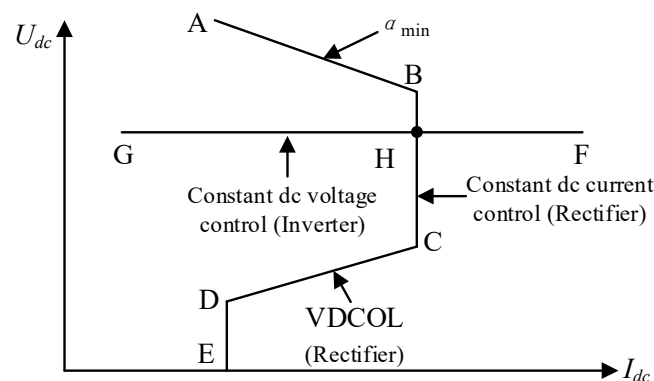


Figure A3. Basic control curves of the hybrid HVDC system.

#### Appendix A.4. The solution of the DC Fault Current in the VSC Station

To seek a solution of the DC fault current in the VSC station, two assumptions are applied:

- (i) Once the firing angle controller of the LCC station is activated, the DC fault current of the LCC station can be down to zero in a relatively short period after the fault;
- (ii) The fault resistance is very little.

Supposing that the initial DC voltage and current are respectively marked as  $U_0$  and  $I_0$ , the following equations are obtained:

$$U_{dci} = A_1 e^{\lambda_1 t} + A_2 e^{\lambda_2 t} \quad (\text{A5})$$

$$I_{dci-f} = C_{VSC} (A_1 \lambda_1 e^{\lambda_1 t} + A_2 \lambda_2 e^{\lambda_2 t}) \quad (\text{A6})$$

where  $\lambda_1, \lambda_2, A_1, A_2$  are expressed as:

$$\lambda_{1,2} = -\frac{R_{SFCLi} + R_{dci} + R_g}{2(L_{smr} + L_{dcr})} \pm \sqrt{\left(\frac{R_{SFCLi} + R_{dci} + R_g}{2(L_{smr} + L_{dcr})}\right)^2 - \frac{1}{(L_{smr} + L_{dcr})C_{VSC}}} \quad (\text{A7})$$

$$\begin{cases} A_1 = \frac{\lambda_2 U_0 + I_0 / C_{VSC}}{\lambda_2 - \lambda_1} \\ A_2 = \frac{\lambda_1 U_0 + I_0 / C_{VSC}}{\lambda_1 - \lambda_2} \end{cases} \quad (\text{A8})$$

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