

Communication

Facile Process for Surface Passivation Using $(\text{NH}_4)_2\text{S}$ for the InP MOS Capacitor with ALD Al_2O_3

Jung Sub Lee ¹, Tae Young Ahn ^{1,*}  and Daewon Kim ^{2,*}

¹ Department of Orthopaedic Surgery and Medical Research Institute, Pusan National University Hospital, 179 Gudeok-ro, Seo-gu, Busan 49241, Korea; jungsublee@pusan.ac.kr

² Department of Electronic Engineering, Institute for Wearable Convergence Electronics, Kyung Hee University, 1732 Deogyong-daero, Giheung-gu, Yongin 17104, Korea

* Correspondence: falconbleu@daum.net (T.Y.A.); daewon@khu.ac.kr (D.K.)

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Abstract: Ammonium sulfide $(\text{NH}_4)_2\text{S}$ was used for the passivation of an InP (100) substrate and its conditions were optimized. The capacitance–voltage (C–V) characteristics of InP metal-oxide-semiconductor (MOS) capacitors were analyzed by changing the concentration of and treatment time with $(\text{NH}_4)_2\text{S}$. It was found that a 10% $(\text{NH}_4)_2\text{S}$ treatment for 10 min exhibits the best electrical properties in terms of hysteresis and frequency dispersions in the depletion or accumulation mode. After the InP substrate was passivated by the optimized $(\text{NH}_4)_2\text{S}$, the results of x-ray photoelectron spectroscopy (XPS) and the extracted interface trap density (D_{it}) proved that the growth of native oxide was suppressed.

Keywords: III–V semiconductor; indium phosphide (InP), Al_2O_3 ; $(\text{NH}_4)_2\text{S}$; sulfur passivation

1. Introduction

As silicon-based, complementary metal-oxide-semiconductor (CMOS) technology has been approaching its fundamental limits, III–V semiconductors have been focused on as alternative channel materials due to their high electron mobility. In particular, indium phosphide (InP) is considered one of the promising materials due to its larger band gap than silicon (~1.34 eV), which results in low off-state leakage current and high breakdown field [1–3]. In addition, InP is preferred to a barrier layer between the gate oxide and the $\text{In}_x\text{Ga}_{1-x}\text{As}$ channel [4]. Despite these advantages, the poor interfacial quality between a high-k dielectric and an InP substrate compared to SiO_2 and Si is still a major obstacle to overcome before high-performance MOS field-effect-transistors (MOSFETs) can be realized. Thus, every endeavor to keep the InP substrate clear of the native oxide growth and external contamination prior to deposition of the high-K dielectric is required for a reduction of D_{it} . For this purpose, ex situ cleaning methods using wet chemicals, such as HCl, H_2SO_4 , NH_4OH , and HF, have consistently been developed [5]. Various works have been done for the enhancement of the interfacial quality over the last few decades [6–8]. Recently, Cuypers et al. reported that sulfur passivation by $(\text{NH}_4)_2\text{S}$ was useful for suppressing unwanted effects arising from pre-existing defects and the rapid re-oxidation of the surface after wet chemical cleaning [9]. As the group VI element, sulfur and oxygen have the same number of valence electrons; however, the electronegativity of sulfur is lower than that of oxygen. Hence, the interface of In–S become stable so that the formation of the native oxide can be effectively inhibited. To take advantage of this feature, $(\text{NH}_4)_2\text{S}$ has widely been employed [1–3,10–13]. However, comprehensive analyses regarding the process parameters used in sulfur passivation which affect the InP MOSFETs remain insufficient.

In this work, the conditions of $(\text{NH}_4)_2\text{S}$ passivation were optimized to enhance the performance of the device. The electrical characteristics of an InP MOS capacitor (MOSCAP) were investigated

while varying the passivation conditions of $(\text{NH}_4)_2\text{S}$, in this case the concentration and treatment time. Then, the chemical properties of the sulfur-passivated interface with the optimized conditions were compared with those of a non-passivated interface. Furthermore, the D_{it} distribution across the InP energy bandgap was extracted using a conductance method [14–17] in order to evaluate the interfacial quality, which affects the performances of InP MOSFETs.

2. Experimental

MOSCAPs were fabricated on an undoped InP (100) wafer with an n-type carrier concentration of $5 \times 10^{15} \text{ cm}^{-3}$. Initially, the substrates were cleaned with a 1% HF solution for 5 min, after which they were treated with $(\text{NH}_4)_2\text{S}$ at concentrations of 1%, 5%, 10%, and 22% which were diluted by deionized H_2O for 10 min at room temperature (300 K). Other substrates were treated with the fixed concentration of 10% $(\text{NH}_4)_2\text{S}$ for 5 min, 10 min, and 30 min. As the gate oxide, 7 nm of Al_2O_3 was deposited on the substrate at a temperature of 150 °C by means of atomic layer deposition (ALD) after a rinse by water was performed. In the ALD process, trimethylaluminum (TMA) and H_2O were sequentially supplied under purging with N_2 during each deposition cycle. For a gate electrode, 10 nm of Ni and 100 nm of Au were deposited using a thermal evaporator through a shadow mask. Afterwards, the MOSCAPs were annealed with ambient gas (4% $\text{H}_2/96\% \text{N}_2$) at 400 °C for 30 min.

3. Discussion and Results

The structural properties of the Au/Ni/ Al_2O_3 /InP samples were characterized by high-resolution transmission electron microscopy (HR-TEM) using a field-emission transmission microscope operated at 300 kV (Tecnai G2 F30). In order to study the bonding status at the Al_2O_3 /InP interface, ex situ X-ray photoelectron spectroscopy (XPS) was analyzed using a monochromated Al K α (1486.7 eV) source with a base pressure in the mid- 10^{-10} Torr range. Capacitance–voltage (C–V) and conductance–voltage (G–V) measurements were carried out using an E4980A precision LCR meter at room temperature.

A schematic of the MOSCAP is shown in Figure 1a. Al_2O_3 was deposited over the entire InP substrate. Afterwards, patterned Ni and Au were deposited through a shadow mask which had holes with a diameter of 300 μm . Figure 1b shows a cross-sectional HR-TEM image of the MOSCAP on the InP substrate, which was treated with the 10% $(\text{NH}_4)_2\text{S}$ solution for 10 min. The TEM image indicates that the ALD Al_2O_3 has a uniform thickness and an amorphous structure. Moreover, an abrupt interface was created without the growth of the native oxide.

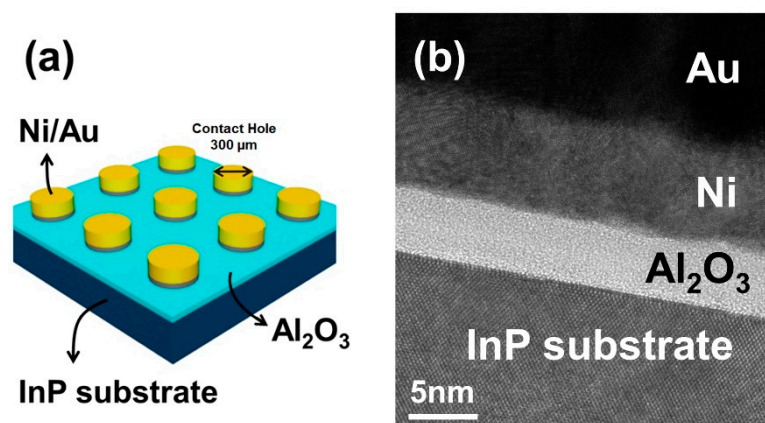


Figure 1. (a) Device schematic for the InP metal-oxide-semiconductor (MOS) capacitor. (b) HR-TEM image of 7 nm thick Al_2O_3 on the InP (100) substrate.

Figure 2a–e shows the C–V characteristics of the devices treated with diluted $(\text{NH}_4)_2\text{S}$ solutions at different concentrations. Three issues exist in all of the curves. First, the accumulation capacitance cannot reach the theoretical value of the oxide capacitance, which is calculated according to the actual thickness of the gate dielectric. This phenomenon originates from the low density of states (DOS) of the InP substrate above the conduction band. Secondly, there is frequency dispersion in the depletion mode, an indicator of the level of D_{it} , which is an important characteristic in terms of enhancing the performance of MOSFETs. Lastly, there is also frequency dispersion in the accumulation mode. This is associated with conductive losses, which are mostly caused by border traps located in the gate dielectric near the interface [16,18,19]. As shown in Figure 2f, hysteresis and frequency dispersion in the accumulation are effectively suppressed in the sample treated with the 10% $(\text{NH}_4)_2\text{S}$ solution. Consequentially, the smallest D_{it} and border trap distribution were achieved by the 10% $(\text{NH}_4)_2\text{S}$ treatment, whereas $(\text{NH}_4)_2\text{S}$ concentrations of 1% and 5% were not sufficient for substrate passivation, and a concentration of 22% resulted in excessive surface roughness [20].

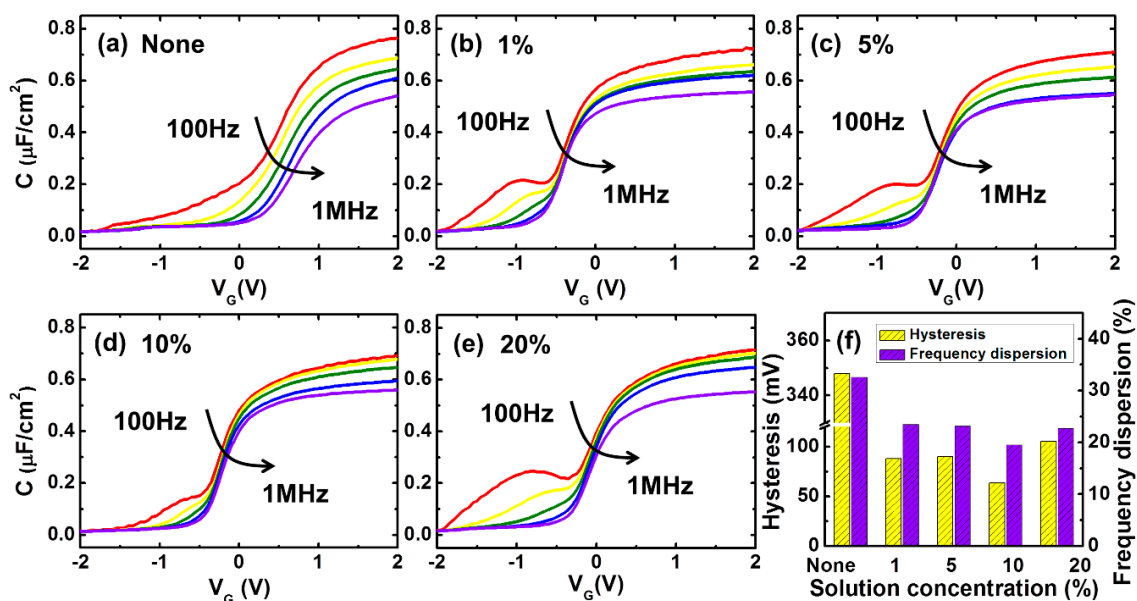


Figure 2. The capacitance–voltage (C–V) characteristics of (a) 0%, (b) 1%, (c) 5%, (d) 10%, and (e) 22% $(\text{NH}_4)_2\text{S}$ treated Au/Ni/ Al_2O_3 /InP. They were measured at room temperature under various frequencies of 100 Hz, 1 kHz, 10 kHz, 100 kHz, and 1 MHz. (f) Measured hysteresis at 100 kHz for all samples. Frequency dispersion of the accumulation capacitance ranging from 100 Hz to 1 MHz (four decades).

Subsequently, based on a concentration of 10%, a short-term treatment time such as 5 or 10 min is proper for passivation, while a longer treatment time such as 30 min could attack the surface akin to the process with the 22% solution at 10 min (refer to the Supplementary Figure S1). On the other hand, other concentrations are also able to passivate the substrate, but they are not appropriate, because the 1% and 5% solutions require longer treatment times and 22% causes excessive surface roughening; there are no additional advantages compared with 10%. In this regard, another substrate, such as $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ [8,21] or InSb [20], shows the same trend depending on the concentration and treatment time of the solution. Therefore, the 10% $(\text{NH}_4)_2\text{S}$ solution for 10 min is an optimal passivation condition for the InP (100) as well as other III–V substrates to attain the best electrical characteristics.

Using the 10% $(\text{NH}_4)_2\text{S}$ treatment as the optimum condition for InP substrates, the interface characteristics of Al_2O_3 /InP were further studied through an analysis of the chemical properties and D_{it} distributions beyond the electrical properties.

Figure 3a,b shows the In 3d core level spectra of InP substrates with or without sulfur passivation, respectively. There are three deconvoluted peaks caused by the native oxides of indium oxides— InO , $\text{InPO}_4/\text{In}(\text{PO}_3)_3$, and InPO_x with binding energy levels of 444.9 eV, 445.5 eV, and 446.1 eV, apart

from another peak caused by the InP substrate with a binding energy of 444.4eV [9,22]. Importantly, according to a comparison of Figure 3a,b, the peaks related to $\text{InPO}_4/\text{In}(\text{PO}_3)_3$ and InPO_x were reduced due to sulfur passivation, which prevented the native oxide from growing. A similar trend was also observed at P 2*p* core level spectra of the InP substrate, as shown in Figure 3c,d. There were two peaks caused by $\text{In}(\text{PO}_3)_3$ and the InP substrate with binding energies of 134.1 and 129 eV [9,22]. In addition to the In 3*d* spectra, the P 2*p* spectra also indicated that the native oxide was reduced due to sulfur.

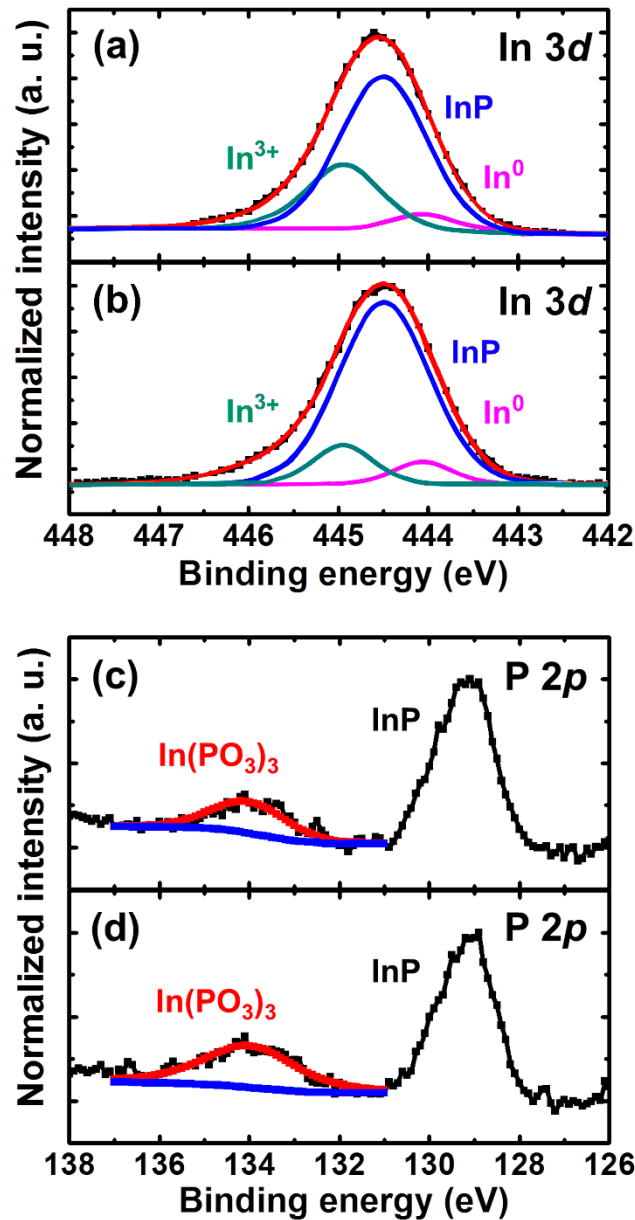


Figure 3. The In 3*d* core level XPS spectra of the sample (a) with or (b) without 10% $(\text{NH}_4)_2\text{S}$ treatment. The P 2*p* core level spectra of the sample (c) with or (d) without 10% $(\text{NH}_4)_2\text{S}$ treatment.

Figure 4 illustrates G–V contour maps and the D_{it} extracted from the InP MOSCAPs with or without sulfur passivation. These contour maps exhibit the magnitude of the normalized parallel conductance, $(G_p/\omega)/Aq$, versus both the AC frequency and the gate voltage, where ω is the frequency, A is the area of the MOSCAP, and q is the elementary charge. From the contour maps, the line to connect the maximum value of $(G_p/\omega)/Aq$ represents the band bending efficiency and the Fermi level movement with gate bias [15,23,24]. The maximum value of $(G_p/\omega)/Aq$ increases with a steeper slope

with the 10% $(\text{NH}_4)_2\text{S}$ compared to the case with no sulfur passivation, as shown in Figure 4a,b. Therefore, it should be noted that the sulfur passivation leads to the depinning of the Fermi level, making the band bending more efficient. Moreover, border traps were validated again. In the case with no passivation, the $(G_p/\omega)/Aq$ peak spreads over the entire frequency range in the accumulation, compared to the case with 10% $(\text{NH}_4)_2\text{S}$ passivation. This implies that the conductive loss is caused by two factors: border traps and series resistance. The maximum value of $(G_p/\omega)/Aq$ extracted by the measurement equipment was used as the level of the D_{it} distribution across the maps. Figure 4c indicates that the MOSCAP with a sulfur treatment shows a lower D_{it} distribution than that without a sulfur treatment. This result is consistent with the C–V characteristics shown in Figure 2a,d.

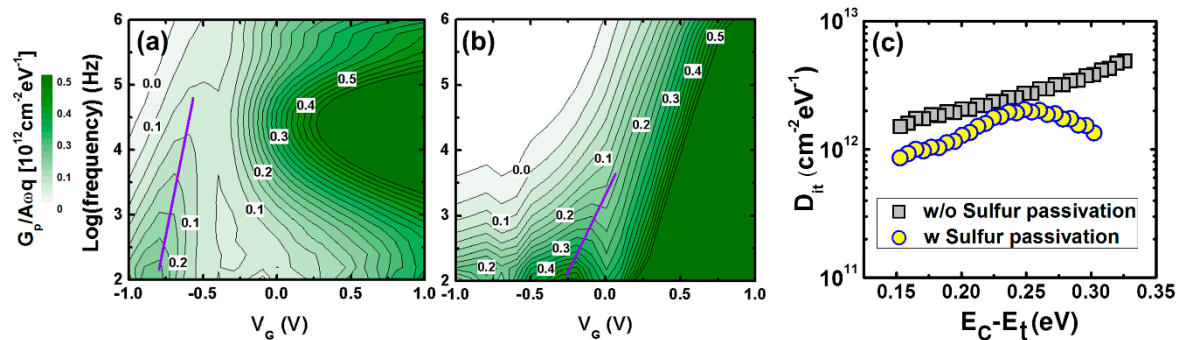


Figure 4. Contour map of normalized conductance $(G_p/\omega)/Aq$ as a function of frequency and gate bias for MOSCAPs (a) without or (b) with 10% $(\text{NH}_4)_2\text{S}$ treatment. (c) D_{it} distribution across the InP energy bandgap extracted from the conductance method for MOSCAPs with or without 10% $(\text{NH}_4)_2\text{S}$ treatment.

4. Conclusions

The effects of $(\text{NH}_4)_2\text{S}$ passivation with various concentrations and treatment times were investigated. Two characterization methods, an electrical method and a chemical method, were employed for comprehensive analyses of the surface properties. In terms of the electrical characteristics, the 10% $(\text{NH}_4)_2\text{S}$ treatment for 10 min was the optimal condition to improve the electrical properties of devices built on InP (100) substrates. This was supported by both the C–V plot and the G–V contour map in terms of the frequency dispersions and hysteresis. In terms of the chemical characteristics, the device with the 10% $(\text{NH}_4)_2\text{S}$ treatment for 10 min showed relatively low native oxide peaks, particularly arising from the phosphorus-related oxide compared to that without sulfur passivation. This was supported by XPS data. Finally, it was also found that the level of D_{it} was lower in the device with the 10% $(\text{NH}_4)_2\text{S}$ treatment than in the device with no sulfur passivation. The proposed strategy to optimize the conditions of diluted $(\text{NH}_4)_2\text{S}$ provides a guideline for further improvements of InP-based high-performance CMOS technology.

Supplementary Materials: The following are available online at <http://www.mdpi.com/1996-1944/12/23/3917/s1>, Figure S1: The capacitance-voltage characteristics of the Au/Ni/ Al_2O_3 /InP which was treated on 10% $(\text{NH}_4)_2\text{S}$ for (a) 5, and (b) 10, and (c) 30 min. Measurement frequencies are 100 Hz, 1 kHz, 10 kHz, 100 kHz, and 1 MHz.

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Zhao, H.; Shahrjerdi, D.; Zhu, F.; Kim, H.S.; Ok, I.; Zhang, M.; Yum, J.H.; Banerjee, S.K.; Lee, J.C. Inversion-type indium phosphide metal-oxide-semiconductor field-effect transistors with equivalent oxide thickness of 12 Å using stacked HfAlO_x/HfO₂ gate dielectric. *Appl. Phys. Lett.* **2008**, *92*, 203506.
2. Wu, Y.Q.; Xuan, Y.; Shen, T.; Ye, P.D.; Cheng, Z.; Lochtefeld, A. Enhancement-mode InP n-channel metal-oxide-semiconductor field-effect transistors with atomic-layer-deposited Al₂O₃ dielectrics. *Appl. Phys. Lett.* **2007**, *91*, 022108. [[CrossRef](#)]
3. Chen, Y.-T.; Zhao, H.; Yum, J.H.; Wang, Y.; Lee, J.C. Metal-oxide-semiconductor field-effect-transistors on indium phosphide using HfO₂ and silicon passivation layer with equivalent oxide thickness of 18 Å. *Appl. Phys. Lett.* **2009**, *94*, 92–95. [[CrossRef](#)]
4. Zhao, H.; Chen, Y.-T.; Yum, J.; Wang, Y.; Zhou, F.; Xue, F.; Lee, J.C. Effects of barrier layers on device performance of high mobility In_{0.7}Ga_{0.3}As metal-oxide-semiconductor field-effect-transistors. *Appl. Phys. Lett.* **2010**, *96*, 102101. [[CrossRef](#)]
5. Black, L.E.; Cavalli, A.; Verheijen, M.A.; Haverkort, J.E.M.; Bakkers, E.P.A.M.; Kessels, W.M.M. Effective Surface Passivation of InP Nanowires by Atomic-Layer-Deposited Al₂O₃ with PO_x Interlayer. *Nano Lett.* **2017**, *17*, 6287. [[CrossRef](#)] [[PubMed](#)]
6. Iyer, R.; Chang, R.R.; Lile, D.L. Sulfur as a surface passivation for InP. *Appl. Phys. Lett.* **1988**, *53*, 134. [[CrossRef](#)]
7. Klopfenstein, P.; Bastide, G.; Rouzeyre, M. Interface studies and electrical properties of plasma sulfide layers on n-type InP. *J. Appl. Phys.* **1988**, *63*, 150. [[CrossRef](#)]
8. Herman, J.S.; Terry, F.L. Hydrogen sulfide plasma passivation of indium phosphide. *J. Electron. Mater.* **1993**, *22*, 119. [[CrossRef](#)]
9. Cuypers, D.; van Dorp, D.H.; Tallarida, M.; Brizzi, S.; Rodriguez, L.; Conard, T.; Arnauts, S.; Schmeisser, D.; Adelman, C.; de Gendt, S. Study of InP Surfaces after Wet Chemical Treatments. *ECS Trans.* **2013**, *58*, 297–303. [[CrossRef](#)]
10. Yen, C.-F.; Lee, M.K. Very Low Leakage Current of High Band-Gap Al₂O₃ Stacked on TiO₂/InP Metal–Oxide–Semiconductor Capacitor with Sulfur and Hydrogen Treatments. *Jpn. J. Appl. Phys.* **2012**, *51*, 1201.
11. Gu, J.J.; Neal, A.T.; Ye, P.D. Effects of (NH₄)₂S passivation on the off-state performance of 3-dimensional InGaAs metal-oxide-semiconductor field-effect transistors. *Appl. Phys. Lett.* **2011**, *99*, 152113. [[CrossRef](#)]
12. Galatage, R.V.; Dong, H.; Zhernokletov, D.M.; Brennan, B.; Hinkle, C.L.; Wallace, R.M.; Vogel, E.M. Electrical and chemical characteristics of Al₂O₃/InP metal-oxide-semiconductor capacitors. *Appl. Phys. Lett.* **2013**, *102*, 132903. [[CrossRef](#)]
13. Alian, A.; Brammertz, G.; Degraeve, R.; Cho, M.; Merckling, C.; Lin, D.; Wang, W.-E.; Caymax, M.; Meuris, M.; Meyer, K.D.; et al. Oxide Trapping in the InGaAs–Al₂O₃ System and the Role of Sulfur in Reducing the Al₂O₃ Trap Density. *IEEE Electron Devices Lett.* **2012**, *33*, 1544–1546. [[CrossRef](#)]
14. Steven, C.; Witczak, J.; Suehle, S.; Gaitan, M. An experimental comparison of measurement techniques to extract Si–SiO₂ interface trap density. *Solid-State Electron.* **1992**, *35*, 345–355.
15. Engel-Herbert, R.; Hwang, Y.; Stemmer, S. Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces. *J. Appl. Phys.* **2010**, *108*, 124101. [[CrossRef](#)]
16. Brammertz, G.; Alian, A.; Lin, H.C.; Meuris, M.; Caymax, M.; Wang, W.-E. A Combined Interface and Border Trap Model for High-Mobility Substrate Metal–Oxide–Semiconductor Devices Applied to In_{0.53}Ga_{0.47}As and InP Capacitors. *IEEE Trans. Electron Devices* **2011**, *58*, 3890–3897. [[CrossRef](#)]
17. Lin, D.H.C.; Brammertz, G.; Sioncke, S.; Nyns, L.; Alian, A.; Wang, W.-E.; Heyns, M.; Caymax, M.; Hoffmann, T. Electrical Characterization of the MOS (Metal–Oxide–Semiconductor) System: High Mobility Substrates. *ECS Trans.* **2011**, *34*, 1065–1070.
18. Kim, E.J.; Wang, L.; Asbeck, P.M.; Saraswat, K.C.; McIntyre, P.C. Border traps in Al₂O₃/In_{0.53}Ga_{0.47}As (100) gate stacks and their passivation by hydrogen anneals. *Appl. Phys. Lett.* **2010**, *96*, 012906. [[CrossRef](#)]
19. Hinkle, C.L.; Galatage, R.V.; Zhernokletov, D.M.; Dong, H.; Anwar, S.R.M.; Brennan, B.; Vogel, E.M. III-V/High-k Defects: DIGS vs. Border Traps. *ECS Trans.* **2013**, *53*, 161–167. [[CrossRef](#)]
20. Zhernokletov, D.M.; Dong, H.; Brennan, B.; Kim, J.; Wallace, R.M. Optimization of the ammonium sulfide (NH₄)₂S passivation process on InSb(111)A. *J. Vac. Sci. Technol. B* **2012**, *30*, 04E103. [[CrossRef](#)]

21. O'Connor, É.; Brennan, B.; Djara, V.; Cherkaoui, K.; Monaghan, S.; Newcomb, S.B.; Contreras, R.; Milojevic, M.; Hughes, G.; Pemble, M.E.; et al. A systematic study of $(\text{NH}_4)_2\text{S}$ passivation (22%, 10%, 5%, or 1%) on the interface properties of the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ system for n-type and p-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ epitaxial layers. *J. Appl. Phys.* **2011**, *109*, 024101. [[CrossRef](#)]
22. Hollinger, G.; Bergignat, E.; Joseph, J.; Robach, Y. On the nature of oxides on InP surfaces. *J. Vac. Sci. Technol. A* **1985**, *3*, 2082. [[CrossRef](#)]
23. Hwang, Y.; Engel-Herbert, R.; Rudawski, N.G.; Stemmer, S. Analysis of trap state densities at $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interfaces. *Appl. Phys. Lett.* **2010**, *96*, 102910. [[CrossRef](#)]
24. Lin, H.C.; Brammertz, G.; Martens, K.; Valicourt, G.; Negre, L.; Wang, W.-E.; Tsai, W.; Meuris, M.; Heyns, M. The Fermi-level efficiency method and its applications on high interface trap density oxide-semiconductor interfaces. *Appl. Phys. Lett.* **2009**, *94*, 153508. [[CrossRef](#)]



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