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Analysis of the THD and Common-Mode Voltage of the Three-Phase Boost-Buck EV Traction Inverter

Yongjie Han [1], Yuan Zhu [1] and Deliang Wu [2,*]

[1] School of Automotive Studies, Tongji University, Shanghai 201804, China; hanyongjie2020@outlook.com (Y.H.); yuan.zhu@tongji.edu.cn (Y.Z.)
[2] School of Mechatronic Engineering and Automation, Shanghai University, Shanghai 200444, China
* Correspondence: wudeliang@shu.edu.cn

Abstract: A three-phase boost-buck inverter (BBI) comprised of three identical boost-buck DC/DC converter modules is presented for an EV traction inverter application. It allows the step-up and/or step-down of the battery pack voltage according to the operating condition of the traction motor so that the overall performance can be optimized, which is essential for EVs with relatively low and varying battery voltages such as a hybrid EV or fuel-cell EV. It also features low switching losses, low harmonic distortion in the output current, and reduced common-mode voltage and/or current. A detailed analysis and performance evaluation of the BBI compared to the conventional technology demonstrate its feasibility in EV traction applications. The functionality and performance of the boost-buck inverter are verified with simulation and experimental results.

Keywords: three-phase inverter; boost-buck inverter; EV traction inverter

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1. Introduction

Traction inverters in Electric Vehicles (EV) have to handle wide operating ranges of the motor corresponding to the complex driving cycle characteristics. The battery voltage also varies depending on the state-of-charge of the widely adopted lithium-ion batteries. In fuel cell (FC)-type EVs, the terminal voltage of the FC stack typically varies in a wide range depending on the load condition. EV motors operate in wide speed and torque ranges, which requires the traction inverter to operate reliably in wide voltage and current ranges. In order to reduce the energy consumption and increase mileage, it is critical for the inverter to be highly efficient under different loading conditions [1–6].

The conventional two-level voltage source inverter (VSI) is widely used in motor drive applications. It has a simple structure and low parts count, which translates into a lower cost and higher reliability. However, the high-power requirement of the EV motor drive still requires paralleling multiple semiconductor power devices either at the chip level or at the power module level [7,8]. The main constraint of this topology is that it only has buck-type functionality, i.e., the amplitude of the ac line-to-line voltage is always lower that the dc input (battery pack) voltage. In the high-speed range of the EV motor, due to the limited output voltage amplitude, field-weakening control is usually adopted to increase the motor speed. However, field-weakening control has the disadvantages of reduced driving torque, higher torque ripple, complicated control, and possible demagnetization of the permanent magnets [9–11].

A two-stage topology, as shown in Figure 1a, consists of a bidirectional boost/buck converter and a VSI, denoted as B-VSI hereafter, has been proposed to enable voltage step-up functionality [1–3]. The dc link voltage can be controlled by the boost converter according to the operating condition of the motor. The design of the battery pack and the motor can then be decoupled so that the system performance can be optimized [12,13]. The operating range of the inverter and the motor is extended, and the motor control in the high-speed range can be simplified. For the control of the inverter, a conventional space

vector PWM (SVPWM) is typically used due to its low total harmonic distortion (THD) of the three-phase output current. However, as the B-VSI is essentially a two-stage topology, more power losses are generated in the switching devices, resulting in a lower efficiency of the inverter.

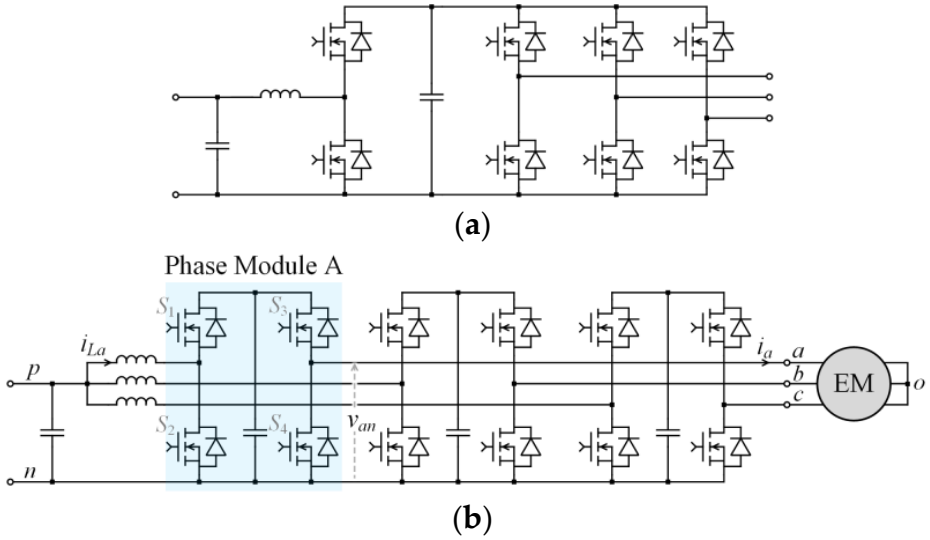

Figure 1. Circuit topology of (**a**) B-VSI: voltage source inverter with a preceding booster stage and (**b**) BBI: boost-buck inverter.

The THD of the Inverter output current is relevant as it directly affects the torque ripple, noise, and eddy current losses in the motor [14–22]. The THD can be reduced by simply increasing the switching frequency. However, due to efficiency requirements and the constraints on the cost and size of the cooling system, the switching frequency of the power switches in the traction inverter is typically limited to a few kilohertz (kHz). Wide-band-gap (WBG) semiconductor power devices such as SiC MOSFETs enable a higher switching frequency due to its much faster switching speed (high dv/dt) and lower switching losses [23]. However, the application of WBG devices exacerbates the challenges associated with a high dv/dt and common-mode (CM) voltage and/or current. CM current or leakage current will be induced by the CM voltage due to the distributed stay capacitances between the winding and the ground [24–26]. The leakage current flows through the motor bearings and may cause damage, which is a major reliability issue [27–29].

A three-phase dc/ac inverter based on modular boost-buck dc/dc converters, denoted as BBI, has been studied in the literature [30]. The BBI has voltage buck and boost functionality and high efficiency. Its operating principle and device loss characteristics have been analyzed, and its efficiency has been evaluated with simulation results. However, detailed analysis of the THD and CM voltage/current characteristics of the BBI has not been found in the literature. This article serves to fill this gap and presents extensive analysis with simulation and experimental validation, including a performance comparison between the BBI and the B-VSI. An interleaving method is also designed so that the ripple in the input current can be reduced.

The operation principle of the BBI is first described in Section 2 to facilitate further analyses. Detailed analysis of the CM voltage and current, THD of the output current, and the design of an interleaving method are presented in Section 3. The analyses are verified by extensive simulation results in Section 4, with the performance comparison between the BBI and B-VSI. Experimental results based on a scaled-down hardware prototype are shown in Section 5, which validates the performance of the BBI. Finally, the conclusions are given in Section 6.

2. Operating Principle

The basic operating principle of the BBI has been described in the literature [30]. It is briefly summarized here to facilitate further analyses and discussions. The BBI topology is shown in Figure 1b. Each phase module of the inverter is a boost-buck converter consisting of two switch legs. The three phase modules are the same, and phase A is explained in detail. The switch leg S1–S2, together with the input inductor L, forms a boost converter. The switch leg S3–S4 forms a buck converter.

The operation modes of phase module A in the BBI are illustrated in Figure 2. When the reference for the phase voltage v_{an} is lower than the input voltage V_{in}, the phase modules operate as a buck converter. S1 is always turned-on and S2 is always turned-off, i.e., the boost switch leg has no switching actions. The buck switch leg is controlled in pulse width modulation (PWM) mode with duty cycle d_2 for S3.

Figure 2. The two modes of a phase module of the BBI: (**a**) boost mode and (**b**) buck mode.

When the reference for the phase voltage v_{an} is higher than the input V_{in}, the phase modules operate as a boost converter. S3 is always turned-on and S4 is always turned-off, i.e., the buck switch leg has no switching actions. The boost switch leg is controlled in pulse width modulation (PWM) mode with duty cycle d_1 for S1. In this mode, the output voltage is filtered by the dc link capacitor of the phase module.

The phase-modules are dc/dc converters that generate positive output voltages consisting of a sinusoidal component and a dc bias:

$$v_{an} = V_{om}\cos(\omega_1 t) + v_{bias} \tag{1}$$

$$v_{bn} = V_{om}\cos\left(\omega_1 t - \frac{2\pi}{3}\right) + v_{bias} \tag{2}$$

$$v_{cn} = V_{om}\cos\left(\omega_1 t + \frac{2\pi}{3}\right) + v_{bias} \tag{3}$$

where V_{om} and ω_1 are the amplitude and angular frequency of the fundamental output voltage of the inverter, respectively. It is assumed that the load has a unity power factor. The overall modulation index is expressed as

$$M = \frac{2V_{om}}{V_{in}} \tag{4}$$

which describes the combined effect of the voltage gain of the boost stage and the modulation depth of the buck (inverter) stage. Due to symmetry of the three phases, only the analysis of phase A is described here.

The discontinuous pulse width modulation (DPWM) strategy is implemented by a bias voltage expressed as

$$v_{bias}(t) = -\min[v_{ao}(t), v_{bo}(t), v_{co}(t)] \tag{5}$$

The operating waveforms of the BBI with the DPWM strategy are shown in Figure 3. Among the three buck switch legs of the three phases, the phase with the most negative

reference voltage is clamped to the negative dc bus for one third of the fundamental period. Therefore, the number of switching actions and the associated switching losses are significantly reduced compared to continuous PWM methods such as the conventional SVPWM.

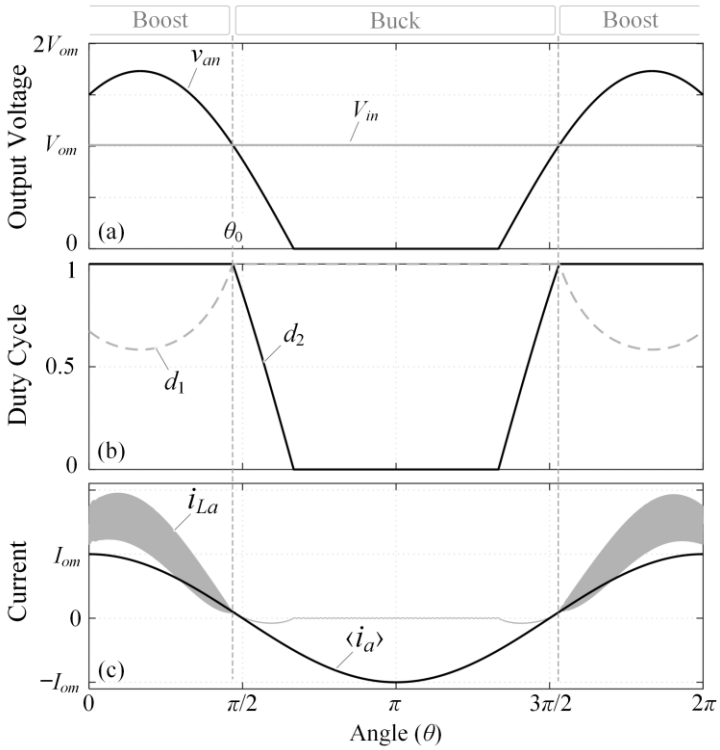

Figure 3. The characteristic waveforms of phase module A of the boost-buck inverter. (**a**) The input voltage V_{in}, reference output voltage v_{an}, (**b**) duty cycle d_1 for the boost switch leg, duty cycle d_2 for the buck switch leg, (**c**) input current i_{La}, and average output current i_a are shown.

As the waveforms are symmetrical about $\theta = \omega_1 t = \pi$, the expressions are derived only for the interval $\theta \in (0,\ \pi]$. The operation of the phase module switches between the buck mode and the boost mode, as shown in Figure 3. By equating the reference voltage and the input voltage, the boundary phase angle between the two modes can be solved and is expressed as

$$\theta_o = \text{acos}\left(\frac{2}{\sqrt{3}M}\right) + \frac{\pi}{6} \tag{6}$$

Based on the characteristics of the buck and boost converter, the control duty cycles for the two switch legs can be expressed as

$$d_1(\theta) = \begin{cases} \dfrac{2}{\sqrt{3}M\cos(\theta - \pi/6)}, & \theta \in (0, \theta_o] \\ 1, & \theta \in (\theta_o, \pi] \end{cases} \tag{7}$$

$$d_2(\theta) = \begin{cases} 1, & \theta \in (0, \theta o] \\ \dfrac{\sqrt{3}Mcos(\theta - \pi/6)}{2}, & \theta \in (\theta o, 2\pi/3] \\ 0, & \theta \in (2\pi/3, \pi] \end{cases} \tag{8}$$

3. CM Voltage, THD, and Interleaving Method

The CM voltage and/or current, THD of the output current, and characteristics of the input current are important factors for the design of a traction inverter. Characteristics of the relevant waveforms are analyzed, and analytical expressions are derived in the following, which can be used for the design and control of the inverter.

3.1. CM Voltage and Current

In motor drive applications, leakage current is induced by the CM voltage due to the high dv/dt of the switching actions and the parasitic elements in the system. The parasitic elements in the electric machines are mainly capacitive due to the large surface area of the windings and the frame, and the small distance between them. The influence of the CM voltage mainly depends on dv/dt and the magnitude of the CM voltage.

Figure 4 illustrates the characteristic waveforms of the output voltages of the three phases (v_{an}, v_{bn}, and v_{cn}, referenced to the negative dc rail), as well as the CM voltage v_{CM} that is equal to the load neutral voltage v_{on}, i.e.,

$$v_{\mathrm{CM}} = v_{on} = (v_{an} + v_{bn} + v_{cn})/3 \tag{9}$$

The waveforms of the output voltages are smooth during the boost mode of the phase modules. The corresponding CM voltage waveform is also smooth when at least two phase modules are in boost mode, which means it does not excite dv/dt-related high-frequency leakage current.

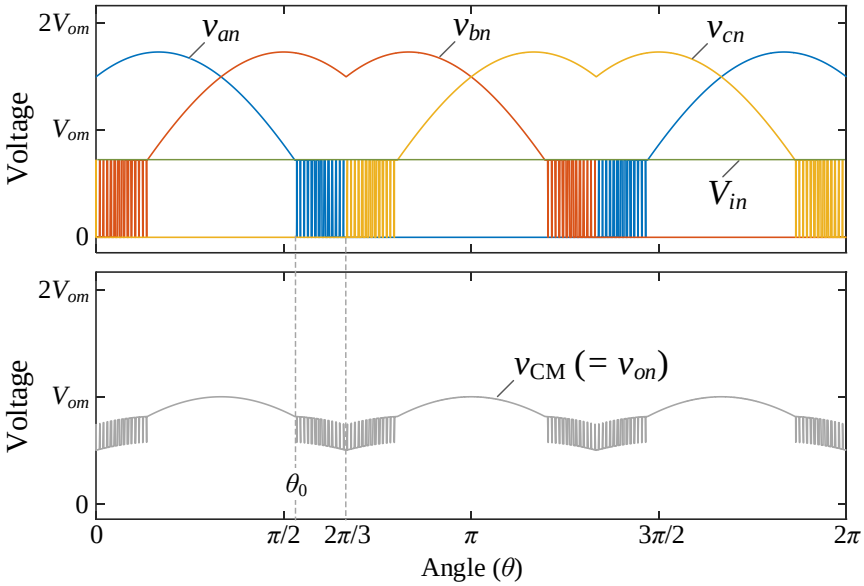

Figure 4. The characteristic waveforms of three-phase output voltages and the CM voltage.

The CM voltage only presents a pulsed pattern when any of the phase modules is in buck mode. For the BBI, the magnitude of the voltage level shift V_{CMP} of the CM voltage pulses is directly related to the lower input voltage, i.e.,

$$V_{CMP,BBI} = V_{in}/3 \tag{10}$$

For the B-VSI, it is directly related to the boosted dc-link voltage, i.e.,

$$V_{CMP,B-VSI} = V_{dclink}/3 \tag{11}$$

Moreover, as the high-frequency pulses occur only in buck mode of the BBI, the average switching frequency corresponding to the high-frequency CM voltage and/or current can be expressed as

$$f_{sw,CM} = \frac{2\left(\frac{2\pi}{3} - \theta_0\right)}{\frac{2\pi}{3}} f_{sw} \tag{12}$$

For the B-VSI, as the three phases are constantly switching when the conventional space vector modulation is used, the average switching frequency is the same as f_{sw}. The amplitude of the leakage current pulses is approximately proportional to V_{CMP}, and the number of leakage current pulses over a fundamental cycle is proportional to $f_{sw,CM}$. The ratio of the RMS leakage current of the BBI to that of the B-VSI, at the same load voltage and power level, can be approximated as

$$\frac{I_{CM,BBI}}{I_{CM,B-VSI}} \approx \frac{V_{in} f_{sw,CM}}{V_{dclink} f_{sw}} \tag{13}$$

When the commanded output voltage is relatively low ($M < 2/\sqrt{3}$), the boost stage is bypassed, and $V_{dclink} = V_{in}$ so that

$$\frac{I_{CM,BBI}}{I_{CM,B-VSI}} \approx \frac{f_{sw,CM}}{f_{sw}} \tag{14}$$

When the commanded output voltage is relatively high ($M \geq 2/\sqrt{3}$), the highest utilization of the dc link voltage is usually adopted, i.e., $V_{dclink} = \sqrt{3} V_{om}$, neglecting nonideal effects such as device voltage drop, dead-band time, and design margin, etc. Equation (13) can then be expressed as

$$\frac{I_{CM,BBI}}{I_{CM,B-VSI}} \approx \frac{V_{in} f_{sw,CM}}{\sqrt{3} V_{om} f_{sw}} = \frac{2}{\sqrt{3} M} \frac{f_{sw,CM}}{f_{sw}} \tag{15}$$

Therefore, it is concluded that the high-frequency leakage current generated by the BBI is always smaller than that with the B-VSI. The reduction is more significant when the output voltage, i.e., the overall modulation index M, is high.

3.2. THD of the Output Current

Figure 5 illustrates the characteristic waveforms of phase A of the BBI, specifically, the phase module output voltage v_{an}, the load neutral voltage v_{on} with respect to the negative dc rail, the load phase voltage $v_{ao} = v_{an} - v_{on}$, and the load phase current i_a. Note that these waveforms follow the same pulse pattern during the buck mode.

During the boost mode, the load ripple current is negligible thanks to the inherent filtering effect of the dc-link capacitors. During the buck mode—for instance, $\theta \in \left[\theta_0, \frac{2\pi}{3}\right]$—the characteristic of the load ripple current is the same as that of the inductor current in a buck converter. As the magnitude of the pulsating component of the CM voltage is $V_{in}/3$, the magnitude of the pulsating voltage across the load inductance L_M is, therefore, equal to $2V_{in}/3$. The peak-to-peak ripple in the load current can be expressed as

$$\Delta i(\theta) = \Delta I_n d_2(\theta)(1 - d_2(\theta)),\ \theta \in \left[\theta_0, \frac{2\pi}{3}\right] \tag{16}$$

$$\Delta I_n = \frac{2V_{in}}{3L_M f_{sw}} \tag{17}$$

Due to symmetry, the RMS ripple current over a fundamental cycle can be calculated as

$$\Delta I_{rms} = \sqrt{\frac{1}{\pi} \int_0^{\pi} \Delta i_{rms}^2(\theta) \mathrm{d}\theta} \tag{18}$$

where $\Delta i_{rms}^2(\theta)$ is the local RMS of the ripple current and, during the phase interval of $\theta \in \left[\theta_0, \frac{2\pi}{3}\right]$, it can be expressed as

$$\Delta i_{rms}^2(\theta) = \frac{\Delta i^2(\theta)}{12},\ \theta \in \left[\theta_0, \frac{2\pi}{3}\right] \tag{19}$$

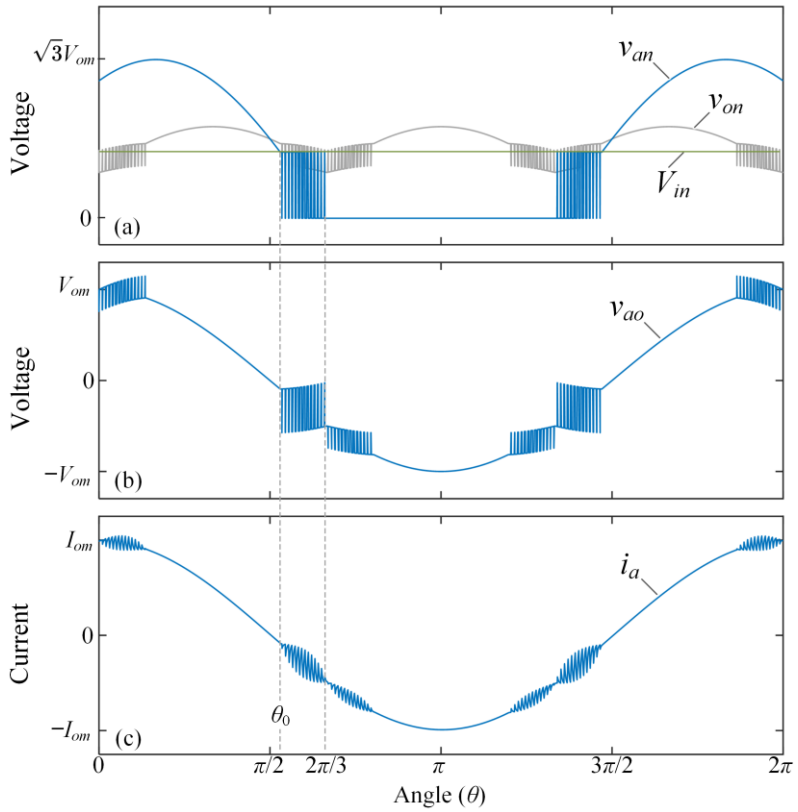

Figure 5. The characteristic waveforms of (**a**) the module output voltage v_{an}, load neutral voltage v_{on}, (**b**) the phase voltage v_{ao}, and (**c**) current i_a of the load.

Due to symmetry of the three-phase waveforms and the characteristic of the CM voltage, the magnitude of the load inductance voltage over the phase intervals $\theta \in \left[0, \frac{2\pi}{3} - \theta_0\right]$ and $\theta \in \left[\frac{2\pi}{3}, \frac{4\pi}{3} - \theta_0\right]$ is equal to half of that during $\theta \in \left[\theta_0, \frac{2\pi}{3}\right]$. Therefore, the RMS ripple current can be expressed as

$$\Delta I_{rms} = \sqrt{\frac{1}{\pi}\int_{\theta_0}^{\frac{2\pi}{3}} \Delta i_{rms}^2(\theta) \cdot \left[2\left(\frac{1}{2}\right)^2 + 1\right] \mathrm{d}\theta} \tag{20}$$

Substituting Equations (16), (17), and (19) into (20), we have

$$\Delta I_{rms} = \frac{\Delta I_n}{\sqrt{8\pi}} \sqrt{\int_{\theta_0}^{\frac{2\pi}{3}} [d_2(\theta)(1 - d_2(\theta))]^2 \mathrm{d}\theta} \tag{21}$$

The exact closed-form expression for the RMS ripple current is unfeasible due to the form of transcendental equations in the solution of the integration in (21). However, it can be numerically calculated to guide the selection of the switch devices. Nonetheless, the duty ratio d_2 can be approximated by a linear relationship with θ, i.e.,

$$d_2(\theta) \approx \frac{\theta - \theta_0}{\frac{2\pi}{3} - \theta_0}, \ \theta \in \left[\theta_0, \frac{2\pi}{3}\right] \tag{22}$$

An approximate closed-form expression of ΔI_{rms} can be obtained by substituting Equation (22) into (21), and with some simplification, i.e.,

$$\Delta I_{rms} \approx \frac{\Delta I_n}{\sqrt{8\pi}} \sqrt{\frac{\frac{2\pi}{3} - \theta_0}{30}} \tag{23}$$

Substituting Equations (6) and (17) into (23), an expanded expression can be obtained as

$$\Delta I_{rms} \approx \frac{V_{in}}{6\sqrt{15\pi}L_M f_{sw}} \sqrt{\frac{\pi}{2} - \operatorname{acos}\left(\frac{2}{\sqrt{3}M}\right)} \tag{24}$$

The THD of the load current can then be calculated as

$$THD_i = \frac{\Delta I_{rms}}{I_{rms,1}} \tag{25}$$

where $I_{rms,1}$ is the fundamental RMS current. It can be concluded from Equation (24) that the THD_i of the BBI will decrease as the overall modulation index M increases. This is because a higher M means a higher output voltage, which, in turn, means a wider duration of the boost operation mode of the BBI, and the inherent filtering effect becomes more significant.

It is noted that the derived expressions apply in the modulation index range of $M > 4/3$, in which the phase-module switches between two modes only once during a half cycle. In the modulation index range of $M \in \left(0,\ 2/\sqrt{3}\right]$, the boost switch leg is always clamped, and the BBI works the same way as the conventional three-phase two-level inverter, of which the THDi expression has been derived in the literature. In the modulation index range of $M \in \left(2/\sqrt{3},\ 4/3\right]$, the phase-module switches between the two modes more than once during a half cycle. However, the derived expressions can still be applied as an approximation, as the modulation index is within a narrow band close to 4/3.

3.3. Phase Swapping Interleaving Method

The fundamental cycle can be divided into three sections, i.e., Section I: $\theta \in (0,\ 2\pi/3]$; Section II: $\theta \in (2\pi/3,\ 4\pi/3]$; Section III: $\theta \in (4\pi/3,\ 2\pi]$. During each of these sections, only two out of the three phase modules are actively operating, while the third one is in clamping mode. Specifically, in Section I, phases A and B are operating and phase C is clamped. In Section II, phases B and C are operating and phase A is clamped. In Section III, phases C and A are operating and phase B is clamped. Based on this pattern, a phase swapping interleaving method for the boost switch-legs is designed so that the input inductor ripple current of the active phase modules is out of phase and the ripple of the total input current can be reduced.

Let Carrier_P and Carrier_N denote two triangular carrier signals of the switching frequency and opposite phase, respectively. Let Carrier_A, Carrier_B, and Carrier_C denote the triangular carrier signals for the boost switch-legs of phases A, B and C, respectively. The phase swapping-interleaving method is implemented by the following pseudo-code.

```
switch(Section) {
    case I:
    Carrier_A = Carrier_P;
    Carrier_B = Carrier_N;
    Carrier_C = Carrier_N;
    break;
    case II:
    Carrier_A = Carrier_N;
    Carrier_B = Carrier_P;
    Carrier_C = Carrier_N;
    break;
    case III:
    Carrier_A = Carrier_N;
    Carrier_B = Carrier_N;
    Carrier_C = Carrier_P;
    break;
}
```

Carrier_A, Carrier_B, and Carrier_C are then used together with the corresponding control signals to generate the control pulses for the boost switch-legs.

4. Simulation Evaluation

The performance of the BBI is simulated in PLECS and compared against the B-VSI. The two topologies are based on the circuit configuration shown in Figure 1b. The B-VSI is implemented by connecting the positive rails of the three modules so that the three boost legs are operating in parallel. The circuit parameters of the simulated inverter are the same as the scaled-down 10 kW hardware prototype and is shown in Table 1. The BBI is controlled with DPWM while the B-VSI is controlled with conventional SVPWM. The load motor is represented by series-connected resistors and inductors, which do not influence the evaluation of the inverter.

Table 1. Parameters of the prototype inverter.

Parameter	Value
Nominal power (kW)	10
Input DC voltage (V)	200
Output voltage, L-L RMS (V)	400
Input filter inductance (uH)	240
DC bus Capacitance (uF)	12
Switching frequency (kHz)	50
Load inductance (mH)	0.5

Figure 6 shows the characteristic voltage and current waveforms of the two topologies under the same operating condition. The corresponding overall modulation index is $M = 3.46$. The output voltages of the phase modules of the BBI demonstrate its two operating modes during a fundamental cycle. For instance, v_{an} is a pulse-width-modulated voltage when the commanded value is lower than the input voltage (buck mode), and it is a filtered smooth waveform when the commanded value is higher than the input voltage (boost mode). The resulting line-to-line voltage is a partially filtered waveform with drastically lower high-frequency harmonics than that with the B-VSI. The total harmonic distortion of the output current (THDi) obtained by the BBI is only 0.85%, 5.2 times lower than the THDi value of 4.40% with the B-VSI.

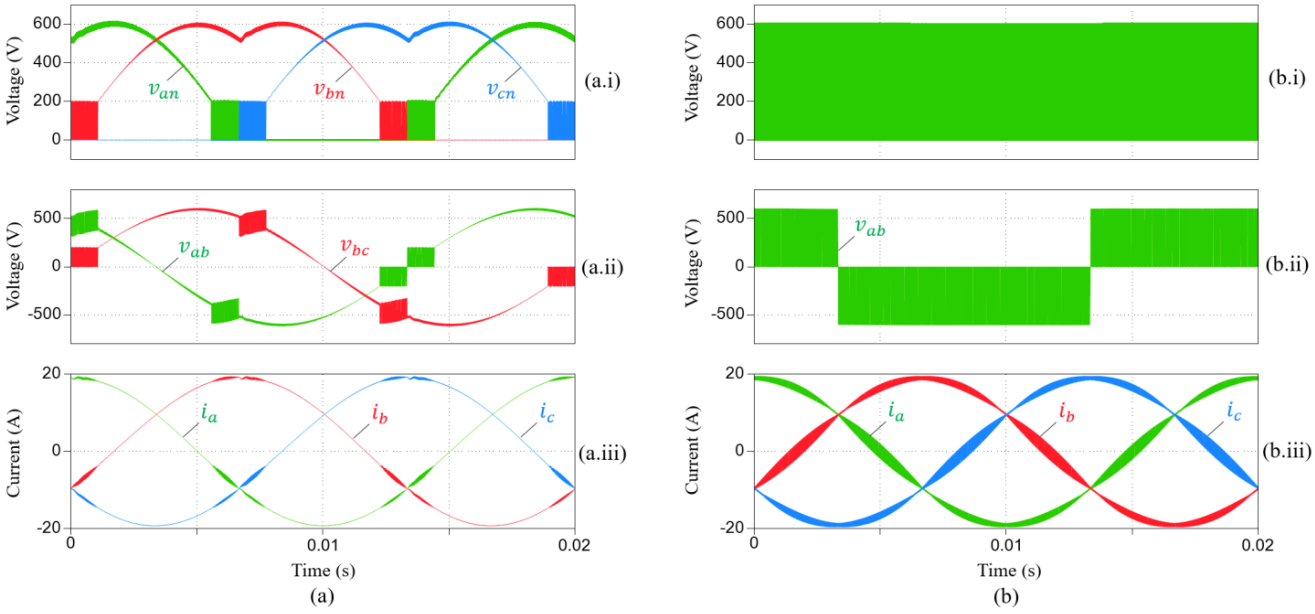

Figure 6. Simulated output voltage and current waveforms of the (**a**) BBI and (**b**) B-VSI. (**a.i**,**b.i**) Phase voltages, (**a.ii**,**b.ii**) phase-to-phase voltages, and (**a.iii**,**b.iii**) output currents.

Figure 7 shows a direct comparison of the ripple component in the current waveforms of the two topologies. With the inherent filter characteristic, the current waveform with the BBI is smooth during most of the fundamental cycle and the peak ripple current is only 0.6 A (3.1% of the fundamental component). In comparison, high-frequency ripple current is present throughout the fundamental cycle with the B-VSI with a peak value of 2.0 A (10.2% of the fundamental component).

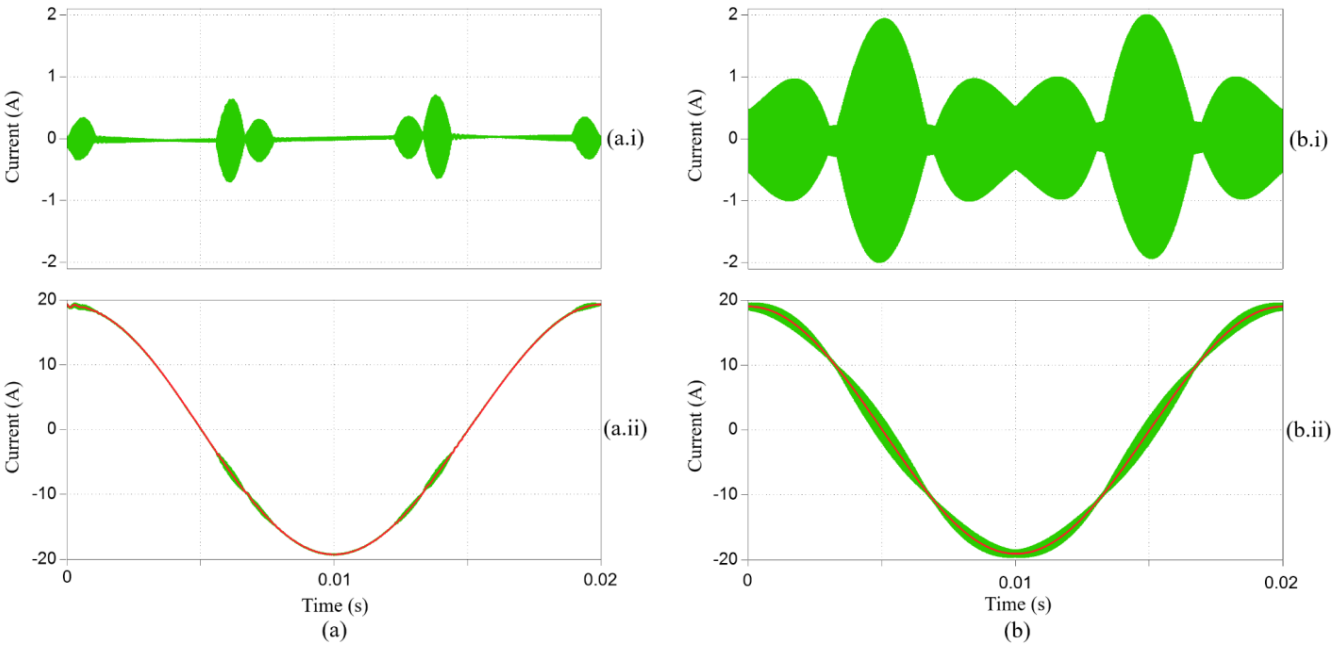

Figure 7. Simulated ripple characteristics of the output current of the (**a**) BBI and (**b**) B-VSI. (**a.i**,**b.i**) Ripple component of the output current and (**a.ii**,**b.ii**) instantaneous (green) and averaged (red) waveform of the output current.

Figure 8 shows the comparison of the THD of the output current of the two topologies at different overall modulation indexes M. When $M \leq 2/\sqrt{3}$, i.e., the peak value of the output line-to-line voltage V_{llm} is not greater than the input voltage V_{in}, the boost switch-legs are bypassed. The BBI is the same as the B-VSI, and both of them work as the regular three-phase two-level inverter. Their THDi levels are the same. When $M > 2/\sqrt{3}$, i.e., the peak value of the output line-to-line voltage V_{llm} is greater than the input voltage V_{in}, the boost switch-legs are actively operating. For the B-VSI, the dc-link voltage is boosted from the input voltage, and the inverter stage is always operating at the maximum modulation index of SVPWM. The THDi level increases linearly with the overall modulation index. For the BBI, a higher M means longer durations of the boost operation mode and shorter durations of the buck mode, hence longer durations of the filtered smooth current waveform, i.e., lower THDi. The simulated THDi of the BBI matches very well with the analytically derived results based on Equation (21).

Figure 9 shows the output CM voltage and the resulting CM current of the BBI and B-VSI. The CM impedance is represented by a 2 nF capacitor to mimic the parasitic capacitance between the winding and the frame of a motor. Due to the inherent filtering effect of the BBI topology, the high-frequency component of the CM voltage is significantly reduced.

Figure 10 shows the zoomed-in details of the CM voltage and CM current waveforms of the BBI and B-VSI topologies. With the BBI topology, not only is the number of CM voltage level jumps during a switching period 3 times less, but the magnitude of the CM voltage level jumps is also significantly lower. Hence, the resulting CM current is significantly lower with the BBI topology. The CM current with the BBI topology is 72 mA RMS, while it is 656 mA RMS (8.7 times higher) with the B-VSI topology. It should be noted that the simulated CM current result only serves to evaluate the relative performance of the

two topologies. As the CM current depends on other parasitic parameters of the inverter system, which is not accurately modeled in the simulation, actual values of the CM current in the hardware test could be different in the experimental tests. However, the CM current with the BBI will be much lower than that with the B-VSI.

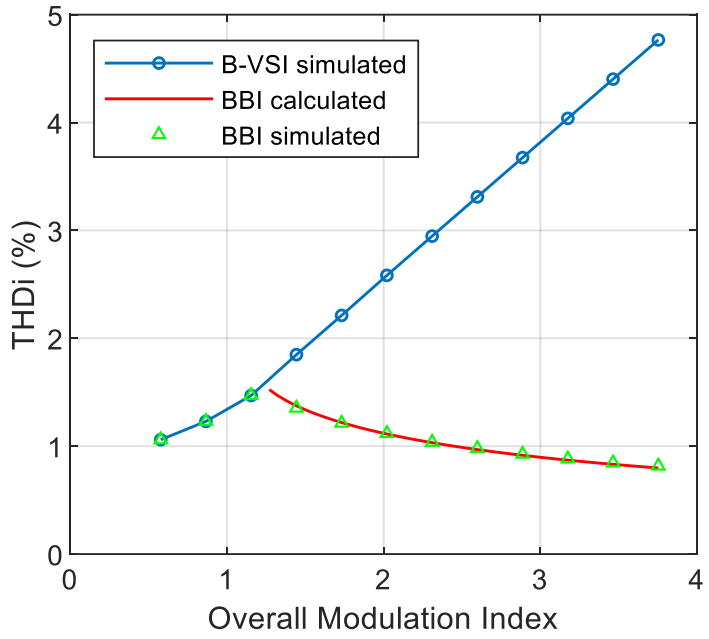

Figure 8. THD of the output current of the two topologies at different overall modulation indexes.

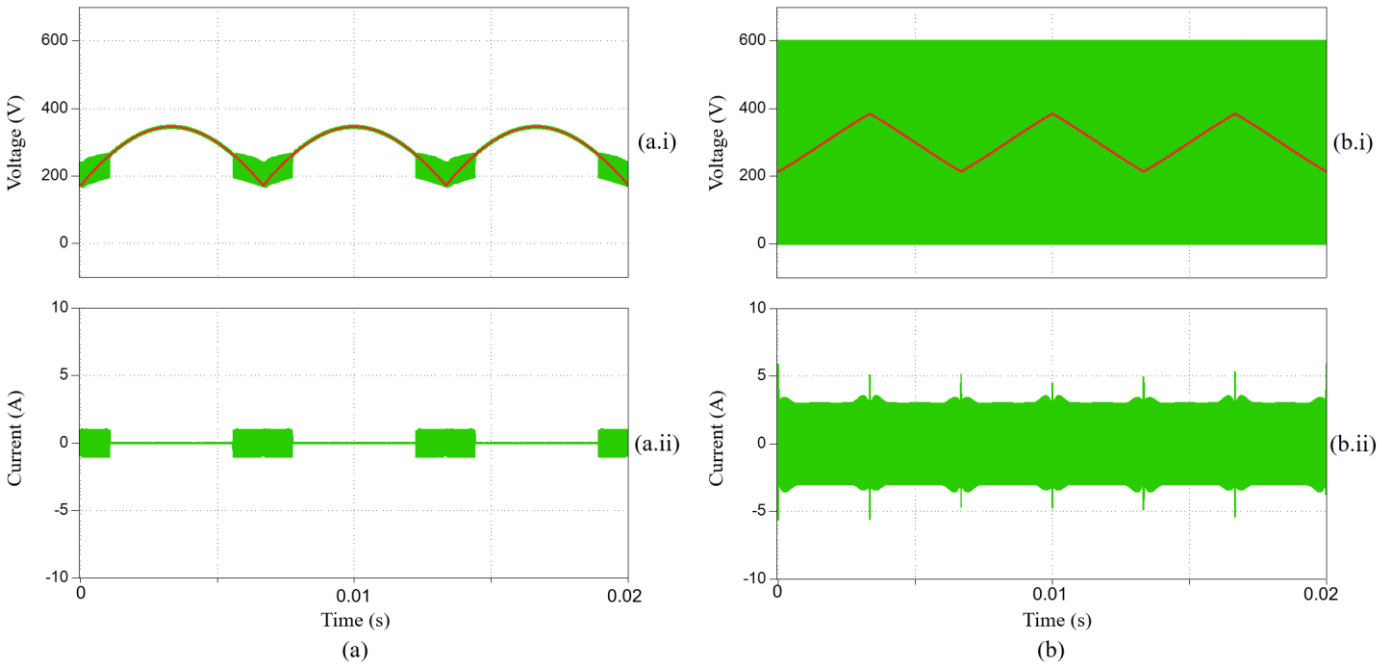

Figure 9. Simulated output CM voltage and current of the (**a**) BBI and (**b**) B-VSI. (**a.i**,**b.i**) Instantaneous (green) and averaged (red) waveform of the CM voltage and (**a.ii**,**b.ii**) CM current.

Figure 11 shows the ripple of the sum of the three input inductor currents without and with the phase swapping interleaving method. With interleaving, the peak-to-peak ripple is reduced from 24.1 A to 13.2 A, and the ripple RMS is reduced from 5.6 A to 2.6 A. The significant reduction in the ripple current means much less filtering effort at the input side.

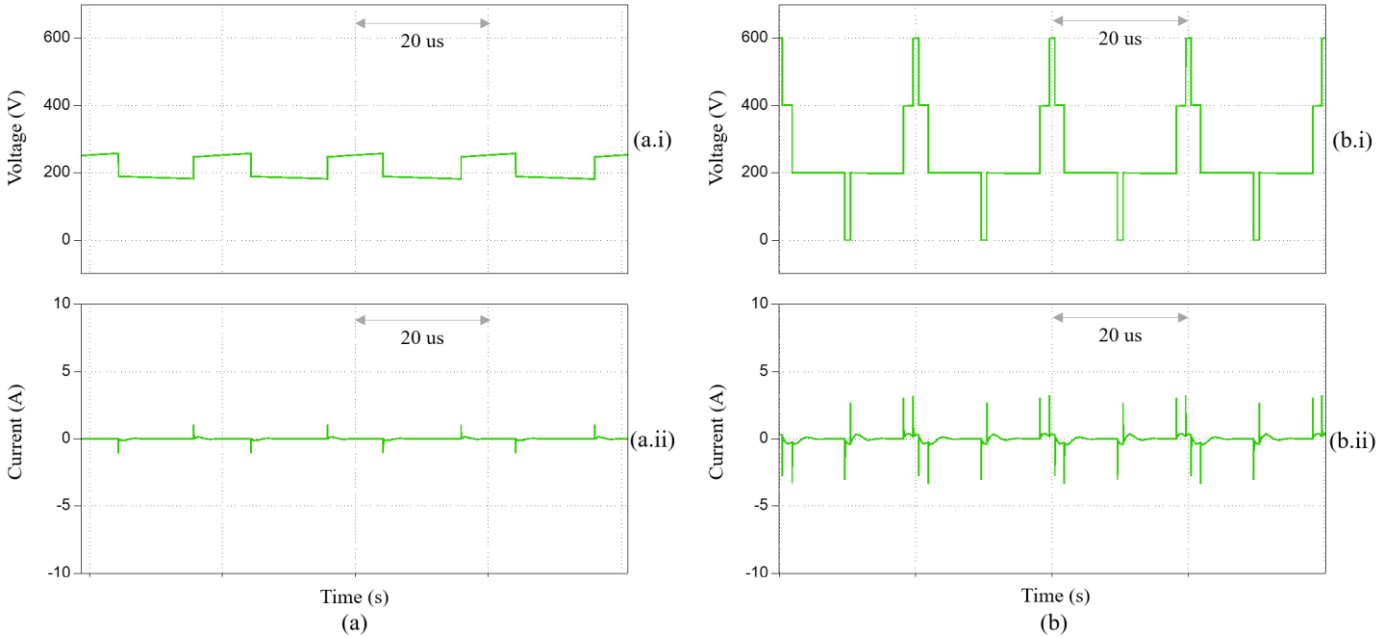

Figure 10. Zoomed-in detail of the CM voltage and current waveforms. (**a**) BBI and (**b**) B-VSI. (**a.i**,**b.i**) CM voltage and (**a.ii**,**b.ii**) CM current.

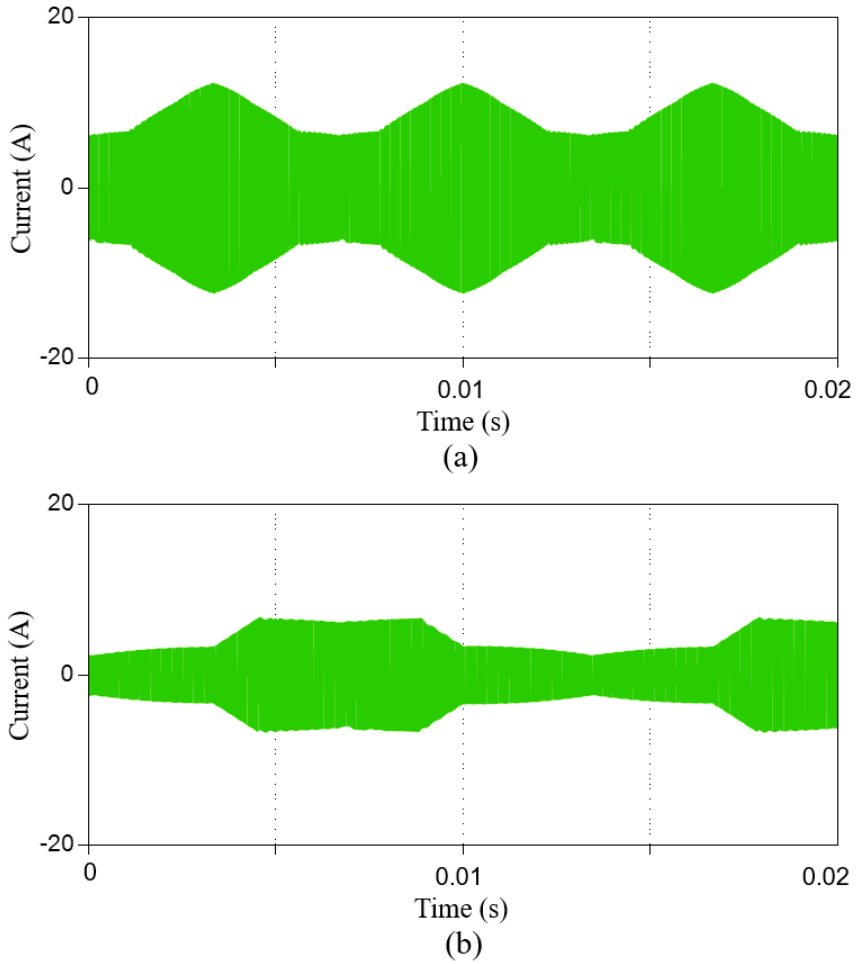

Figure 11. Simulated waveforms of the ripple of the three summed input inductor currents (**a**) without and (**b**) with the phase swapping interleaving method.

Figure 12 shows the waveforms of the voltages across the main switch devices of the two topologies. The switch devices of the B-VSI are switched consistently at the constant dc-link voltage, 600 V in this case. On the contrary, the voltage stresses of the switch devices of the BBI are much lower. For instance, the switched voltage of the boost leg varies between the input voltage (200 V) and the maximum dc-link voltage (600 V). The top switch of the buck leg is switched at the much lower input voltage (200 V), while the bottom switch voltage stress varies between the input voltage and the maximum dc-link voltage. The voltage stress characteristics of the BBI is advantageous in terms of switching losses and the lifetime of the semiconductor devices.

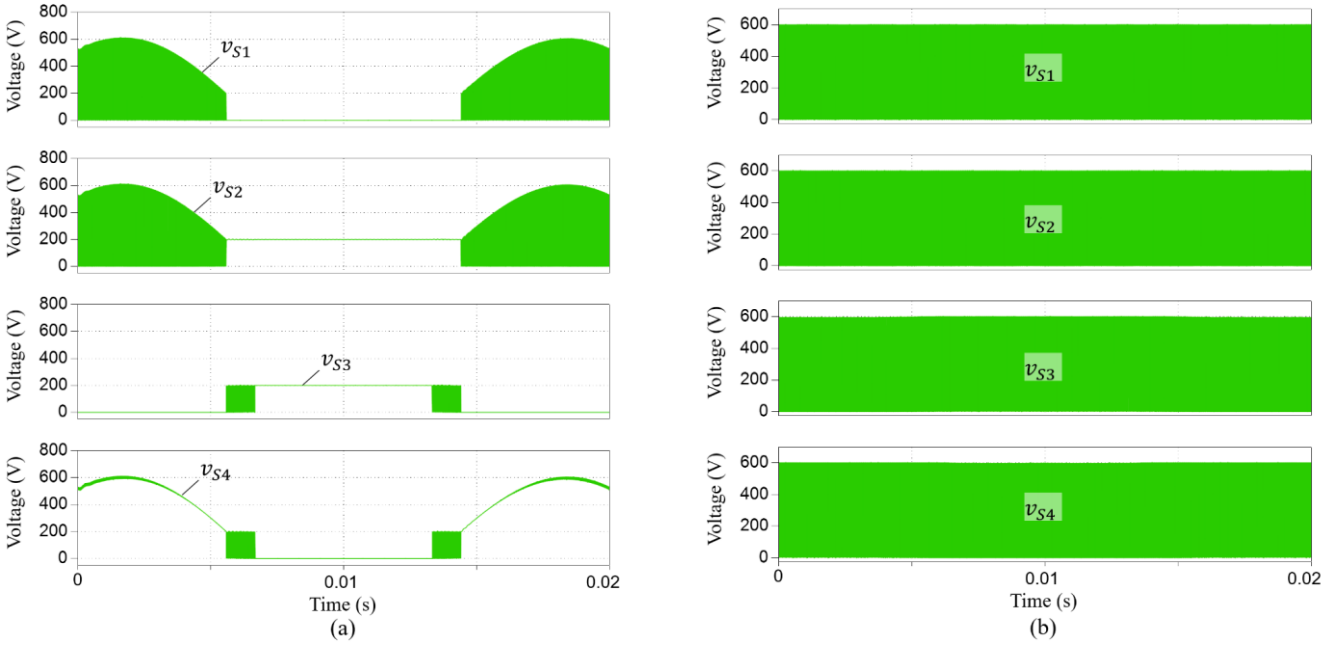

Figure 12. Voltage across the switch devices in a phase module. (**a**) BBI and (**b**) B-VSI.

5. Experimental Results

A scaled-down hardware prototype is designed based on SiC MOSFETs, with a nominal power of 10 kW. SiC devices have been adopted in commercial EV traction inverters. SiC MOSFETs with parameters of 1200 V/40 mΩ are used in the prototype to represent the state-of-the-art technology. The performance of the BBI is validated with the prototype, and it is compared with the B-VSI topology with the same parameters and operating conditions. The parameters of the hardware prototype are shown in Table 1.

Thanks to the modular structure of the BBI, the hardware design can be simplified. The same boost-buck converter module design is reused for the three phase modules. The same hardware can be easily reconfigured as a B-VSI with three paralleled switch legs as the boost stage. The load is configured as a three-phase series-connected resistor-inductor branch to mimic a motor. This does not affect the efficiency and THD performance evaluation of the inverter.

Figure 13 shows the waveforms of the output phase voltage, phase-to-phase voltage, and output currents of the BBI. The waveform of the output phase voltages, referenced to the negative dc bus, conforms with the analysis in Section 2. When the reference voltage is higher than the input voltage, the phase module generates a smooth voltage waveform filtered by the dc bus capacitor. When the reference voltage is lower than the input voltage, the phase module generates a pulse-width-modulated voltage waveform with a magnitude equal to the input voltage. The phase-to-phase voltage is smooth during most of the fundamental cycle and only presents a ripple with a magnitude equal to the input voltage when any of the phase modules operates in buck mode.

Figure 14 shows the waveforms of the output phase voltage, phase-to-phase voltage, and output currents of the B-VSI employing SVPWM. The switch legs are constantly switching during the fundamental cycle. The phase-to-phase voltage is rich in high-frequency harmonics.

The harmonic content of the output current is then evaluated. The current waveform data measured by high-bandwidth current probes are computed in MATLAB to obtain the THDi value. The sampling frequency is 10 MHz and the maximum frequency for THDi calculation is 1 MHz. The THDi value with the BBI topology is 1.74%. It is slightly higher than the analytically calculated value due to nonideal factors in the hardware such as dead band time in the gate drive signals and device voltage drop. The THDi value with the BBI topology is 12.52%. It is much higher than the analytically calculated value mostly due to the high-frequency harmonics induced by the switching transients. As predicted by the theoretical analysis, the THDi with the BBI is much lower than that with the B-VSI. The low THDi with the BBI is mainly due to the inherent filtering effect of the dc-link capacitors even with drastically reduced switching actions.

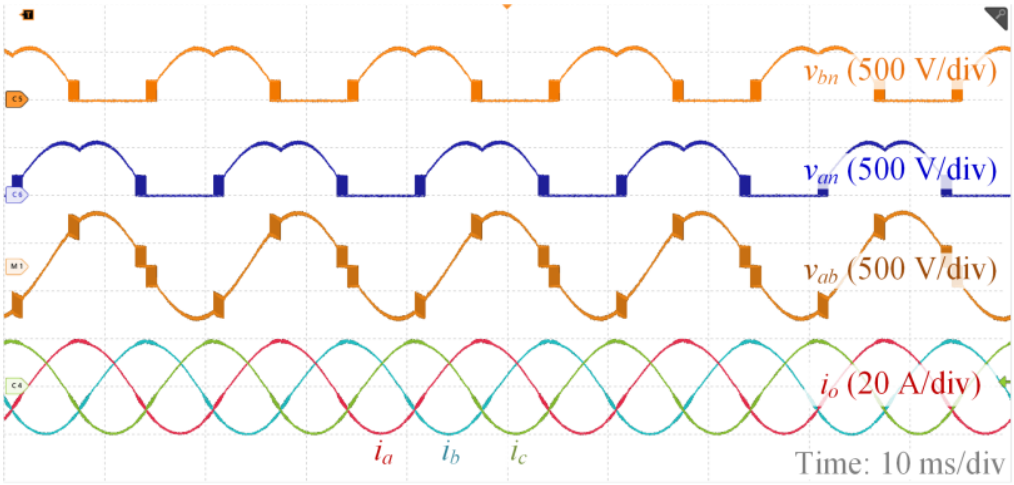

Figure 13. Experimental waveforms of the output phase voltages (v_{an} and v_{bn}), phase-to-phase voltage v_{ab}, and three-phase currents (i_a, i_b, and i_c) of the BBI.

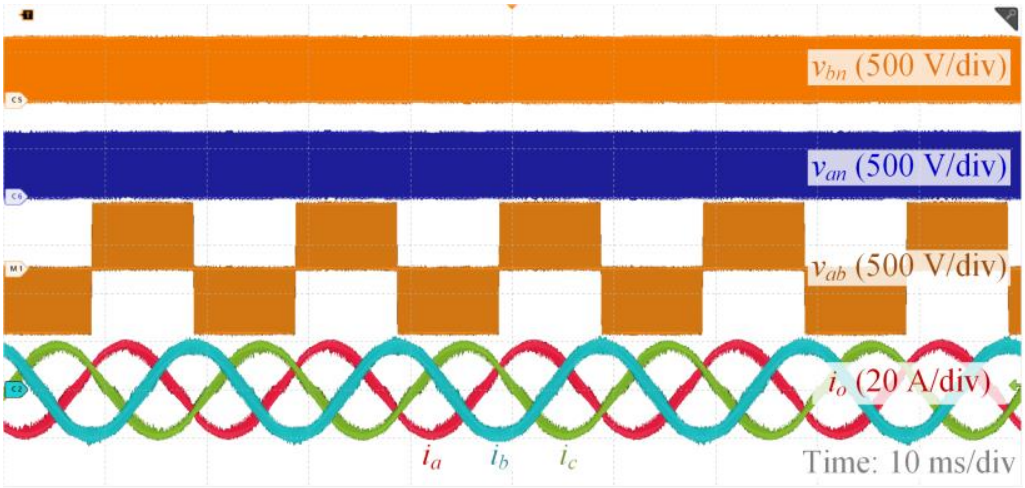

Figure 14. Experimental waveforms of the output phase voltages (v_{an} and v_{bn}), phase-to-phase voltage v_{ab}, and three-phase currents (i_a, i_b, and i_c) of the B-VSI.

As the switches of the B-VSI are constantly switched at a higher voltage and with high frequency, the efficiency of the B-VSI is relatively low. It is measured to be 96.8% at 10 kW. The total losses are calculated to be 322 W. For the BBI, the switch legs are clamped

for 1/3 of a fundamental cycle where they generate no switching losses. When they are switching, they switch at the lower capacitor voltage of the phase modules. Therefore, the BBI has a higher efficiency. It is measured to be 97.7% at 10 kW, 0.9% higher than that of the B-VSI. The total loss is calculated to be 230 W, 28% lower than that of the B-VSI.

Figure 15 shows the measured data of the CM voltage and current of the two topologies. The experimental result matches with the analysis and simulation result. The RMS of the CM current with the BBI is 86 mA while it is 776 mA (9 times higher) with the B-VSI. This is also due to the inherent filtering effect, lower switched voltage, and much lower number of switching actions of the BBI.

The comparison of performance of the BBI and B-VSI is shown in Table 2. It is validated that the BBI topology has a higher efficiency, drastically lower THDi, and lower CM current.

Table 2. Performance Comparison of the Two Topologies at Rated Condition.

Topology	Efficiency	THDi	CM Current RMS
BBI	97.7%	1.74%	86 mA
B-VSI	96.8%	12.52%	776 mA

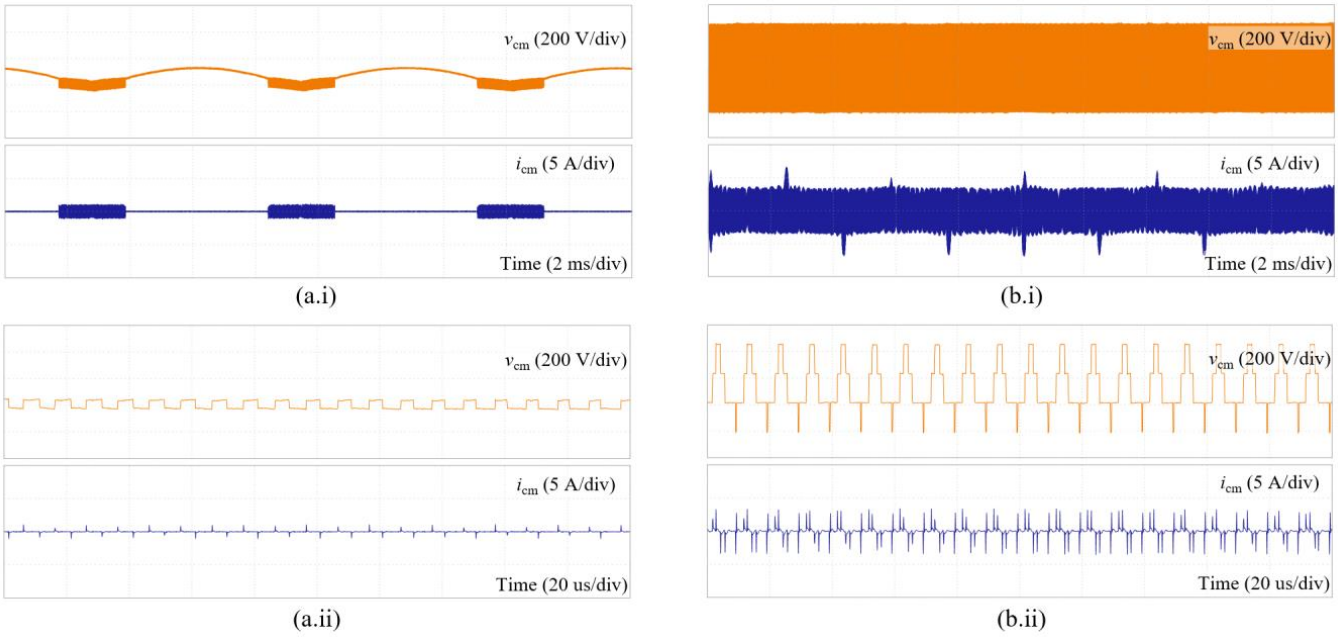

Figure 15. Measured waveforms of the CM voltage and current of (**a**) BBI and (**b**) B-VSI. (**a.i**,**b.i**) Waveform over a fundamental cycle. (**a.ii**,**b.ii**) Zoomed-in detail of the waveforms.

Figure 16 shows the effect of the phase swapping interleaving method for the BBI. The interleaved phases are phases A and B during $\theta \in \left(0, \frac{2\pi}{3}\right]$, phases B and C during $\theta \in \left(\frac{2\pi}{3}, \frac{4\pi}{3}\right]$, and phases C and A during $\theta \in \left(\frac{4\pi}{3}, 2\pi\right]$. It is seen from the zoomed-in waveforms that the ripple currents of the interleaved phases have similar peak-to-peak values and opposite phases, so the ripple of the sum of the three input inductor currents is significantly reduced. The RMS ripple of the input current is reduced from 3.3 A to 2.4 A.

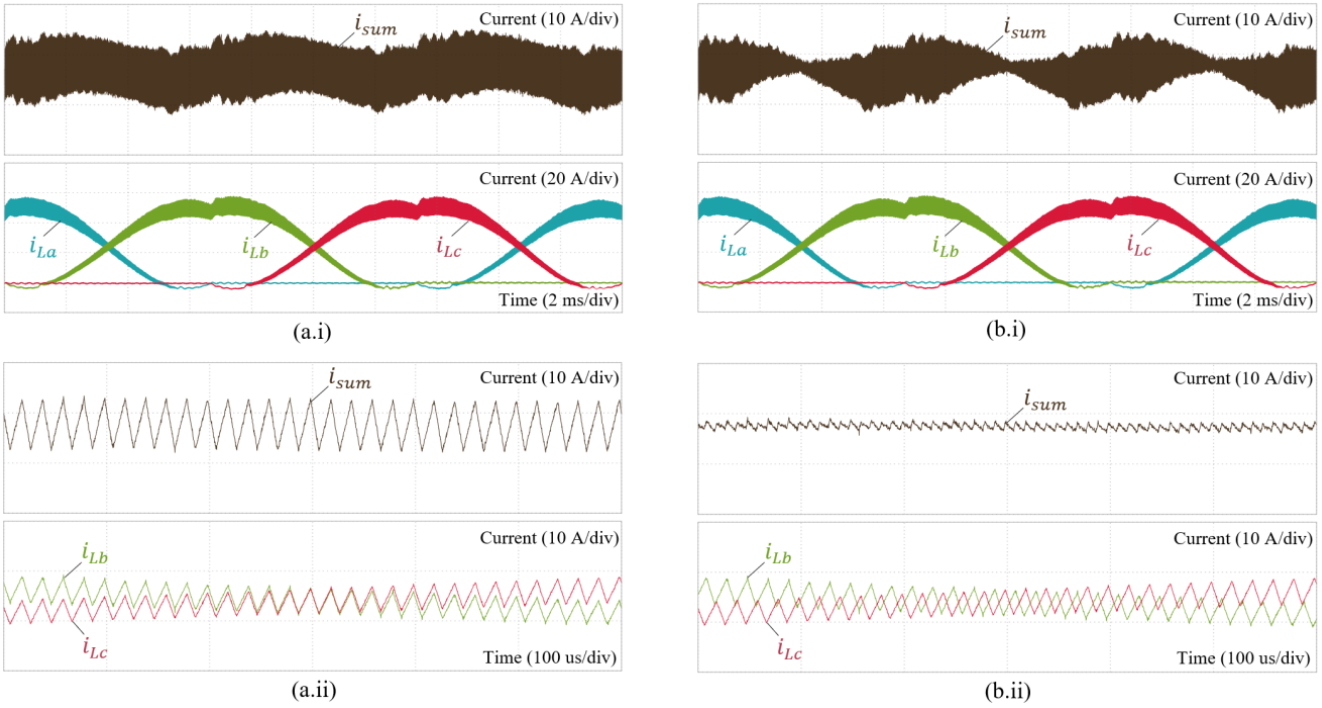

Figure 16. Measured waveforms of the input inductor currents (i_{La}, i_{Lb}, i_{Lc}, $i_{sum} = i_{La} + i_{Lb} + i_{Lc}$) of the BBI. (**a**) Without interleaving. (**b**) With interleaving. (**a.i**,**b.i**) Waveforms over a fundamental cycle. (**a.ii**,**b.ii**) Zoomed-in detail of the waveforms.

6. Conclusions

A comprehensive analysis of the CM voltage and current, and the THD of the output current is presented for the modular three-phase BBI. Analytical expressions are derived for the THD and the reduction ratio of the CM current compared to the conventional topology. A phase swapping interleaving method is designed to reduce the ripple of the input current.

The theoretical analyses are verified by extensive simulation and experimental results. It is validated that the BBI, compared to the conventional B-VSI, has a higher efficiency, much lower THDi, lower CM current, and lower voltage stress on the switch devices. The reduction in THDi and CM current compared to the conventional topology is more significant in the high-modulation-index range. The analysis and comparative evaluation prove that the BBI is a promising topology for the EV traction inverter.

The BBI has a higher component count compared to the conventional topology. However, the input stages are paralleled, and the full power is spread in the three phase modules. For the B-VSI, although there is only one switch leg for the booster stage, it usually also adopts semiconductor paralleling either at the chip level or at the device level. With a modular structure of the BBI, the same design can be used for the three phase modules so that the engineering effort can also be reduced.

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