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# Admittance Criterion of Medium-Voltage DC Distribution Power System and Corresponding Small Signal Stability Analysis

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**Abstract:** Aiming at the stability of a medium-voltage DC network based on a modular multilevel converter (MMC), this paper proposes an admittance stability criterion considering the influence of current-limiting inductors at the medium voltage side, which prevents the complex products and matrix calculations of traditional criteria. The DC admittance model DC transformers (DCTs) under different working modes are then established based on Thevenin/Norton equivalent circuit methods to analyze the stability of the DC system based on the proposed admittance stability criterion, which proves that the voltage resonance problem at the medium voltage side can be improved by adding active damping control strategies on DCTs also proves the effectiveness of the proposed stability criterion. The time-domain simulation and the hardware-in-loop simulation are then built in PLECS and RT Box to further verify the correctness of the system stability analysis and the effectiveness of the proposed admittance criterion, which provides a theoretical basis and technical reserve for the stable operation of the DC distribution power system.

**Keywords:** modular multilevel converter; DC transformer; admittance stability criterion; DC distribution power system



**Citation:** Yang, J.; Wang, J.; Jin, X.; Li, S.; Xiao, X.; Wu, Z. Admittance Criterion of Medium-Voltage DC Distribution Power System and Corresponding Small Signal Stability Analysis. *World Electr. Veh. J.* **2023**, *14*, 235. <https://doi.org/10.3390/wevj14090235>

Academic Editor: Joeri Van Mierlo

Received: 19 July 2023

Revised: 19 August 2023

Accepted: 22 August 2023

Published: 28 August 2023



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## 1. Introduction

With a high proportion of renewable energy and new DC loads interfaced with the power grid, more and more sources and loads in the new power system show DC characteristics, which can provide flexible access to the distributed power and DC loads and improve the operation of the system [1,2]. The high-voltage DC (HVDC) power grid [3] and low-voltage DC (LVDC) microgrid [4] have been gradually promoted and applied, and at present, scholars are making developments in the field of medium voltage DC (MVDC) power distribution systems [5–7].

However, the converters for the MVDC distribution power system (DPS) are mostly customized by different suppliers, which makes the system have the characteristics of low damping, weak inertia, and complex structure. Therefore, the potential stability problem is one of the major challenges for the development of an MVDC DPS, and an effective and simple small signal stability criterion is desperately needed.

Firstly, small signal stability criteria are mainly focused on the stability of two cascaded converters [8], and some scholars have successively proposed impedance criteria with different stability regions, such as the Gain Margin Phase Margin (GMPM) criterion [9], the Opposing Argument (OA) criterion [10], the Energy Source Analysis Consortium (ESAC) criterion [11], etc. However, these criteria divided converters into load converters and source converters [12]. The admittance criterion for current source converters and the impedance criterion for voltage source converters are not equivalent and cannot be directly applied to the analysis of multiple converters connected to the common bus. On this basis, Sun [13] proposed a general criterion for both voltage-source and current-source converters

for grid-connected converters and unified the admittance and impedance criteria. The criteria above first adopted the Nyquist criterion for impedance stability but only focused on the cascaded converters system; these criteria have clear physical meaning and simple methods but are not applicable to the DC system with multiple converters in parallel.

Zhang [14] then divided the converter into bus voltage-controlled converters (BVCCs) or bus current-controlled converters (BCCCs) and obtained the equivalent impedance ratio of the DC system through the loop analysis. The system stability could then be evaluated through the Nyquist criterion, which realized the stability analysis of multiple converters connected to the common DC bus. Pan et al. [15,16] further extended the BVCC and BCCC concepts to the multi-voltage DC system and carried out loop analysis to obtain the overall stability impedance ratio criterion of the system. According to Zhang et al. [14–16], the converter is regarded as directly connected to the DC bus. But for the MVDC DPS, both the output sides of the voltage source converter (VSC) and the DC transformer (DCT) are equipped with a current-limiting inductor due to the low damping characteristics of the system [17,18], and the inductor impedance and line impedance have a certain impact on the loop analysis of criteria based on the concepts of BVCC and BCCC. Therefore, this type of criteria has great scalability and simplicity but ignores the influence of current-limiting inductors and line impedance and is not applicable to the MVDC DPS.

Therefore, Li [19] developed a stability analysis for the multi-terminal DC power grid composed of four modular multilevel converters (MMCs). The voltage stability of each port is analyzed respectively based on the method of node reduction. This method has clear ideas and high accuracy, but it is more complex for a system with more nodes. He [20] puts forward the node admittance criterion method to evaluate the system stability by calculating the node determinant, but it is difficult to obtain the determinant of the admittance matrix when the impedance expression is complex.

Compared with the criteria above, the proposed admittance criterion takes full consideration of line impedance and current-limiting inductors. This criterion has good scalability and clear physical meaning. The stability can be evaluated by the equivalent admittance ratio through this proposed criterion so the evaluation process is simpler, which prevents the complex product and matrix calculation and is convenient and suitable for the stability evaluation of the MVDC DPS.

In this paper, an admittance stability criterion of the DPS considering the influence of current-limiting inductors is proposed. Then, the DCT admittance models under different working modes are established, which shows the potential instability risk of the MVDC DPS through the proposed criterion. Afterwards, active damping strategies are proposed to improve the phase margin and system stability. Finally, the simulation model of the corresponding DC system is built in PLECS, which proves the accuracy of the stability analysis and the effectiveness of the proposed criterion, and RT Box hardware-in-loop simulation is also used to further verify the correctness of the PLECS simulation.

## 2. Structure of MVDC DPS

The grid structure of the MVDC DPS is shown in Figure 1. The MVDC voltage is  $\pm 10$  kV. Two MMCs are used in this system as the interface with the AC side to provide reliable power supply, and several photovoltaic DCTs (PVDCTs) are interfaced to provide renewable power for the DC system. Other DCTs interfaced in this system include DC charging piles and MVDC to LVDC microgrid DCTs, and they can be treated as the load-type DCT (LTDCT) in this system. The LVDC side of DCT is 750 V.

Among the converters, one MMC adopts DC voltage control and the other MMC adopts power control. The PVDCTs work under the (Maximum Power Point Tracking) MPPT mode, and the LTDCTs work under the DC voltage control mode to control the LVDC side voltage. In Figure 1,  $L_{mmc1}$  is the current-limiting inductor at the output side of the voltage-controlled MMC (VCMC).  $L_{mmc2}$  is the current-limiting inductor at the output side of the power-controlled MMC (PCMMC).  $L_{pvk}$  is the current-limiting inductor at the output side of the  $k$ th PVDCT.  $L_{LTm}$  is the current-limiting inductor at the input

side of the  $m$ th LTDCT. By analogy,  $Z_{line\_mmc1}$ ,  $Z_{line\_mmc1}$ ,  $Z_{line\_pvk}$ ,  $Z_{line\_ltn}$  are the line impedances of the corresponding converters, and  $i_{mmc1}$ ,  $i_{mmc1}$ ,  $i_{pvk}$ ,  $i_{ltn}$  are the currents of the corresponding converters.

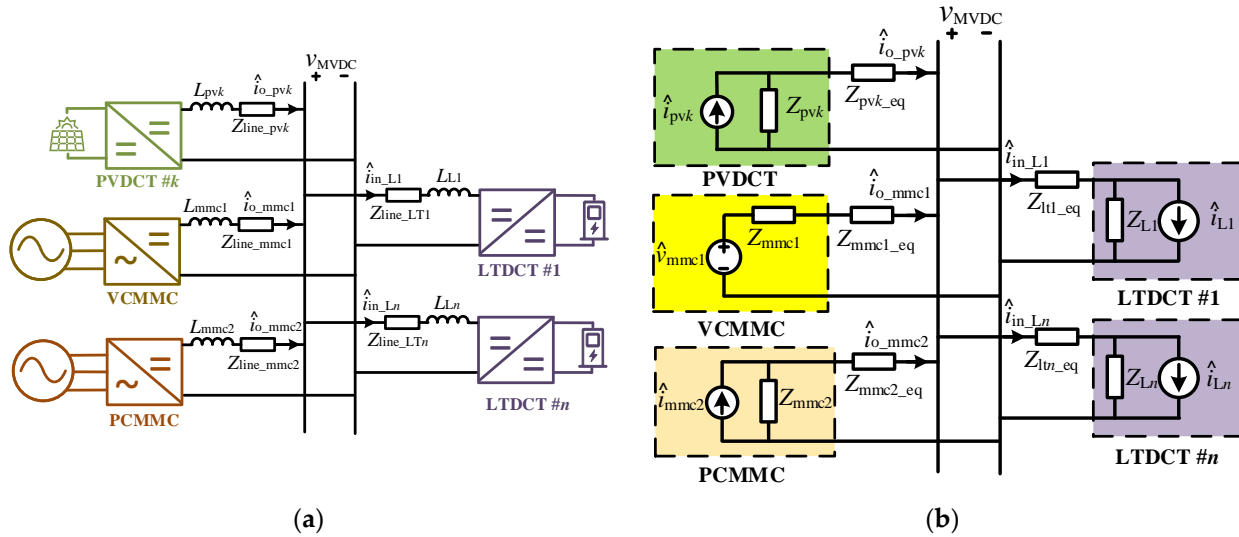


Figure 1. Structure of the MVDC DPS. (a) Topology; (b) Small-signal impedance network.

### 3. Admittance Criterion for MVDC DPS

According to the Thevenin/Norton equivalence theorem, the VMMC controls its output voltage, so it can be equivalent to a voltage source series with the output impedance, which is in the form of Thevenin equivalent circuits. The other converter controls its input/output current, so they are equivalent to the current source resistance parallel with the input/output impedance. The small-signal impedance network of the MVDC DPS is shown in Figure 1b. The equivalent series impedance in Figure 1b is the sum of the inductor and line impedance, which is written as (1). Suppose that the system has  $n$  PVDCs and  $m$  LTDCTs. The input impedance of PCMMC is  $Z_1$ , the output impedance of the 1st to the  $n$ th PVDC is  $Z_2$  to  $Z_{n+1}$ , the input impedance of the 1st to the  $m$ th LTDCT is  $Z_{n+2}$  to  $Z_{m+n+1}$ , the corresponding current source and the equivalent impedance are also numbered according to this law, and the current flowing into the converter is positive. So, the impedance and current of the converters can be expressed as below:

$$\begin{cases} Z_{mmc1\_eq} = sL_{mmc1} + Z_{line\_mmc1} \\ Z_{mmc2\_eq} = sL_{mmc2} + Z_{line\_mmc2} \\ Z_{pvk\_eq} = sL_{pvk} + Z_{line\_pvk} \\ Z_{ltn\_eq} = sL_{ltn} + Z_{line\_ltn} \end{cases} \quad (1)$$

$$\begin{cases} Z_1 = Z_{mmc2}, Z_{L1} = Z_{mmc1\_eq}, i_1 = -i_{mmc2} \\ Z_{i+1} = Z_{pvi}, Z_{Li+1} = Z_{pvi\_eq}, i_{i+1} = -i_{pvi}, i \in [1, n] \\ Z_{j+n+1} = Z_{Lj}, Z_{Lj+n+1} = Z_{Lj\_eq}, i_{j+n+1} = i_{Lj}, j \in [1, m] \end{cases} \quad (2)$$

Then, the output current of the VMMC can be expressed as (4).  $Y'_k$  is the equivalent admittance of the  $k$ th converter considering the effect of current-limiting inductors and line impedance, and  $Z_{out\_k}$  is the impedance of the  $k$ th converter at the MVDC side.

Then, the latter part of  $\hat{i}_{o\_mmc1}$  can be simplified as (5), and  $\hat{i}_{o\_mmc1}$  can be rewritten as (6). At last,  $\hat{v}_{dc\_mmc1}$  can be simplified as (7).

It can be known from Figure 1b that VMMC controls its output voltage, so it is stably loaded by an ideal current source, which means that  $v_{mmc}(s)$  and  $Z'_{mmc}$  are stable. Other converters in this system control their output current, so they are stable loaded by an ideal

voltage source, which means that  $i_k(s)$  and  $Z_k/(Z_{Lk} + Z_k)$  are stable. Then, the stability of the system can be evaluated by applying the Nyquist criterion to  $T_m$  as shown below:

$$T_m = \frac{Y'_{\text{sigma}}}{Y'_{\text{mmc1}}} \quad (3)$$

$$\begin{cases} \hat{i}_{o\_mmc1}(s) = \hat{v}_{mmc1}(s) \cdot \frac{1}{Z'_{mmc1} + \frac{1}{\sum_{k=1}^{m+n+1} Y'_k}} + \sum_{k=1}^{m+n+1} \hat{i}_k(s) \frac{Y_{out\_k}}{Y_{out\_k} + Y_k} \cdot \frac{Y'_{mmc1}}{(Z_{out\_k} - Z_{Lk})} \\ Y'_k = \frac{1}{Z'_k} = \frac{1}{Z_{eqk} + Z_k} = \frac{1}{Z_{Lk} + \frac{1}{Y_k}}, Z_{out\_k} = \frac{1}{\frac{1}{Y_{out\_k}}} = Z_{Lk} + \frac{1}{\sum_{j=1, j \neq k}^{m+n+1} Y'_j + Y'_{mmc1}} \end{cases} \quad (4)$$

$$\begin{aligned} \hat{i}_k(s) \frac{Y_{out\_k}}{Y_{out\_k} + Y_k} \cdot \frac{Y'_{mmc1}}{(Z_{out\_k} - Z_{Lk})} &= \hat{i}_k(s) \frac{Y'_{mmc1}(1 - Z_{Lk} Y_{out\_k})}{Y_{out\_k} + Y_k} \\ &= \hat{i}_k(s) \frac{Y'_{mmc1} [1 + Z_{Lk} (\sum_{j=1, j \neq k}^{m+n+1} Y'_j + Y'_{mmc1})] - Y'_{mmc1} Z_{Lk} (\sum_{j=1, j \neq k}^{m+n+1} Y'_j + Y'_{mmc1})}{\sum_{j=1, j \neq k}^{m+n+1} Y'_j + Y'_{mmc1} + Y_k + Y_k Z_{Lk} (\sum_{j=1, j \neq k}^{m+n+1} Y'_j + Y'_{mmc1})} \\ &= \hat{i}_k(s) \frac{Y'_{mmc1}}{(Y_k Z_{Lk} + 1) (\sum_{j=1}^{m+n+1} Y'_j + Y'_{mmc1}) + Y_k - (Y_k Z_{Lk} + 1) Y'_k} \\ &= \hat{i}_k(s) \frac{Y'_{mmc1}}{(Y_k Z_{Lk} + 1) (\sum_{j=1}^{m+n+1} Y'_j + Y'_{mmc1})} \end{aligned} \quad (5)$$

$$\begin{aligned} \hat{i}_{o\_mmc1}(s) &= \hat{v}_{mmc1}(s) \cdot \frac{Y'_{mmc1} \sum_{k=1}^{m+n+1} Y'_k}{\sum_{k=1}^{m+n+1} Y'_k + Y'_{mmc1}} + \sum_{k=1}^{m+n+1} \hat{i}_k(s) \frac{Y'_{mmc1}}{(Y_k Z_{Lk} + 1) (\sum_{j=1}^{m+n+1} Y'_j + Y'_{mmc1})} \\ &= \frac{1}{1 + \frac{\sum_{k=1}^{m+n+1} Y'_k}{Y'_{mmc1}}} [\hat{v}_{mmc1}(s) \sum_{k=1}^{m+n+1} Y'_k + \sum_{k=1}^{m+n+1} \hat{i}_k(s) \frac{Z_k}{Z_{Lk} + Z_k}] \end{aligned} \quad (6)$$

$$\hat{v}_{dc}(s) = \hat{v}_{mmc}(s) - \frac{i_{o\_mmc1}(s)}{Y'_{mmc1}} = \frac{1}{1 + \frac{Y'_{\text{sigma}}}{Y'_{mmc1}}} \cdot [\hat{v}_{mmc}(s) - \sum_{k=1}^{m+n+1} \hat{i}_k(s) \frac{Z_k}{Z_{Lk} + Z_k} Z'_{mmc1}] \quad (7)$$

#### 4. DC Impedance Modelling of System Converters

The topologies of the converters in this system are shown in Figure 2. The topology of MMC is shown in Figure 2a;  $v_{ga}$ ,  $v_{gb}$ , and  $v_{gc}$  are the AC voltages of MMC, and  $v_{dc}$  is the DC voltage of MMC. Each arm of MMC contains K series sub-modules (SMs) and an arm inductor. In Figure 2,  $i_{au}$  is the current of the upper arm in phase a, and  $i_{al}$  is the current of the lower arm in phase A, and so on.

Due to the voltage restrictions of semiconductor devices, the input-series output-parallel (ISOP) topology is adopted for the DCT, and dual active bridge (DAB) topology is selected as the submodule of the DCT. For the LTDCT,  $v_{in}$  is the input voltage of DCT,  $v_o$  is the output voltage of DCT,  $i_{in}$  is the input current of DCT,  $i_{1k}$  is the input current of the  $k$ th SM,  $i_{2k}$  is the output current of the  $k$ th SM,  $k = 1, 2, \dots, N$ , and  $N$  is the number of SMs.  $Z_L$  is the load impedance, and  $C_o$  is the output capacitance.  $C_{in}$ ,  $L$ ,  $n$  are the input capacitance, transfer inductor, and transformer ratio of the SM, respectively.

For the PVDCT,  $C_b$  is the capacitance of the boost converter, and  $L_b$  is the inductor.  $C_{in\_PV}$  is the capacitance of the DCT at the LVDC side, and  $C_{o\_PV}$  is the capacitance of the DCT at the MVDC side.  $L_{PV}$  is the inductor of each DAB SM, and  $n_{PV}$  is the transform ratio of each DAB SM.

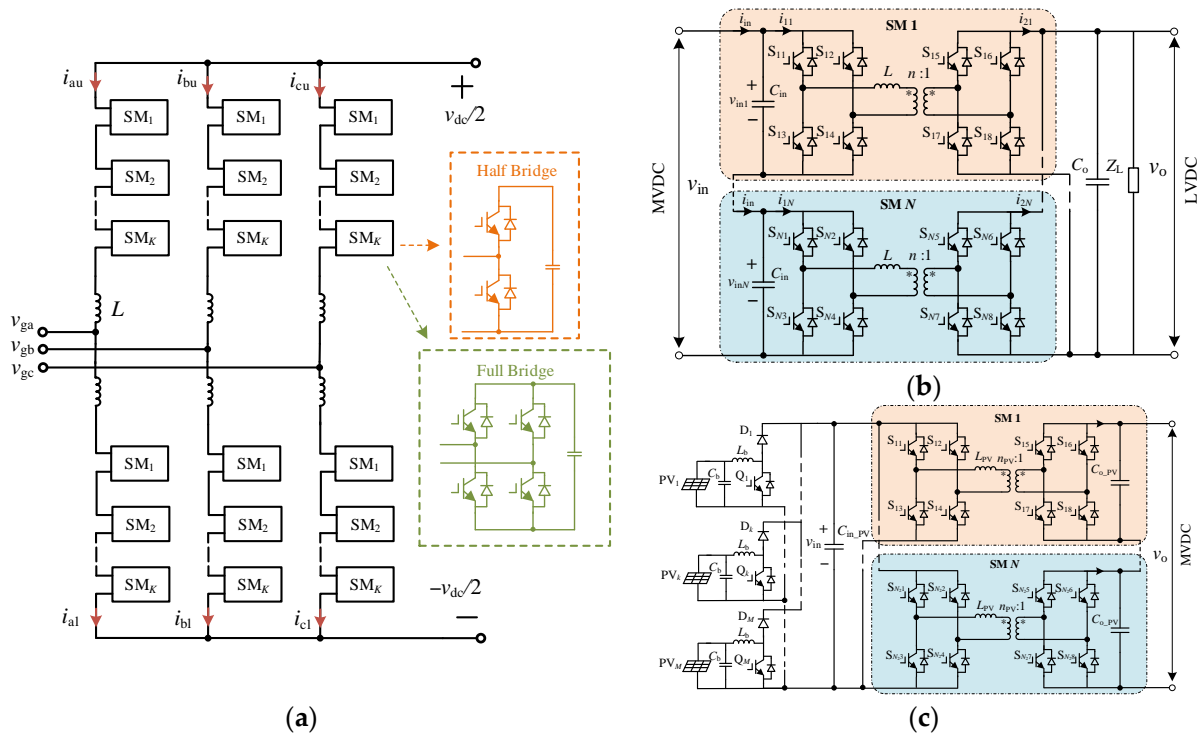


Figure 2. Topology of converters. (a) MMC; (b) LTDCT; (c) PVDCT.

The corresponding control strategies are shown in Figure 3; the circulating current control is adopted at both VMMC and PCMMC. For the LTDCT, it adopts a dual loop control to control its output current and voltage, and the voltage balance control of each module is also implemented. For the PVDCT, the MPPT control is used for boost converters to track the maximum power of PV arrays, and the input voltage control of DAB converters is used to control the voltage of the LVDC system.

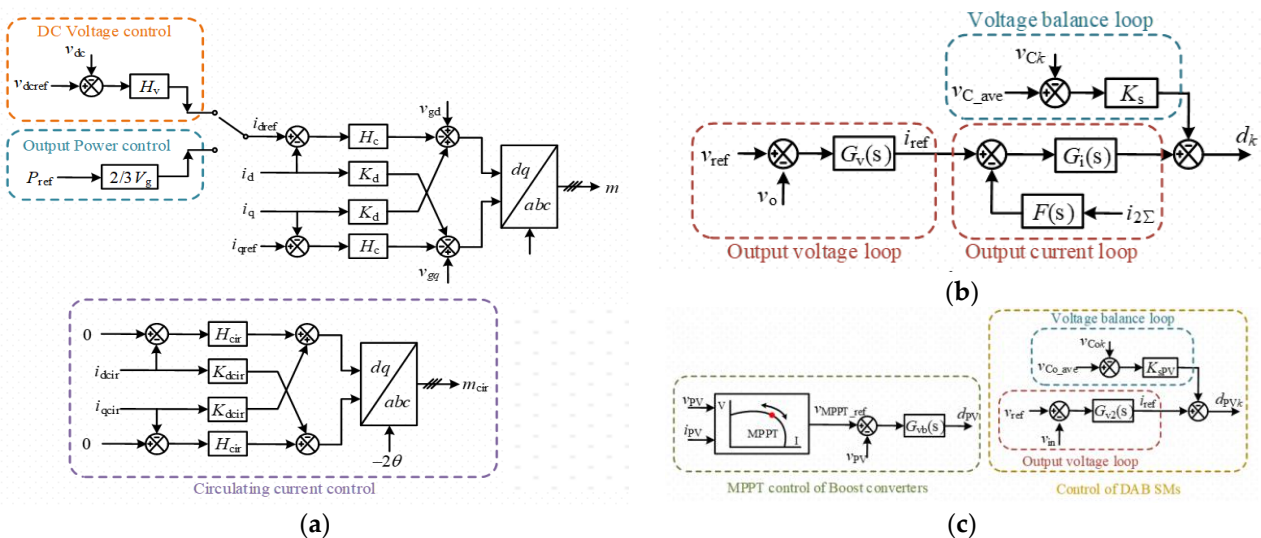


Figure 3. Control strategies of converters (a) MMC; (b) LTDCT; (c) PVDCT.

Li [19] proves that the DC impedance of MMC can be built based on harmonic linearization. To simplify the modeling process, the effect of PLL is ignored, and the specific modeling process is not repeated in this paper.

Zhang et al. [21,22] proves that the voltage balancing control does not affect the impedance characteristics of the ISOP DCT. Thus, the small-signal model of DCTs can be equivalent to a

single module shown as in Figure 4, and the corresponding control diagrams are shown as Figure 5. The parameter with a hat “^” means that it is a small-signal parameter.

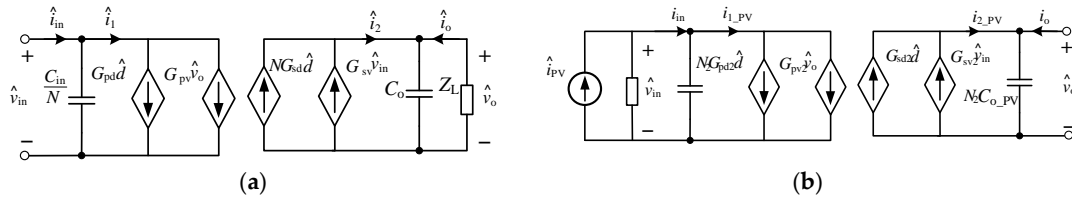


Figure 4. Equivalent small-signal models of DCTs. (a) LTDCT; (b) PVDCT.

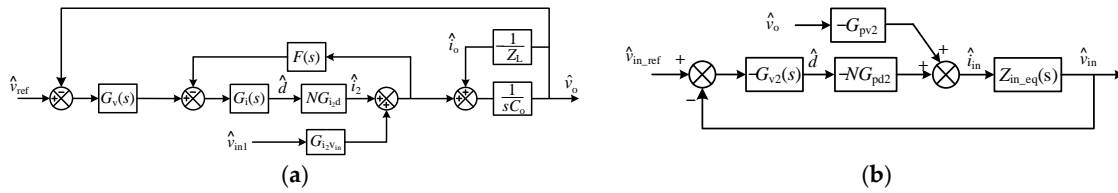


Figure 5. Equivalent control diagrams of DCTs. (a) LTDCT; (b) PVDCT.

In Figure 5, the coefficient terms are derived as (8). For LTDCT,  $f_s$  is the switching frequency of the DAB modules, and  $D$ ,  $V_{in}$ , and  $V_o$  are the phase shift, input voltage, and output voltage of the DAB SM under steady state, respectively. For PVDCT,  $f_{s2}$  is the switching frequency of the DAB SM, and  $D_2$ ,  $V_{in\_PV}$ , and  $V_{o\_PV}$  are the phase shift, input voltage, and output voltage of the DAB SM under steady state, respectively.

$$\begin{cases} G_{pd} = \frac{D(1-D)nV_o}{2f_sL}, G_{sd} = \frac{D(1-D)nV_{in}}{2f_sL} \\ G_{pv} = G_{sv} = \frac{D(1-D)n}{2f_sL} \\ G_{pd2} = \frac{D_2(1-D_2)n_{PV}V_{o\_PV}}{2f_{s2}L_{PV}}, G_{sd2} = \frac{D_2(1-D_2)n_{PV}V_{in\_PV}}{2f_{s2}L_{PV}} \\ G_{pv2} = G_{sv2} = \frac{D_2(1-D_2)n_{PV}}{2f_{s2}L_{PV}} \end{cases} \quad (8)$$

Through Mason’s gain formula, the DC admittance of the DCT can be obtained as (9) and (10).

The corresponding frequency-sweep simulation is established to verify the impedance model. The parameters of LTDCT#1 are listed in Table 1, and the parameters of PVDCT#1 are listed in Table 2. The simulation result in Figure 6 shows that the impedance model is of great accuracy with the simulation result. The LTDCT shows negative input impedance at low frequencies, while the PVDCT shows positive input impedance at low frequencies.

$$Y_{in}(s) = \frac{\hat{v}_{in}}{\hat{i}_{in}} = \frac{-[F(s) + Z_o(s)G_v(s)]G_{sv}G_i(s)G_{pd} + G_{sv}Z_o(s)G_{pv}}{1 + G_i(s)NG_{sd}[F(s) + G_v(s)Z_o(s)]} + \frac{sC_{in}}{N} \quad (9)$$

$$Y_{PV}(s) = \frac{1}{M} \cdot \frac{1 + \frac{G_{vb}(s)V_{in}}{s^2L_bC_b} + \frac{V_{in}DP(s)}{sL_b} + \frac{1}{s^2L_bC_b}}{(1 - D_b)^2 \frac{1}{sL_b} + I_L \frac{1-D_b}{sL_{in}} [DP(s) + \frac{G_{vb}(s)}{sC_b}]} \quad (10)$$

Table 1. Simulation parameters of LTDCTs.

LTDCT#1/#2/#3		LTDCT#4/#5/#6	
Parameter	Value	Parameter	Value
Number of submodules	10	Number of submodules	10
Nominal power (MW)	2	Nominal power (MW)	1
Switching frequency (Hz)	1000	Switching frequency (Hz)	1000

Table 1. Cont.

LTDCT#1/#2/#3		LTDCT#4/#5/#6	
Parameter	Value	Parameter	Value
Input voltage (kV)	20	Input voltage (kV)	20
Output voltage (V)	750	Output voltage (V)	750
Transformer ratio	200/75	Transformer ratio	200/75
Energy transfer inductor of each module (mH)	1.6	Energy transfer inductor of each module (mH)	3.2
Input capacitor of each module (mF)	1	Input capacitor of each module (mF)	0.8
Output capacitor (mF)	20	Output capacitor (mF)	15
Input current-limiting inductor (mH)	15	Input current-limiting inductor (mH)	10
Low-pass filter of current control	$(200\pi)^2 / [s^2 + 1.414 \times 200\pi s + (200\pi)^2]$	Low-pass filter of current control	$(200\pi)^2 / [s^2 + 1.414 \times 200\pi s + (200\pi)^2]$
Output current controller	$(s + 100\pi) / (10,000s)$	Output current controller	$(s + 100\pi) / (5000s)$
Voltage controller	$(s + 40) \times 2850 / [s(s + 400)]$	Voltage controller	$(s + 40) \times 2140 / [s(s + 400)]$
Line distance (km)	4	Line distance (km)	1

Table 2. Simulation parameters of PVDCTs.

PVDCT#1		PVDCT#2	
Parameter	Value	Parameter	Value
Number of submodules	10	Number of submodules	10
Nominal power (MW)	2	Nominal power (MW)	1
Switching frequency (Hz)	1000	Switching frequency (Hz)	1000
Output voltage (kV)	20	Output voltage (kV)	20
Input voltage (V)	750	Input voltage (V)	750
Transformer ratio	75/200	Transformer ratio	75/200
Energy transfer inductor of each module (mH)	0.225	Energy transfer inductor of each module (mH)	0.45
Input capacitor (mF)	20	Input capacitor (mF)	15
Output capacitor of each module (mF)	1	Output capacitor of each module (mF)	0.8
Output current-limiting inductor (mH)	15	Output current-limiting inductor (mH)	10
Output voltage controller	$0.157(s + 180) / [s(s + 100\pi)]$	Output voltage controller	$0.157(s + 180) / [s(s + 100\pi)]$
Line distance (km)	2.5	Line distance (km)	2

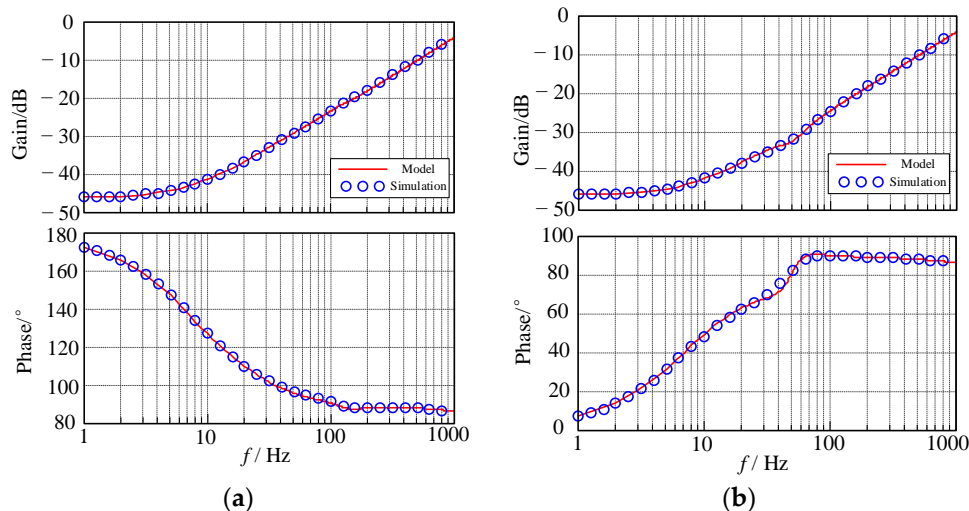


Figure 6. Admittance of DCTs at MVDC side. (a) LTDCT; (b) PVDCT.

### 5. Stability Analysis of the DC System

The stability analysis for the DC system shown in Figure 1 is carried out. The parameters of the VCMMC and PCMMC are shown in Table 3. Suppose that the system includes 2 PVDCTs and 6 LTDCTs; the corresponding parameters are shown in Tables 1 and 2, and the line impedance is listed in Table 4. DCTs all work under rated state, and the PCMMC outputs 3 MW active power. The admittance characteristics of the system are shown in Figure 7a; it can be seen that the resonance occurs at 130 Hz and 178 Hz in the bode plot of  $Y'_{\sigma}$  due to the impact of the DCT's capacitors and its corresponding current limiting inductor. At the same time, the admittance characteristics of PVDCT #2 and LTDCT #4/#5/#6 transfer from inductance to capacitance at 130 Hz, and parallel resonance is generated with PVDCT#1 and LTDCT#1/#2/#3, which are still inductive. Thus,  $Y'_{\sigma}$  has resonance peaks at 130 Hz and 178 Hz and a resonance valley at 151 Hz. The resonance problem may lead to oscillation of the capacitor voltage of the DCT. Moreover, the resonance may lead to the oscillation of the grid voltage.

Table 3. Simulation parameters of MMC.

VCMMC		PCMMC	
Parameter	Value	Parameter	Value
DC Voltage (kV)	20	DC Voltage (kV)	20
AC Voltage (kV)	10	AC Voltage (kV)	10
Nominal power (MW)	10	Nominal power (MW)	10
Arm inductor (mH)	8	Arm inductor (mH)	8
Equivalent capacitor of each arm (mF)	0.4	Equivalent capacitor of each arm (mF)	0.4
Current-limiting inductor (mH)	10	Current-limiting inductor (mH)	10
Current controller	$3 + 300/s$	Current controller	$3 + 300/s$
Low-pass filter of the DC voltage	$100\pi/(s + 100\pi)$	Circulating current controller	$3 + 500/s$
Voltage controller	$3 + 300/s$	Line distance (km)	2
Circulating current controller	$20 + 500/s$		

Table 4. Line impedance.

Line Impedance (per km)
$0.0599 + j2\pi \times 2.714 \times 10^{-4} \Omega$

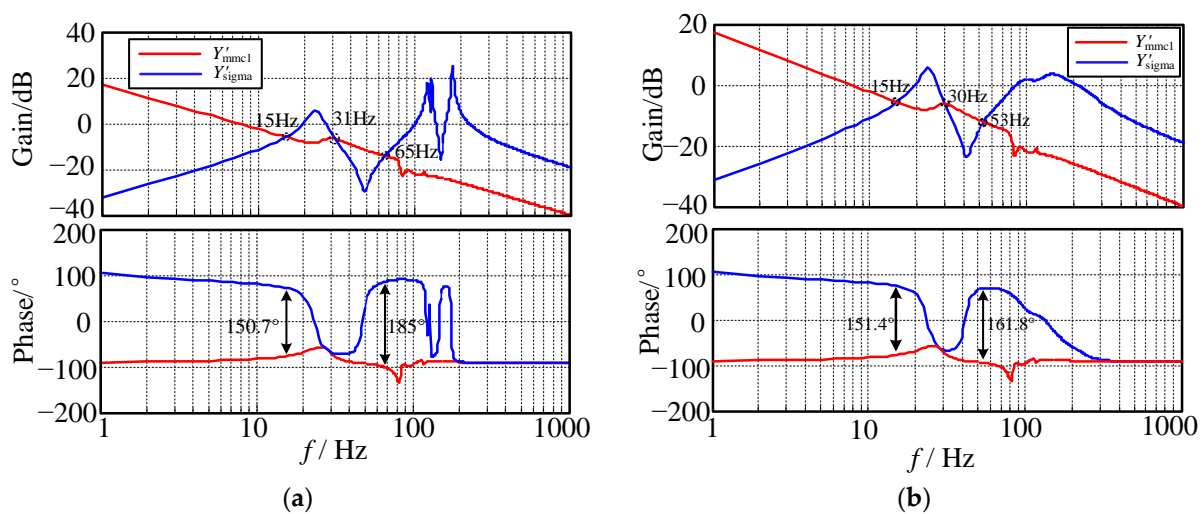


Figure 7. Stability analysis bode plots of the system under different conditions. (a) Without the active damping loop. (b) With the active damping loop.



As shown in Figure 7a,  $Y'_{mmc1}$  overlaps with  $Y'_{sigma}$  at 15 Hz, 31 Hz, and 65 Hz. The phase difference at 15 Hz is  $150.7^\circ$ , and the phase difference at 31 Hz is  $3.4^\circ$ , which all meet the stability requirements. Meanwhile, the phase difference at 65 Hz is  $185^\circ$ , which means that the phase margin is  $-5^\circ$ , and the system is unstable. It can be seen that at 65 Hz,  $Y'_{sigma}$  shows capacitance, while  $Y'_{mmc1}$  shows negative resistance and inductance. The lack of damping leads to system instability.

To solve the instability problem, the LC resonance at the medium voltage side of the DCT can be weakened by adding active damping, which can effectively enhance the stability at the input side of the DCT.

### 5.1. Active Damping Control Strategies for DCTs

It can be known from the previous analysis that the resonant peak and valley of  $Y'_{sigma}$  are mainly caused by the influence of the capacitor and current-limiting inductor at the medium voltage side of DCTs. Therefore, active damping control strategies can be implemented to increase the equivalent resistance at the resonant frequency to improve the system stability. The active damping loops are implemented in Figure 8:

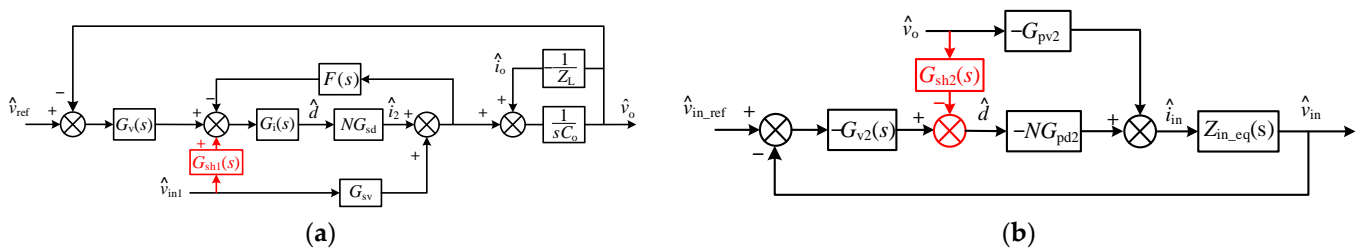


Figure 8. Active damping control strategies of DCTs. (a) LTDCT; (b) PVDCT.

With the active damping loops above, the admittance of the LTDCT and PVDCT are reshaped as (11) and (12). Comparing (9) with (11) and (10) with (12), it can be known that the active damping control is equivalent to parallel virtual impedance at the medium voltage side of DCTs.

Let  $G_{sh1}(s)$ ,  $G_{sh2}(s)$  satisfy the relationship in (13) and (14) respectively, where  $BF_1(s)$ ,  $BF_{PV}(s)$  are the band-pass filters (BFs) for LT DCTs and PV DCTs. The center frequency of the filter is its corresponding DCT's LC resonant frequency. The expression of the BF is written as (15);  $Q$  is the quality factor, which is 1 in this article, and  $f_p$  is the center frequency of the filter. In (13),  $R_{vd}$  is the virtual resistance of the LTDCT. In (14),  $R_{vPV}$  is the virtual resistance of the PVDCT.

$$Y_{ind}(s) = \frac{1}{N} \cdot \frac{G_{sv}Z_o(s)G_{pv} - [F(s) + G_v(s)Z_o(s)]G_{pd}G_i(s)}{1 + G_i(s)NG_{sd}[F(s) + G_v(s)Z_o(s)]} + \frac{G_{sh1}(s)G_i(s)[G_{pd} + NG_{sd}Z_o(s)G_{pv}]}{1 + G_i(s)NG_{sd}[F(s) + G_v(s)Z_o(s)]} + \frac{sC_{in}}{N} \tag{11}$$

$$Y_{ind\_PV}(s) = \frac{G_{pv2}Z_{in\_eq}(s)[G_{sv2} + G_{v2}(s)G_{sd2}]}{1 + G_{v2}(s)N_2G_{pd2}Z_{in\_eq}(s)} + \frac{G_{sh2}(s)[G_{sd2} - NG_{pd2}Z_{in\_eq}(s)G_{sv2}]}{1 + G_{v2}(s)N_2G_{pd2}Z_{in\_eq}(s)} + \frac{sC_{o\_PV}}{N_2} \tag{12}$$

$$G_{sh1}(s) = \frac{BF_1(s)}{R_{vd}} \cdot \frac{1 + G_i(s)NG_{sd}[F(s) + G_v(s)Z_o(s)]}{G_i(s)[G_{pd} + NG_{sd}Z_o(s)G_{pv}]} \tag{13}$$

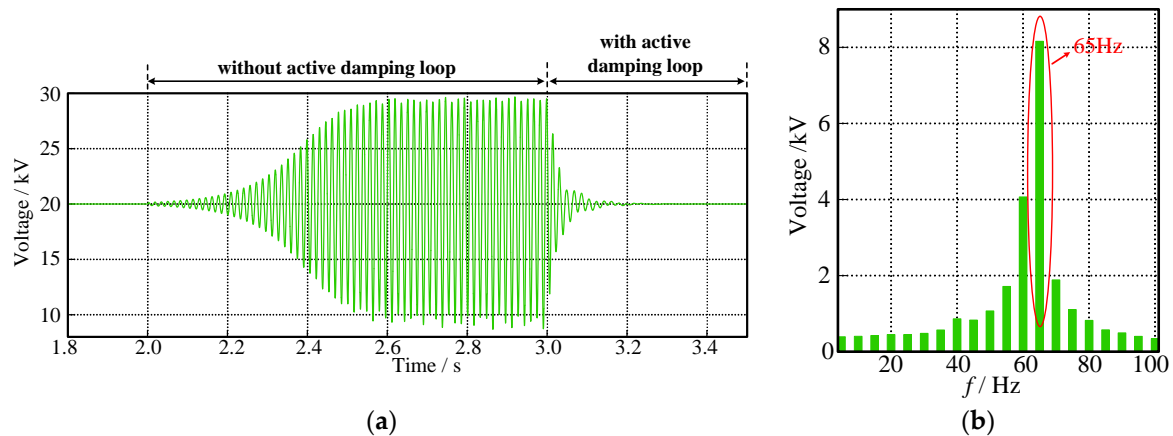
$$G_{sh2}(s) = \frac{BF_{PV}(s)}{R_{vPV}} \cdot \frac{1 + G_{v2}(s)N_2G_{pd2}Z_{in\_eq}(s)}{G_{sd2} - NG_{pd2}Z_{in\_eq}(s)G_{sv2}} \tag{14}$$

$$BF(s) = \frac{(2\pi f_p/Q)s}{s^2 + (2\pi f_p/Q)s + (2\pi f_p)^2} \tag{15}$$

According to the system parameters in Tables 1 and 2, set  $R_{vd}$  and  $R_{vPV}$  as  $25 \Omega$ . For LTDCT#1/#2/#3 and PVDCT#1, the central frequency for their BFs is 130 Hz. For LTDCT#4/#5/#6 and PVDCT#2, the central frequency for their BFs is 178 Hz. With the active damping loop, the bode plot of system admittance is shown in Figure 7b. The admittance overlapping frequencies are 15 Hz, 30 Hz, and 53 Hz. The phase difference is  $151.4^\circ$  at 11 Hz and  $4.5^\circ$  at 30 Hz, which all meet the stability requirements. At 53 Hz, the phase difference is decreased to  $161.8^\circ$ , which means that the phase margin increases to  $18.2^\circ$  and the system stability is effectively improved.

### 5.2. PLECS Simulation Verification

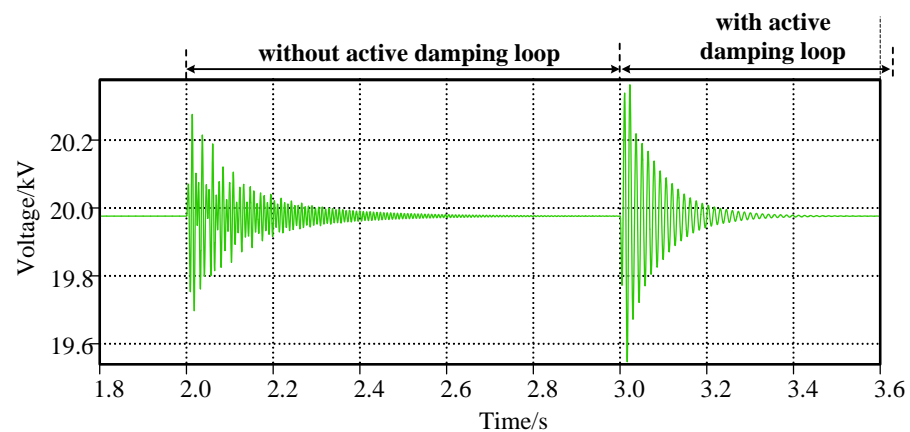
To verify the stability analysis above, the corresponding system simulation is built in PLECS. The system adopts the parameters in Tables 1–4. The system reaches the rated operating point before 2 s. At 2 s, the active damping control methods are cancelled. Then, the active damping control loops are implemented at 3 s. The voltage waveform of the DC system is shown as Figure 9a.



**Figure 9.** Voltage waveforms of the DC system. (a) With or without the active damping loop; (b) Frequency spectrum of the oscillation.

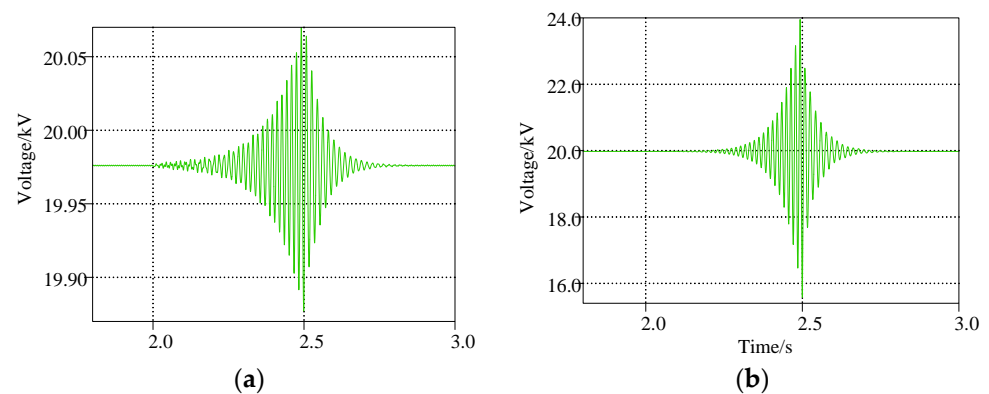
In Figure 7a, the impedance amplitude of  $Y'_{\sigma}$  and  $Y'_{mnc1}$  intersects at 65 Hz without the active damping loop, the phase angle difference is  $185^\circ$ , and the phase margin is  $-5^\circ$ , which means that the system is unstable. The corresponding DC voltage waveform in Figure 9a is 2–3 s, and the DC voltage fluctuates up to 10 kV. The corresponding Fourier analysis spectrum is shown in Figure 9b. It shows that the oscillation frequency is 65 Hz, indicating that the instability phenomenon is consistent with the theoretical analysis. With the active damping loop implemented, Figure 7b shows that the impedance amplitude of  $Y'_{\sigma}$  and  $Y'_{mnc1}$  intersects at 53 Hz with the active damping loop implemented. The phase difference is  $161.8^\circ$ , and the phase margin increases to  $18.2^\circ$ . The system can operate stably, and the corresponding waveform shown in Figure 9a is after 3 s. The bus voltage is maintained at 20 kV, which is consistent with the theoretical analysis in Figure 7b.

To verify the voltage resonance results from the current-limiting inductors, the corresponding system simulations were repeated while both inductors of the PCMMC and VCMMC at the medium voltage side were removed. As shown in Figure 10, the system remains stable, and the corresponding DC voltage fluctuates slightly and quickly stabilizes to 20 kV at 2 s and 3 s when the loop control is withdrawn or added.



**Figure 10.** Voltage waveforms of the DC system without current-limiting inductors.

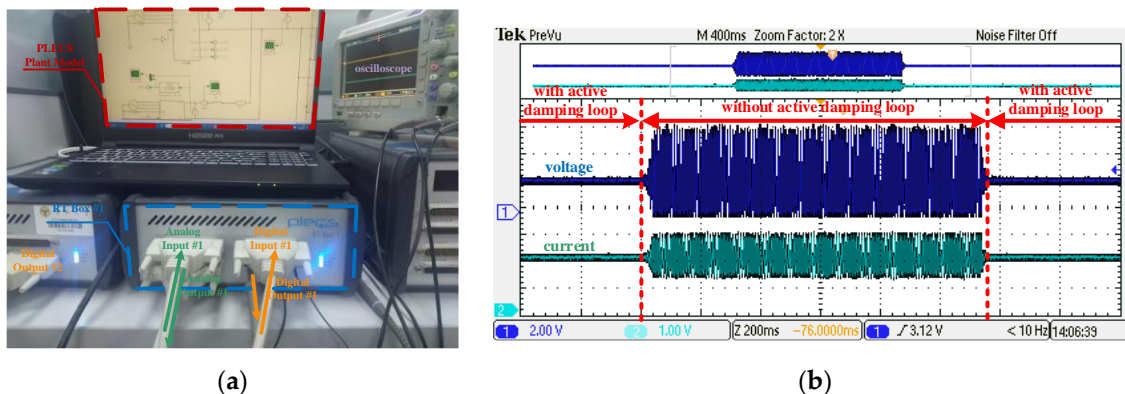
In Figure 6, the LTDCT shows negative input impedance at low frequencies, while the PVDCT shows positive input impedance at low frequencies. Therefore, the PVDCT can provide damping for the system and be conducive to system stability, and the LTDCT has the opposite effect. The corresponding system simulation verifies the characteristics through setting differently rated power ratios of the LTDCT and PVDCT. As shown in Figure 11, a disturbance is added at 2 s and withdrawn at 2.5 s, and the corresponding voltage can stabilize to 20 kV in both conditions. However, the voltage fluctuation in the high ratio condition (LTDCT:PVDCT = 1:2) is less than 0.1 kV and much smaller than the low ratio condition (LTDCT:PVDCT = 1:5), which is over 4.0 kV at 2.5 s. The result verifies the analysis above, and it is recommended to moderately increase the rated power of the LTDCT in the DC system.



**Figure 11.** Voltage waveforms of the DC system with differently rated power ratios of LTDCT and PVDCT. (a) LTDCT:PVDCT = 1:2; (b) LTDCT:PVDCT = 1:5.

### 5.3. RT Box Hardware-in-Loop Simulation Verification

Hardware-in-loop simulation is highly recommended to further verify the correctness of the theoretical analysis and simulation results, and the RT Box semi-physical simulator of PLECS is designed for power electronics applications with rich digital and analog interfaces. It can effectively simulate the actual performance of converters while avoiding device damage caused by real experiments of the 20 kV system. As shown in Figure 12a, connecting two RT Boxes back-to-back allows for complete system testing; one simulates the system, and the other simulates the controller.



**Figure 12.** RT Box hardware-in-loop simulation. (a) Voltage waveforms of the oscilloscope; (b) Back-to-back experiment platform.

As shown in Figure 12b, the fluctuation of voltage waveforms is similar to Figure 9, which further verifies the correctness of the simulation in PLECS.

## 6. Conclusions

1. A new admittance stability criterion is proposed in this paper. The overall stability of the system can be determined only by the equivalent admittance ratio  $T_m$  in Equation (3). This criterion has clear physical meaning and concise evaluation expression. In practical engineering, the corresponding impedance sum can be obtained with frequency-sweeping impedance measurement, and the impedance stability can be determined.
2. The output impedance of the PVDCT shows positive resistance characteristics in the bandwidth range, which can provide damping for the system and be conducive to system stability, while the input impedance of the LTDCT shows negative resistance characteristics in the bandwidth range, which is not conducive to system stability.
3. The current-limiting inductors are equipped in DCTs and have resonance with the capacitors of DCTs. Due to the negative input impedance characteristic of the LTDCT, resonance between the inductor and capacitor easily causes the instability of the system. The active damping control methods adopted in this paper can provide virtual resistance for DCTs to suppress resonance. The active damping methods can be generally configured in DCTs connected with the DC DPS to improve the stability of the DC system.

**Author Contributions:** Conceptualization, J.Y. and J.W.; methodology, J.W.; software, S.L.; writing—review and editing, X.J.; validation, X.X.; resources, Z.W. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research was funded by the Science and Technology Project of State Grid Corporation of China (5400-202255160A-1-1-ZN).

**Data Availability Statement:** No new data were created or analyzed in this study. Data sharing is not applicable to this article.

**Conflicts of Interest:** The authors declare no conflict of interest.

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