



Article

Resonant Gate Drive Circuit with Active Clamping to Increase Efficiency and Reliability

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Abstract: In power converters with high switching frequency, drive losses constitute a significant portion of the overall power losses. Resonant gate drivers can reduce drive losses, thereby enhancing the efficiency. However, resonant drivers suffer certain challenges: parameter drifts lead to the mismatch between the resonant frequency and the control frequency, and this mismatch can cause gate-to-source voltage overshoot. Moreover, the resonant driver is susceptible to external interference. This paper proposes a resonant circuit structure and control timing scheme aimed at overcoming these limitations. By incorporating a half-bridge clamp circuit, the proposed design achieves voltage clamping, thereby insulating the system from disturbances caused by mains power fluctuations. When there is a mismatch in resonant frequencies, the strategy employs a combination of hardware circuit diodes and control system timing to prevent overvoltage issues. Additionally, the utilization of MOSFETs minimizes the loss caused by prolonged current flow through body diodes, further reducing the resonant driving losses. Simulations have demonstrated the system's stability under varying resonant parameters and its effective anti-interference capabilities in voltage clamping. Experiments achieved a power saving of 83.3% at a 1 MHz operating frequency. Both simulations and experimental validations confirm the feasibility of the proposed solution, its effectiveness in interference suppression, handling of resonant mismatches, and its role in further augmenting power conservation.

Keywords: high frequency; resonant gate driver; low power consumption; sensitivity



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1. Introduction

High switching frequency leads to power density enhancement in power converters [1–7]. However, increasing switching frequencies sharply enlarges the power losses [8,9]. This increased power loss issue is particularly notable in low-voltage circuits, such as Point of Load (POL) circuits [10]. For example, in [11], gate drive losses account for 19% of the total power loss at a frequency of 100 kHz. Therefore, increasing switching frequency will significantly increase the power loss and reduce the power efficiency. As a consequence, reducing driving power loss is necessary in applications with high switching frequency.

Ref. [12] proposed a resonant circuit in gate driver, and reduced the power loss from 122.02 mW to 64.5 mW [13]. The principle involves injecting energy into the gate capacitance of a MOSFET drive using a resonant inductor. In contrast, conventional gate drivers (CGD) use a drive Resistance R_g to provide energy, with 50% of the energy lost in the drive resistance. This circuit effectively reduces driving losses.

However, resonant driving has not been widely applied in the industry [14]. Compared to conventional driving schemes, resonant driving faces several issues:

1. Resonant gate drivers are susceptible to external interference [13,15–19]. When there is high-frequency external interference, the interference directly flows through the MOSFET's gate capacitance rather than being bypassed by the driving circuit. This interference current causes voltage changes in the drive capacitor, potentially leading to system falsely turned ON/OFF. Conversely, in the conventional driver circuit, the V_{gs} is clamped to ON/OFF voltages with R_g , and is relatively less susceptible to the external interference current.
2. Resonant gate drivers may encounter frequency mismatch between the resonant frequency and the control frequency [15,20–23]. When the control frequency and the resonant frequency are not perfectly matched, the system may face issues such as overvoltage [24], increased losses [25], and over-resonance, severely affecting system reliability.
3. The losses in the resonant circuit are still high and need further reduction [16,26].

To solve the first issue, ref. [27–29] proposes a resonant gate driver based on a half-bridge circuit structure, achieving V_{gs} voltage clamping by enabling the upper and lower switches. However, significant energy loss occurs in the resonant circuit due to the body diode introduced in the MOSFETs, through which the current flows during operation [30]. The structure presented in [31] is similar to [27], utilizing additional capacitors in the circuit to achieve negative voltage cutoff. However, the cutoff voltage is determined by the pre-charge current, leading to inappropriate cutoff voltage during fluctuations in circuit parameters. Ref. [16] employs a full-bridge circuit structure, achieving voltage clamping by enabling the upper and lower switches in the right bridge arm. Nevertheless, the loss through the body diode during the energy recovery phase is non-negligible.

Ref. [32] leverages the unidirectional conduction property of the MOSFET's body diode to address the second issue. However, the body diode in the circuit also induces substantial conduction losses. Ref. [33–35] adopt a similar approach by adding additional diodes to the resonant circuit to resolve the second issue. However, these diodes similarly result in significant conduction losses. The circuit proposed in [15], as shown in Figure 1, exhibits high tolerance to pulse width variations, but the gate is clamped only during the energy recovery stage, and the diode in this stage introduces non-negligible losses.

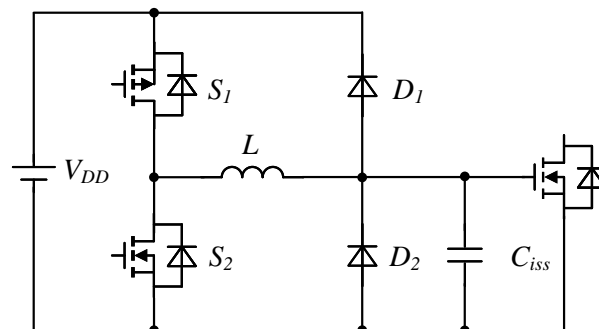


Figure 1. Resonant gate driver with efficient energy recovery in [15].

The driver proposed in [36,37] achieves bidirectional voltage switching, with the energy transferred from the driven capacitor to the inductor returning to the capacitor with opposite voltage polarity, significantly reducing power losses. However, this method fails to address clamping and mismatch issues arising from parameter fluctuations. Refs. [38,39] adopts a full-bridge circuit structure, avoiding losses through the body diode with different operating timing and achieving voltage clamping. Nevertheless, mismatch issues arise due to parameter fluctuations.

This manuscript proposes a new resonant driving circuit topology, meeting all the three key requirements of reduced loss, reliable clamping, and stability in the face of frequency simultaneously. By utilizing the body diode of auxiliary MOSFETs, this design can operate stably even when the resonant frequency changes, achieving V_{gs} clamping through the conduction of the upper and lower tubes. In high-frequency resonant circuits,

the conduction loss of diodes constitutes a significant percentage of the overall losses of driving losses. The circuit proposed in this paper avoids diode losses, further reducing driving losses.

The structure of this paper is as follows: Section 2 introduces the circuit structure and working principle of the resonant driver; Section 3 discusses the impact of errors on the sensitivity of the resonant gate driver; Section 4 presents the parameter design process for the proposed gate driver; Sections 5 and 6 cover simulation and experimental validation, respectively. Finally, the conclusions are drawn in Section 7.

2. Circuit and Operation Principle

2.1. Gate Drivers Power Losses

Figure 2 illustrates the conventional gate driver circuit for the widely used power MOSFET, employing a totem pole topology. In conventional gate driver circuits, the losses are given by:

$$P_{\text{gate}} = QVf = CV^2f \quad (1)$$

In addition to the CV^2 losses, under high-frequency operating conditions, the losses associated with the auxiliary switch cannot be neglected. These include both the drive losses and switch losses.

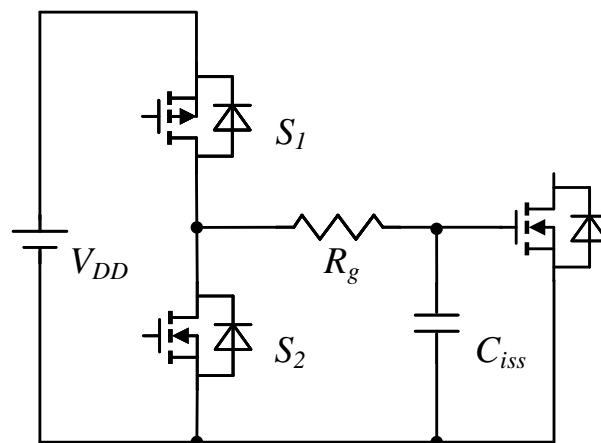


Figure 2. Conventional gate drivers (CGD).

Switch losses comprise switch capacitor losses and hard switch losses. Furthermore, the turn-on and turn-off of the traditional gate driver circuit can be equivalent to an RC circuit, where the switching time is constrained by the gate resistance and input capacitance. This results in slow drive speeds. Under high-frequency switching conditions, it becomes challenging to reduce gate losses effectively.

2.2. Existing Resonant Drivers

Resonant driving, achieved by incorporating a resonant inductor, serves to mitigate driving losses and, to a certain extent, expedite switching times. The majority of resonant driving topologies are based on half-bridge and full-bridge circuit structures. This approach aims to enhance the efficiency and performance of the driving circuit, contributing to a reduction in power losses and an improvement in switching dynamics.

Taking the structure in Figure 1 as an example, the resonant circuit has four operational stages. In the first stage, switch S_1 conducts, and LC resonance charges. The inductor current and C_{iss} voltage start to rise until the current reaches its maximum value, and C_{iss} voltage is V_{cc} . In the second stage, S_1 is turned off, and the inductor current continues to flow through the body diode of switch S_2 , inductor, diode D_1 , and V_{DD} loop. The voltage across the input capacitor is clamped by diode D_1 . In another operational stage, switch

S_2 conducts, and LC resonance discharges. Resonant drive losses include switch drive losses, conduction losses (equivalent resistance losses and diode losses), switch losses, and inductor losses.

In resonant drive circuits, beyond losses through resistive dissipation in the loop, it is imperative to consider losses incurred in the diodes within the circuit. The recovery path of energy following resonant charging and discharging traverses through the body diodes of MOSFETs and diodes. Consequently, within the losses of this resonant circuit, the impact of diode losses emerges as a significant factor that should not be disregarded. This recognition underscores the importance of comprehensively assessing and addressing diode-related losses for a more thorough understanding and optimization of resonant drive circuit performance.

2.3. Proposed Resonant Circuit and Operation Principle

2.3.1. Operation Principle

Recognizing the significance of diode losses in resonant gate drive circuits, this paper proposes a novel circuit topology aimed at further reducing the losses in the drive circuit. The proposed resonant drive circuit structure is illustrated in Figure 3. This circuit comprises four N-channel MOSFETs, a resonant inductor (L), and capacitors (C_1 and C_2). Capacitors C_1 and C_2 are utilized to evenly divide the supply voltage. By controlling the timing of four auxiliary switches, diode losses can be mitigated, thus achieving a more efficient resonant drive. The main waveforms of the resonant gate driver are depicted in Figure 4. Figures 5 and 6 illustrate six operational modes of the resonant gate driver. These modes manifest sequentially in the order of time t_0 – t_6 . The intricacies of these modes are discussed below.

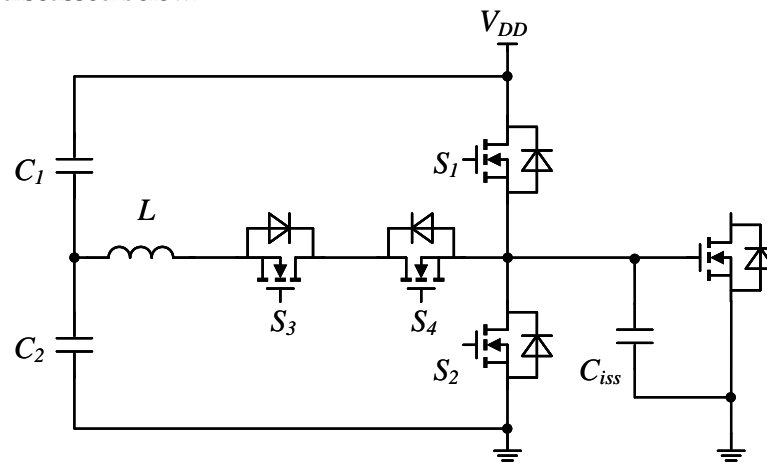


Figure 3. Proposed resonant gate driver with active clamping.

t_0 – t_1 : Before t_0 , only switch S_2 is conducting, and the gate-source voltage of the power MOSFET is clamped at zero volts through S_2 . At time t_0 , switches S_3 and S_4 conduct in a zero-current switching mode, treating capacitor C_1 as a voltage source for resonant charging of the inductor and power MOSFET gate capacitance. The current path is C-L- S_3 - S_4 - C_{iss} .

t_1 – t_2 : At t_1 , switch S_3 is turned off in advance, allowing the current to freewheel through the body diode of S_3 . When the current decreases to zero, the resonant charging stage ends due to the unidirectional conduction of the diode.

t_2 – t_3 : At t_2 , switches S_3 and S_4 are turned off, and switch S_1 is turned on. The gate-source voltage of the power MOSFET is connected to V_{cc} , and the gate-source voltage is clamped at V_{DD} . At t_2 , exactly halfway through the resonant period, the inductor current decreases to zero, and the gate-source voltage of the power MOSFET increases to V_{DD} , enabling switches S_3 and S_4 to turn off in a zero-current switching mode and switch S_1 to turn on in a zero-voltage switching mode.

t_3-t_4 : At t_3 , switch S_1 turns off in a zero-voltage switching mode, and switches S_3 and S_4 conduct in a zero-current switching mode. C_{iss} starts to discharge, and its current path is $C_{iss}-S_4-S_3-L-C$. The energy stored in C_{iss} is fed back to C.

t_4-t_5 : At t_4 , switch S_4 is turned off in advance, allowing the current to freewheel through the body diode of S_4 . When the current decreases to zero, the resonant charging stage ends due to the unidirectional conduction of the diode.

t_5-t_6 : At t_5 , the same principle applies. Switches S_3 and S_4 turn off in a zero-current switching mode, and switch S_2 turns on in a zero-voltage switching mode. The gate-source voltage is clamped at zero volts.

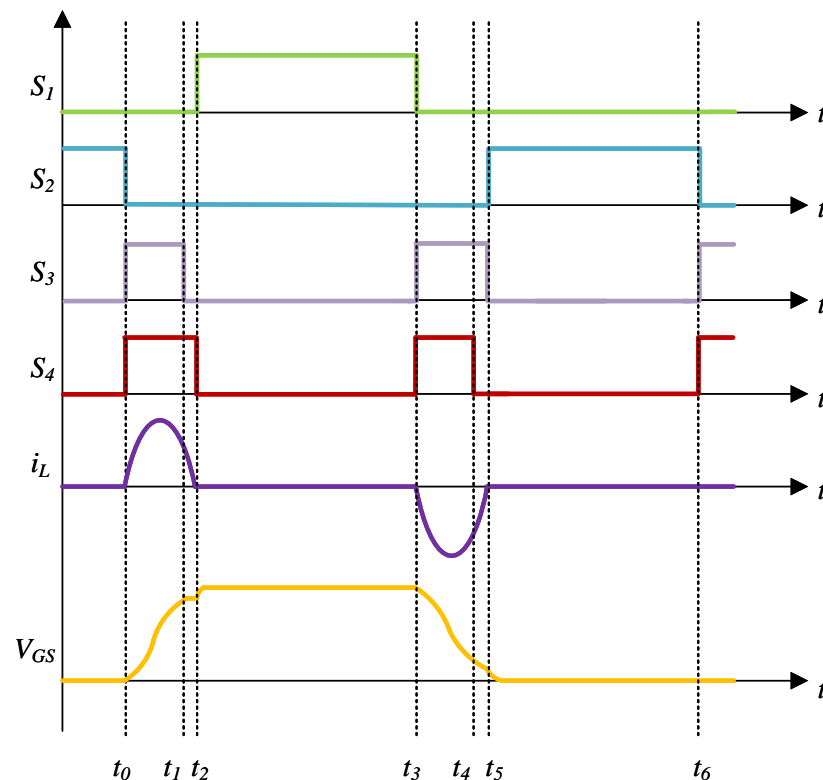


Figure 4. Switching states of MOSFETs and waveforms of i_L and V_{GS} .

2.3.2. Loss Analysis

In the previous chapter, we discussed the turn-on and turn-off operations of switches S_3S_4 under ZCS conditions and switches S_1S_2 under ZVS conditions. Consequently, in the analysis of losses, the switch losses of the auxiliary switches were significantly reduced. Due to the relatively small and short-duration current flow through the body diode of the MOSFET, the associated losses are considered negligible in the loss calculation. The losses within the gate driver circuit encompass the driver losses of the MOSFETs, the conduction losses of the driver circuit, and the losses within the inductor.

The driver losses of the MOSFETs switch can be expressed as:

$$P_g = (2Q_{g_{s1}} V_{g_{s1}} + 2Q_{g_{s2}} V_{g_{s2}} + Q_{g_{s3}} V_{g_{s3}} + Q_{g_{s4}} V_{g_{s4}}) f \quad (2)$$

Here, Q_g represents the gate charge of the MOSFETs, and V_g represents the gate-source voltage of the MOSFETs.

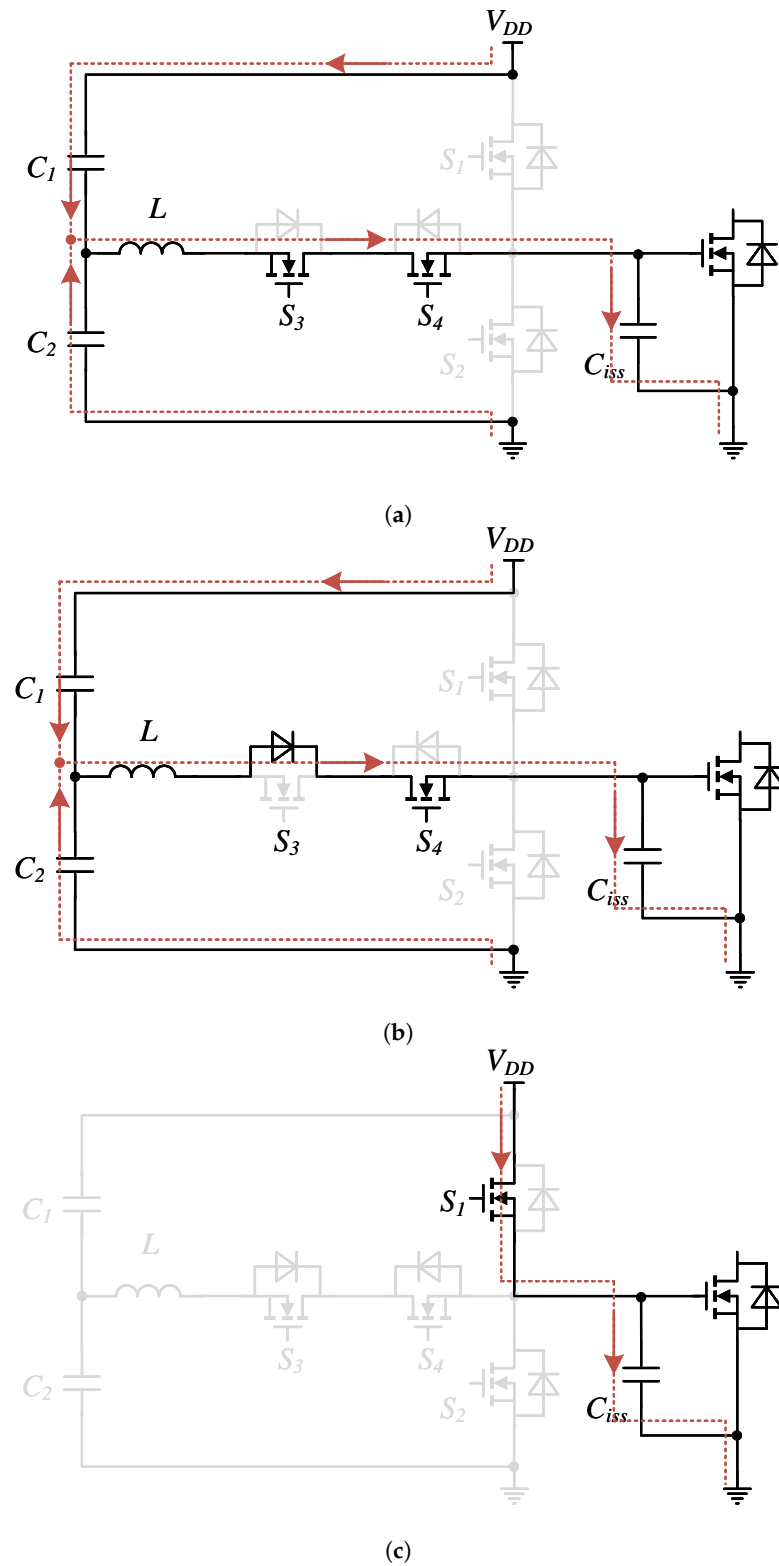


Figure 5. Equivalent circuits of each stage during turn-on transition, (a) resonant charging stage, $[t_0, t_1]$, (b) reverse current mitigation stage, $[t_1, t_2]$, (c) clamping stage, $[t_2, t_3]$.

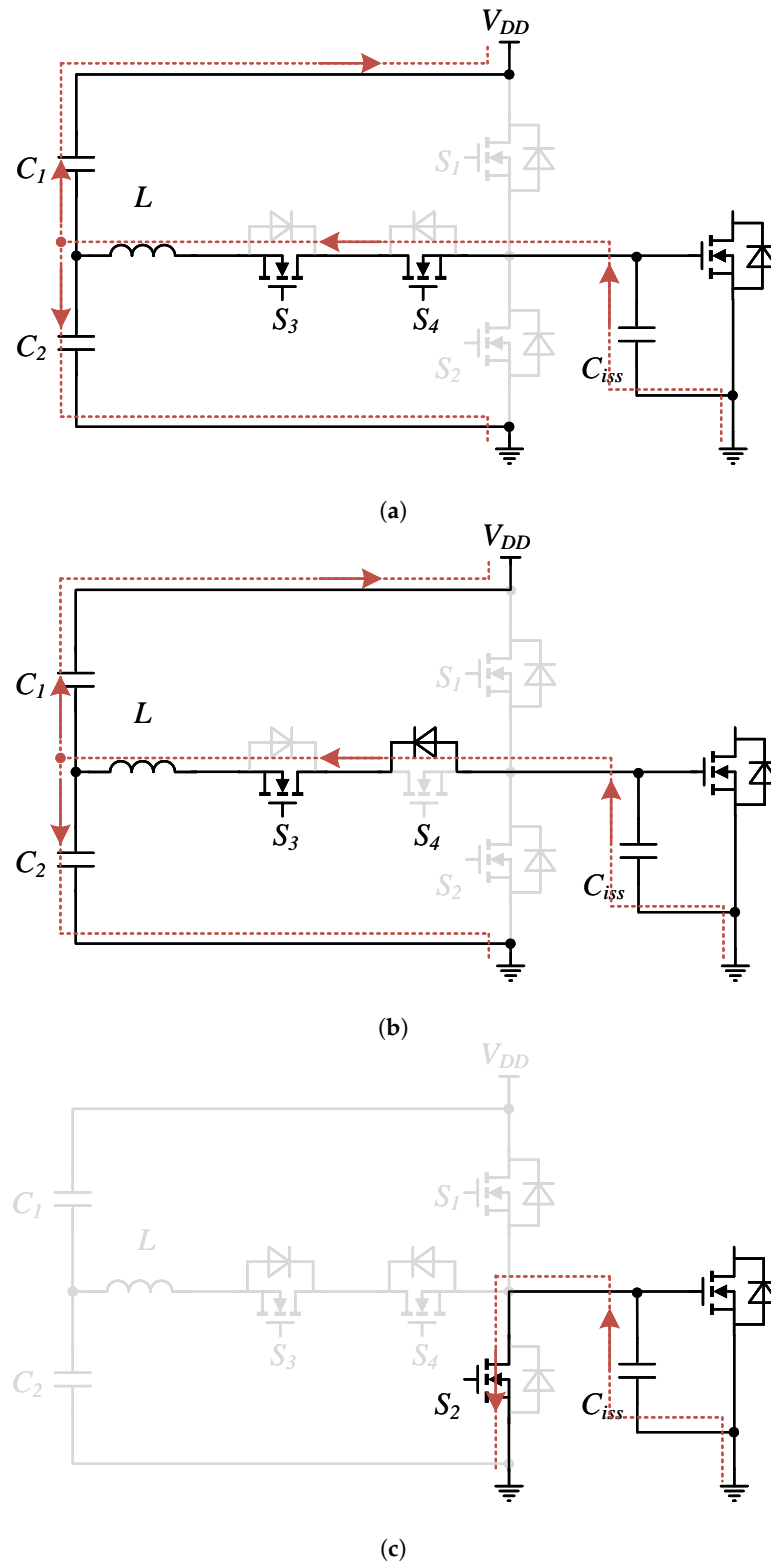


Figure 6. Equivalent circuits of each stage during turn-off transition, (a) resonant discharging stage, $[t_3, t_4]$, (b) reverse current mitigation stage, $[t_4, t_5]$, (c) clamping stage, $[t_5, t_6]$.

The resonant frequency can be calculated based on the selected inductance and the equivalent input capacitance. The resonant frequency can be expressed as

$$f = \frac{1}{2\pi\sqrt{LC_{iss}}} \quad (3)$$

The resonance period can be expressed as

$$T_{res} = 2\pi\sqrt{LC_{iss}} \quad (4)$$

Resonance conduction loss can be expressed as

$$P_{cond} = 2f \int_0^{\frac{T_{res}}{2}} i_L(t)^2 R_{eq} dt \quad (5)$$

R_{eq} are $2R_{ds}$.

$$i_L(t) = \frac{V_{DD}}{2\omega L} e^{-\alpha t} \sin \omega t \quad (6)$$

The angular frequency of damped resonance is denoted as ω . Due to the relatively small value of R_{eq} , the damped resonance angular frequency can be approximated as the undamped resonance angular frequency. The damping coefficient is

$$\alpha = \frac{R_{eq}}{2L} \quad (7)$$

After a charging stage lasting half a resonant period, at this point, the voltage across C_{iss} is

$$V_{gs} = \frac{V_{DD}}{2} (1 + e^{-\frac{\alpha\pi}{\omega}}) \quad (8)$$

Subsequently, energy is replenished to C_{iss} through the power supply, and clamping is applied. The current during this stage is

$$i_r(t) = \frac{V_{DD} - V_{gs}}{R_{eq}} e^{-\frac{t}{R_{eq}C_{iss}}} \quad (9)$$

At this juncture, R_{eq} is equivalent to R_{ds} .

The energy replenishment stage involves

$$P_r = 2f \int_0^{KR_{eq}C_{iss}} i_r(t)^2 R_{eq} dt \quad (10)$$

K is a constant. When K is greater than or equal to 3, the capacitor voltage approximately reaches its maximum value. It is recommended to set K as 3.

The inductive losses include copper loss and iron core loss. Copper loss is as follows:

$$P_{copper} = 2f \int_0^{\frac{T_{res}}{2}} i_L(t)^2 R_{ac} dt \quad (11)$$

The iron core loss is calculated using standard estimation methods. Compared to other losses, the iron core loss is relatively small and can be neglected. In addition, an air-core inductor is employed, and the iron loss is zero.

So, the total loss of the gate driver circuit can be expressed as:

$$P_d = P_{cond} + P_{copper} + P_g + P_r \quad (12)$$

3. Error to Sensitivity

The variation in the performance of inductor devices is a common phenomenon in power electronic circuits. One of the primary reasons influencing this variation is the temperature-induced impact on the magnetic core. With temperature fluctuations, the

magnetic properties of the core undergo changes, leading to fluctuations in the crucial characteristics of the inductor.

Furthermore, hollow-core inductor devices are similarly susceptible to direct influences from the external environment. External factors such as humidity, temperature, and surrounding materials can significantly affect the performance of air-core inductors. Therefore, the ability of gate driver circuits to resist interference in situations of small-scale fluctuations in inductance values becomes crucial.

3.1. Existing Resonant Drive Circuit

The full-bridge resonant driving circuit is a common power electronic circuit, and its schematic diagram is shown in the Figure 7. During the charging stage, when both lower MOSFETs are simultaneously turned on, resonance occurs between the resonant inductor and the input capacitance of the power MOSFET, causing the C_{iss} voltage to change from $-V_{DD}$ to V_{DD} . Subsequently, the voltage across the input capacitance is maintained by turning on S_1S_4 . In the discharging stage, the same two lower MOSFETs are turned on, and resonance occurs between the inductor and capacitor, causing the input voltage to change to $-V_{DD}$. The voltage across the input capacitance is then maintained by turning on S_2S_3 .

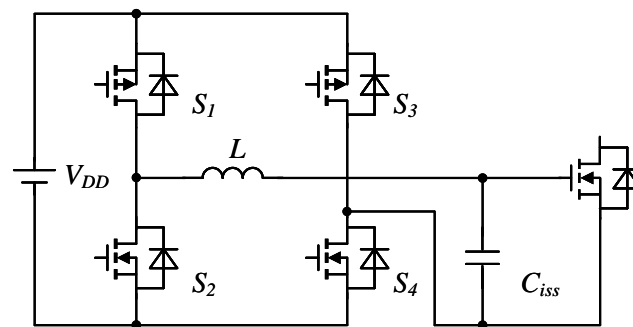


Figure 7. Resonant gate driver capable of high-frequency and high-efficiency operation in [36].

In existing resonant driving circuits, if the inductance is influenced under certain conditions, causing its actual value to be smaller than the ideal value, the resonant period may be smaller than the ideal value, leading to the occurrence of over-resonance. The input voltage of the power MOSFET continues to resonate even after reaching its maximum value, causing the voltage to decrease from its peak. Therefore, during the voltage maintenance stage, the power source needs to provide additional charging to the input capacitance, resulting in increased energy losses.

On the other hand, when the inductance is larger than its actual value, the actual resonant period may be greater than the ideal resonant period. Assuming the charging phase has ended and both lower switches are turned off, if the resonance has not ended and the inductor current has not decreased to zero, the continuity of the inductor current through $V_{DD}-S_1-L-C_{iss}-S_4$ may lead to overvoltage.

Thus, fluctuations in the inductance value may cause instability in the output of the full-bridge resonant driving circuit, impacting the performance of the circuit.

3.2. The Proposed Resonant Drive Circuit

The proposed resonant driving circuit demonstrates outstanding stability in the face of minor fluctuations in the inductance value or other errors. Even with slight variations in the actual inductance value, the circuit maintains relatively stable performance, being less susceptible to excessive impacts. This error-tolerance capability makes the resonant driving circuit more reliable in practical engineering applications, especially when dealing with small-scale fluctuations in inductance values, compared to other driving circuits.

When the actual inductance value is small, the circuit successfully avoids over-resonance through cleverly designed driving timing sequences. In the resonant charging phase, by strategically timing the shutdown of switch S_1 , the current flows through the

body diode of S_1 and S_2 , effectively concluding the resonant charging. As the inductor current decreases to zero, the resonant charging concludes through the unidirectional conduction of the diode. The same strategy applies in the discharge phase, where the timely shutdown of switch S_2 prevents over-resonance.

In the case of a larger actual inductance value, during the shutdown of switches S_3 and S_4 , the inductor current does not impact the voltage across the input capacitance. The inductor current continues to flow through the switches S_3S_4 in the driving loop, ensuring the smooth operation of the circuit.

4. Parameter Design

The parameter design of the resonant circuit is shown in the Figure 8.

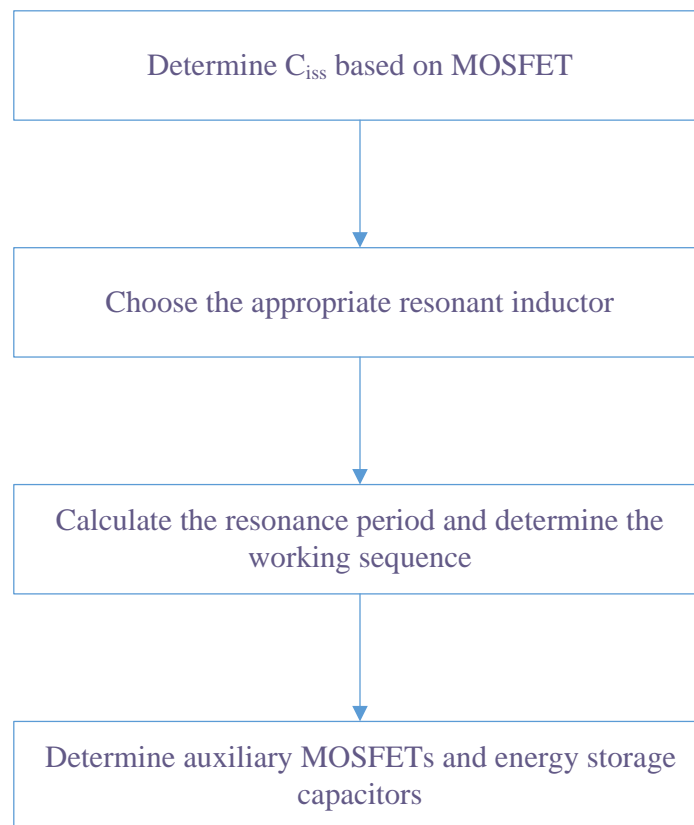


Figure 8. Parameter design flow chart.

1. Determination of Power MOSFET Model:

Select a suitable Power MOSFET model, considering its input capacitance (C_{iss}), and calculate the total charge (Q_g) to ensure that the drive circuit meets the design requirements.

2. Selection of Resonant Inductor:

Consider the impact of the resonant inductor on the charging and discharging speed as well as the overall system efficiency. When selecting the inductor, strike a balance between the charging and discharging speed of the circuit and its efficiency, avoiding severe influence from the equivalent resistance (R_{eq}) in the circuit. Choose an appropriate inductance value to enhance system efficiency while ensuring that the switch speed meets the requirements.

3. Calculation of Resonant Period and Determination of Drive Timing:

Based on the selected values of capacitance and inductance, calculate the resonant period and subsequently determine the drive timing of the resonant circuit. Ensure that the timing design meets the stability and performance requirements of the circuit.

4. Selection of Auxiliary Switch:

Choose an appropriate auxiliary switch to minimize conduction losses and drive losses. Ensure that the auxiliary switch operates stably in the circuit while meeting the design goals for performance and efficiency.

5. Selection of Energy Storage Capacitor:

Consider the energy storage requirements of the system and select a suitable energy storage capacitor. Ensure that the chosen energy storage capacitor can meet the energy storage and release requirements of the circuit and maintain stability throughout the entire system.

Below is a numerical example for design and parameter selection.

The IRF3415S/LPbF is chosen as the power device to be driven. According to the datasheet, at $V_{gs} = 10$ V, Q_g is 200 nC, and consequently, C_{iss} is determined to be 20 nF. Assuming the MOSFET's switching speed should be less than 200 ns, based on (4), the inductance value should be less than 202 nH. A larger inductance results in a higher quality factor of the resonant circuit, leading to lower energy loss. Considering energy loss and switching speed comprehensively, a 100 nH inductor is chosen for this example. According to (4), the resonant period is 280 ns, and the drive timing of the switch is controlled through software. Without considering circuit resistance, estimating the peak current is below 4.47 A based on the formula

$$I_{\max} = \frac{V}{\sqrt{\frac{L}{C_{iss}}}} \quad (13)$$

The IRLML6346 can meet the current-voltage requirements of the circuit. When the energy storage capacitor meets the voltage design requirements, the voltage drop should be minimized. In this case, a capacitor with a value three orders of magnitude higher than the input capacitor is chosen as the energy storage capacitor.

5. Simulation

Using Ltspice software (version 17.1.8 x64), the proposed resonant circuit was simulated to validate the rationality and feasibility of the circuit. The selection of the auxiliary switch model and parameters for the devices is presented in the table below. R_{sample} is added to the left side of the resonant inductor. The current waveform through the inductor can be obtained by measuring the voltage waveform across the sampling resistor.

According to the parameters of C_{iss} and L in Table 1, it can be calculated using (4) that the resonant period is approximately 280 ns. Under stable system conditions at an operating frequency of 1 MHz, it is observed that the switching frequency of the S_3S_4 switch is 2 MHz, with an on-time of 140 ns, while the switching frequency of the S_1S_2 switch is 1 MHz, with an on-time of 360 ns. Figure 9 illustrates the drive voltages and operational timing of each switch, along with the waveforms of inductor current and C_{iss} voltage obtained under these operating conditions.

The original simulation files are attached in the multimedia folder.

Figure 10 presents the V_{gs} under variations in inductance values, indicating that the resonant circuit can operate normally with a fluctuation of $\pm 10\%$ in inductance, ensuring system stability.

Table 1. The parameters of the resonant gate driver.

Parameter	Value	Parameter	Value
C_{iss}	20 nF	V_{DD}	10 V
$S_1 - S_4$	IRLML6346	L	100 nH
C	10 μ F	R_{sample}	100 m Ω

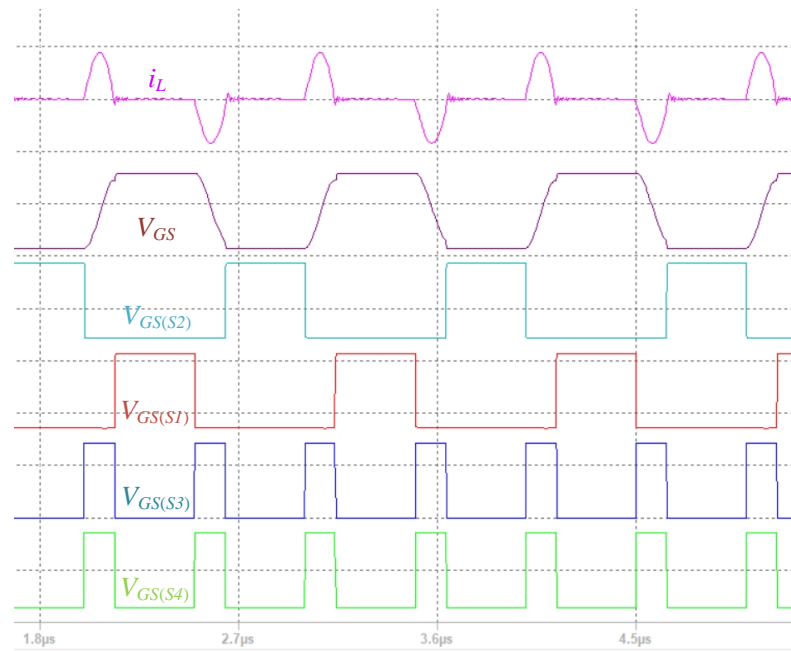


Figure 9. The simulated switching state of MOSFETs and the waveforms of i_L and V_{GS} .

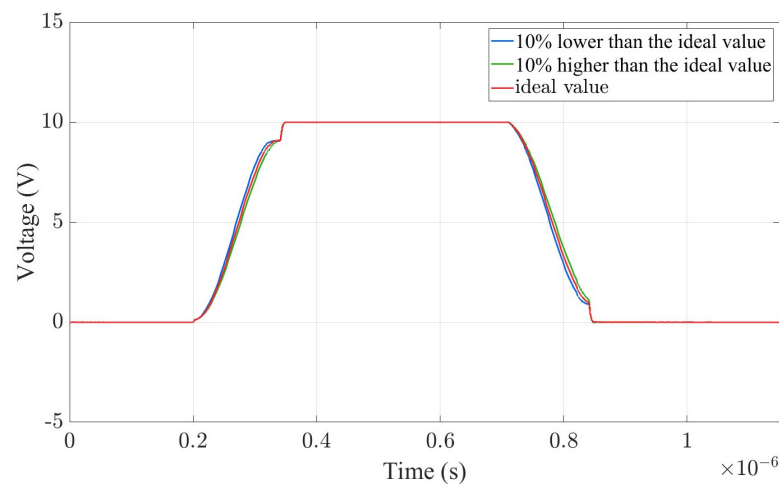


Figure 10. Impact of inductor value variations on V_{GS} .

6. Experiment

Figure 11 illustrates the PCB board of the resonant drive circuit, with a length of 4.15 cm and a width of 2.87 cm. To facilitate testing, the PCB board is initially designed with larger dimensions, but optimization can be applied to make the PCB more compact. The PCB includes a 100 m Ω sampling resistor for capturing the current of the resonant inductor, and a 20 nF capacitor serves as the input capacitance for the equivalent power MOSFET. There are a total of six input ports, including four input drive signals, V_{DD} , and GND.

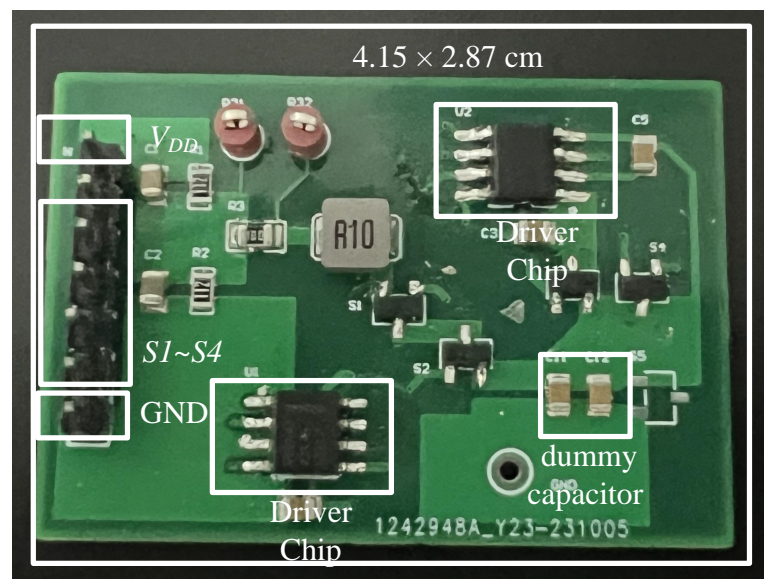


Figure 11. The proposed resonant gate driver circuit board.

Drive four auxiliary switches through a half-bridge driver chip and a low-side driver chip. The driver chip is a meticulously designed integrated circuit that controls the gate of a MOSFET by delivering essential signals, thereby regulating the MOSFET’s switching between the on and off states. Figure 12 shows the circuit diagram after adding a low-side driver chip that drives switches S_3S_4 and a half-bridge driver chip that drives half-bridge switches S_1S_2 . Table 2 provides the model numbers of the driver chips used in the experiment.

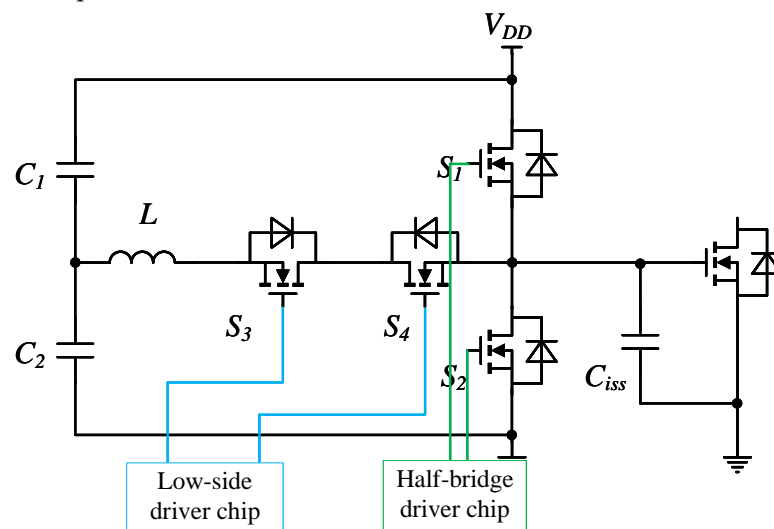


Figure 12. Driver circuit connection diagram.

Table 2. Driver chip selection table.

Driver Chip Type	Model Name
Low Side	UCC27324DR
Half Bridge	LM5101A

Figure 13 illustrates the experimental platform employed for the resonant gate driver. The utilized development board, namely LAUNCHXL-F28379D, has been programmed to generate customized fundamental drive signals tailored for the specific characteristics of

the investigated circuit. The power supply equipment utilized in the experimental setup is the RIGOL DP831, capable of delivering a direct current (DC) voltage of 10 V.

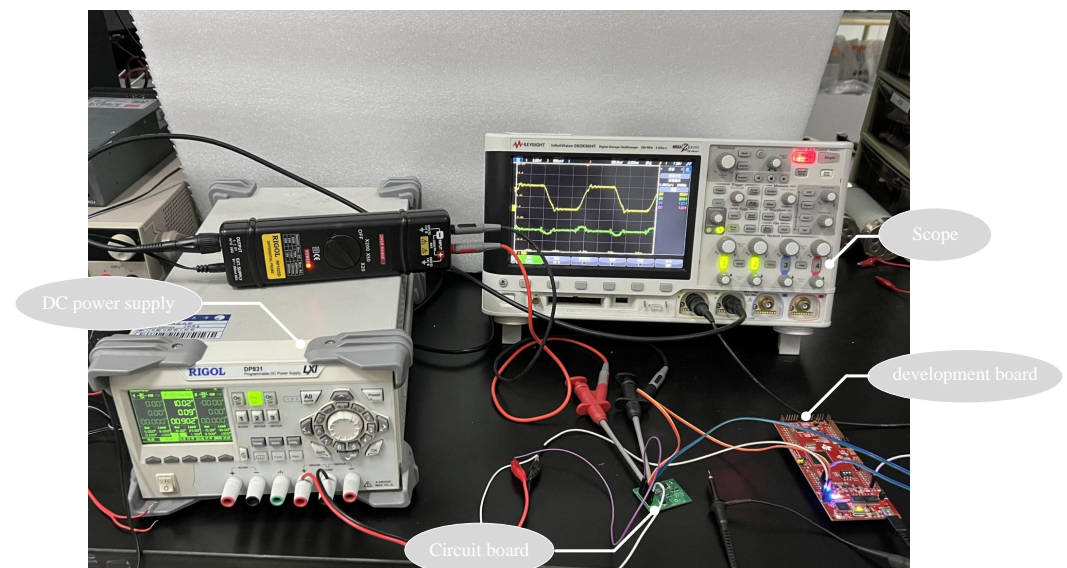


Figure 13. Experimental setup.

Figure 14 depicts the waveforms of V_{GS} and i_L . The experimental setup operates at a switching frequency of 1 MHz, with a peak current of 2 A in the inductor during resonance. After resonant charging stage, the voltage of the output V_{GS} remains stably at 10 V.

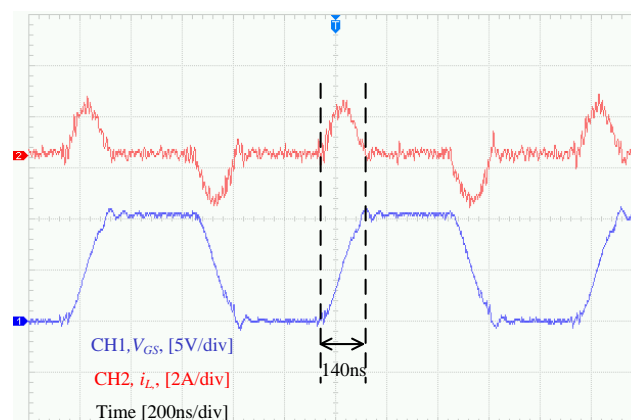


Figure 14. V_{GS} and i_L during switching transitions.

The table below illustrates the power losses of the CGD circuit, utilizing the circuit structure depicted in Figure 2, and the proposed resonant gate drive circuit. The comparison is made between power with the Driver Chip Loss and power without the Driver Chip Loss, showcasing the percentage reduction in power consumption for the proposed circuit compared to the conventional gate drive circuit.

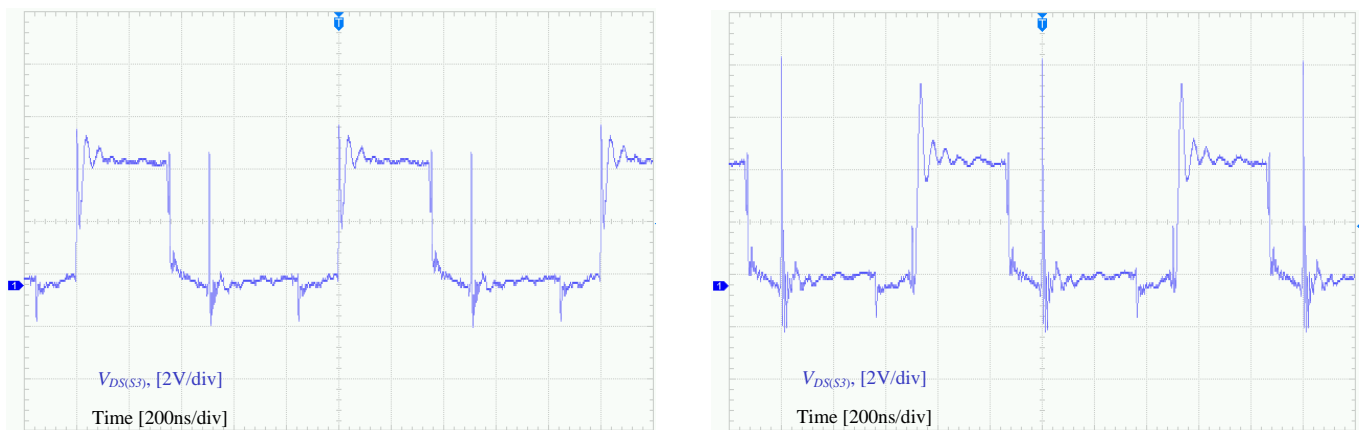
As indicated in Table 3, for the proposed resonant gate drive circuit with the inclusion of the drive chip, the power loss is reduced by 63.68% compared to the CGD. And in the absence of the drive chip, the power loss reduction reaches 83.30% compared to the CGD. This shows the significant improvement in power efficiency achieved by the proposed resonant gate drive circuit.

Table 3. Power loss comparison of CGD and proposed resonant gate drive at 1 MHz.

Type	Power with Driver Chip Loss		Power without Driver Chip Loss	
	Power Loss	Reduction	Power Loss	Reduction
CGD circuit	2512.89 mW	–	2185.72 mW	–
Proposed circuit	912.64 mW	63.68%	364.93 mW	83.30%

The experimental results indicate that the proposed resonant gate drive circuit exhibits higher efficiency and a smaller footprint compared to existing drive circuits.

It is noteworthy that when the actual value of the inductance is biased towards a higher value in resonant driving, the inductor current at the end of resonance does not decrease to zero. Consequently, the inductor current cannot continue flowing through the original circuit. At this point, switch S_3 experiences overvoltage across its terminals. Figure 15 illustrates the situation of the drain-source voltage across S_3 switch under normal conditions and during hard turn-off. Within a small error range of inductance values, the generated overvoltage remains within the rated V_{ds} range of the MOSFET. Despite the circuit exhibiting robust anti-interference capabilities and stability in practical design, the potential impact on the switch should not be overlooked.

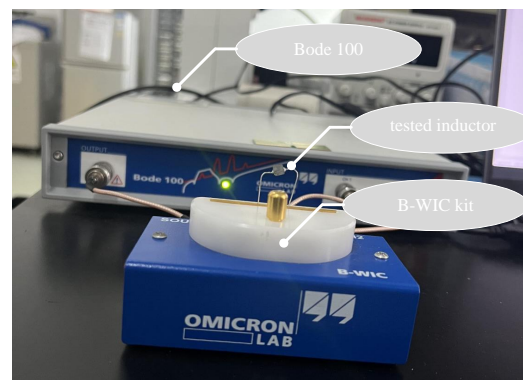


(a)

(b)

Figure 15. Impact of inductor on V_{ds} of Switch S_3 , (a) $L = 100$ nH, (b) $L = 131$ nH.

The inductance of 131 nH was achieved by adjusting the winding configuration on the existing 100 nH inductor. Figure 16 illustrates the impedance testing of the inductor using the Bode 100. Figure 17 depicts the test results, showing an inductance value of 131 nH at a working frequency of 1 MHz.

**Figure 16.** Impedance test using a Bode 100 with a B-WIC kit.

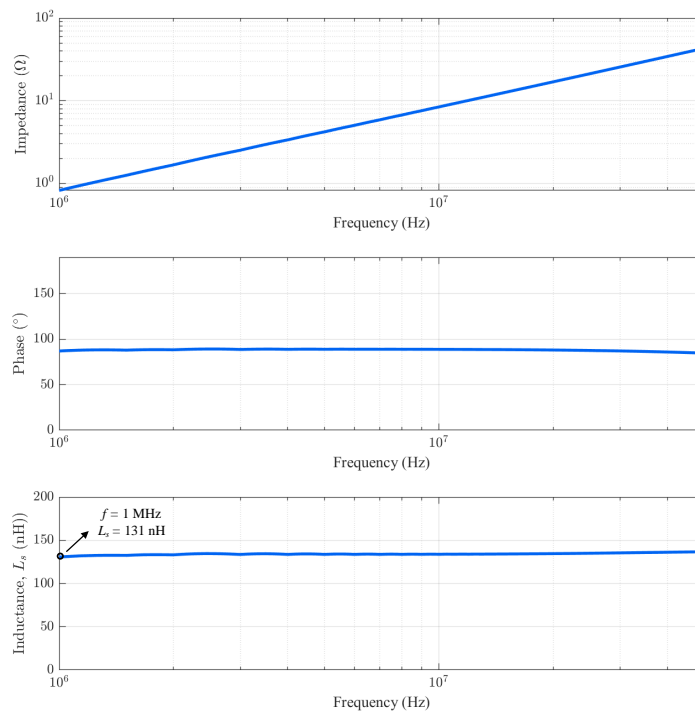


Figure 17. Inductance measurement results: phase, impedance, and inductance.

7. Conclusions

This paper proposes a resonant gate driving circuit with active clamping. Similar to the existing resonant gate drivers, the proposed circuit employs ZCS and ZVS to mitigate switching losses. In addition to the resonant driving effect, the proposed circuit has the following contributions:

1. The circuit is able to stabilize V_{gs} by the proposed active-clamp bridge, effectively preventing V_{gs} fluctuations.
2. The simultaneous switching of S_3 and S_4 avoids diode losses, thereby enhancing the overall system efficiency.
3. The control of switch scheme can mitigate the adverse effect caused by the mismatch between the resonant frequency and the control frequency.

Experimental validation shows that at $f_{sw} = 1$ MHz, the power consumption was reduced by 63.68%. Excluding the power consumption of the half-bridge and the low-side driver chips, the overall power reduction reached 83.30%.

Supplementary Materials: The following supporting information can be downloaded at: <https://www.mdpi.com/article/10.3390/wevj15020074/s1>.

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