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Theoretical Analysis on the Short-Circuit Current of Inverter-Interfaced Renewable Energy Generators with Fault-Ride-Through Capability

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Abstract: Renewable energy generators (REGs) usually employ power electronic devices for connecting with the grid, which makes their fault characteristics completely different from those of conventional synchronous generators. In the existing studies, the simulation methods are mainly adopted to analyze fault current contribution from REG. As a result, the explanations on the fault current show diversity and cannot reach a recognized standard. The REGs' mathematical model in relay-setting calculations is unknown. Thus, this paper theoretically analyses the fault current characteristics of inverter-interfaced REGs (IIREGs) with fault-ride-through (FRT) ability. In order to understand the fault current characteristics, the FRT control strategy for IIREGs is firstly studied. Then the characteristics of high-frequency and fundamental-frequency fault currents from IIREGs are theoretically analyzed after and during the faults. The affecting factors and duration time of different frequency fault currents are, respectively, revealed. Further, the mathematical expression of fundamental fault currents from IIREGs are derived and verified based on the experimental test bench. The results can be used in estimating the IIREGs' fault contributions and developing the fault calculation model.

Keywords: inverter-interfaced renewable energy generators; fault current; fault-ride-through control; wind power; solar power

1. Introduction

With the worldwide concern on environment pollution and the crisis on traditional fossil energy, renewable-energy penetration in power grids is expected to grow spectacularly [1]. In China, the government has launched eight 10-GW-level wind-power bases with an accumulated installed capacity of over 150 million kW and several large-scale solar energy power stations with a total installed capacity of 5 million kW during 2011–2015 [2]. These wind-power bases and solar power stations are located in the Chinese northern regions and coastal areas. They are connected to the transmission grid in a concentrated mode. As a result, the share of the renewable-energy generators (REGs) is increasing in the connected regional grids [3]. The REGs become indispensable in maintaining the stable and reliable operation of the grid.

In many countries, the newly devised grid code demands that the REGs must have the fault-ride-through (FRT) ability. As a result, the fault current contribution from REGs cannot be neglected. However, the fault characteristics of REGs are different from those of conventional synchronous generators (CSGs). Due to the REGs' special electricity-generating principles and the integration of power electronic converters, the analysis on the fault characteristics of REGs becomes

difficult. The existing study adopts the simulation methods [4,5]. The results depend on the simulation tests, so it is diversified. Thus, the universal equivalent model of REGs is unknown for fault analysis and relay setting calculations of power grids with high REG penetration.

As a result, Chinese regional power utilities generally adopt two protection solutions. One method considers the REGs as loads; thus, protection relay is not installed (or enabled). The other method considers the REGs as the CSGs; thus, the protection relays configured for both the REGs and grid sides at the outgoing lines are the same. This configuration may lead to protection malfunction at the wind-farm side of the outgoing lines [6]. To solve the problems, the fault contribution of different REGs must be theoretically analyzed.

REGs are classified into two types in terms of the integration mode of power electronic converters: partial- and fully-rated converter-interfaced REGs [7,8]. The former generally refers to wind turbines with doubly-fed induction generators, whereas the latter is referred to as inverter-interfaced REGs (IIREGs), including wind turbines with permanent magnet synchronous generators and photovoltaic panels and so on. This paper mainly concerns with the IIREGs' fault characteristics.

The IIREGs are connected to the grids only through a full-scale inverter, so their generating units are completely decoupled from the grid. The IIREGs' fault characteristics are affected mainly by the inverters' control mode, the inverters' integration circuits, and so on. With the FRT requirements [9,10], the IIREG fault characteristics are closely associated with the grid-tie inverters' FRT strategy. However, the FRT strategies are diverse from manufacturer to manufacturer and unknown to the public.

To clearly reveal the fault characteristics of IIREGs, the basic action is to study on the FRT control strategy. Many advanced control techniques have been developed for grid-tie inverters, including deadbeat controllers [11], predictive techniques [12,13], controllers based on artificial intelligence tools [14], and multi-loop feedback controllers [15–19], and so on. Due to its good performance and simplicity, multi-loop feedback control appears as an attractive way for the inverter control. In achieving FRT ability, the widely used control strategies are the vector-oriented current feedback control [15]. They are suitable only for symmetrical faults and cannot improve the FRT ability under the asymmetrical faults.

In order to enhance the asymmetrical FRT ability, some control strategies have also been proposed, such as the single vector current controller with feed forward negative-sequence grid-side voltage [16], dual vector current controller (DVCC) in a positive and negative synchronously rotating frame [17], and proportional-resonant controllers in a two-phase stationary frame [18,19]. However, their main concerns are how to eliminate the DC-link fluctuation or to decrease the negative fault current. The inverters' maximum current limit, which inevitably exists under severe faults [20], is not still considered in these strategies.

In revealing the IIREG fault characteristic, most studies adopt the simulation methods. Ref. [21,22] analyzes the fault current contribution based on the IIREG' simulation models. In the simulation test, the IIREG adopts the normal grid-connected control strategies. The research result cannot accord with the FRT requirement. Further, Ref. [23–25] studies the fault current characteristics of IIREGs by considering the FRT control strategy. However, this FRT control strategy is not available under the asymmetrical grid faults. The mentioned above research results depend on the designated control strategy and show diversity due to different control strategies.

At the same time, in some references the IIREGs' fault current is also derived based on the designated control strategies. Consequently, the fault current expressions are not universal and cannot been applied for relay setting calculation. Ref. [26,27] proposes a controlled current source model for the IIREG system. In the model, its current magnitude depends on the terminal voltage and the DC-side active power. It is assumed that the reactive power supply is equal to zero after a grid-side fault [28,29]. The assumption does not accord with the reactive power requirement of FRT codes. Ref. [30,31] deduce the fault current expression with the effect of the FRT control strategy. However, the inverters' current limit is not considered in the FRT control strategy and the fault current expression is suitable only for the assigned FRT control.

In this paper, in order to derive a consolidated expression of the fault current, the fault characteristics of IIREGs are theoretically analyzed. Since the fault characteristics are related to the FRT control strategy, the improved FRT strategy is developed to solve the problems in the existing literature. The remaining paper is organized as follows: Section 2 discusses the improved FRT control strategy under a severe fault. In Section 3, the characteristics of different frequency fault current from IIREGs are theoretically analyzed. In Section 4 the mathematical expression of the fundamental fault current is derived and verified based on the experimental test bench. Conclusions are drawn in Section 5.

2. Main Circuit Model and the FRT Control Strategy of Inverter-Interfaced Generators

2.1. Main Circuit Model

This section presents the main circuit model of IIREGs, which serve as the basis for both the design of the FRT strategy and the analysis on the fault current contribution. The integration topology of an IIREG is shown in Figure 1. Under the faults, the mathematical model on the AC-side of the grid-connected inverter can be expressed as Equation (1).

$$\begin{cases} \mathbf{E}_{dq}^{p} = Ld\mathbf{I}_{dq}^{p}/dt + (R + j\omega L)\mathbf{I}_{dq}^{p} + \mathbf{V}_{dq}^{p} \\ \mathbf{E}_{dq}^{n} = Ld\mathbf{I}_{dq}^{n}/dt + (R - j\omega L)\mathbf{I}_{dq}^{n} + \mathbf{V}_{dq}^{n} \end{cases} \tag{1}$$

where the subscripts p and n indicate the positive- and negative-sequence components, respectively. $\mathbf{E}_{dq}^{k}$, $\mathbf{I}_{dq}^{k}$ and $\mathbf{V}_{dq}^{k}(k = p, n)$ denote the space vectors of the grid-side voltage, output current, and AC-side voltage of the inverter, respectively. Here, $R = R_1 + R_2$, and $L = L_1 + L_2$. R_1 and L_1 are the inverter-side resistance and inductance of the inductor-capacitor-inductor (LCL) filter, respectively, and R_2 and L_2 denote the grid-side ones of the LCL filter. ω is the grid frequency.

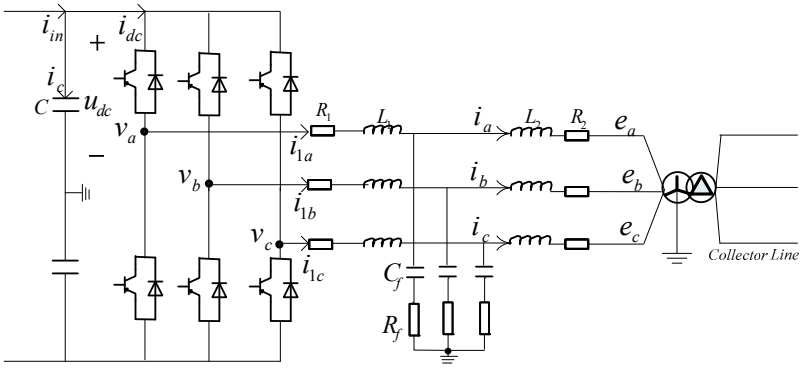

Figure 1. Main circuit of an IIREG.

The instantaneous active and reactive output power of the IIREGs during severe faults can be described as Equation (2). Here, we note that reactive power Q_{out} is different from that defined in classical steady-state circuit theory [32], i.e.,

$$\begin{cases} P_{out} = \text{real}(1.5(e^{j\omega t}\mathbf{E}_{dq}^{p} + e^{-j\omega t}\mathbf{E}_{dq}^{n})conj(e^{j\omega t}\mathbf{I}_{dq}^{p} + e^{-j\omega t}\mathbf{I}_{dq}^{n})) = 1.5(P_{out}^{o} + P_{out}^{c}\cos 2\omega t + P_{out}^{s}\sin 2\omega t) \\ Q_{out} = \text{real}(1.5(-je^{j\omega t}\mathbf{E}_{dq}^{p} + je^{-j\omega t}\mathbf{E}_{dq}^{n})conj(e^{j\omega t}\mathbf{I}_{dq}^{p} + e^{-j\omega tn}{}_{dq})) = 1.5(Q_{out}^{o} + Q_{out}^{c}\cos 2\omega t + Q_{out}^{s}\sin 2\omega t) \end{cases} \tag{2}$$

where the superscript c, s and o denote the cosine, sine and average components. P_{out}^{c}, P_{out}^{s}, Q_{out}^{c}, and Q_{out}^{s} are not equal to zero after asymmetrical faults. They can be represented in terms of the grid-side voltage and output current as:

$$\begin{cases} P_{out}^{o} = e_d^p i_d^p + e_q^p i_q^p + e_d^n i_d^n + e_q^n i_q^n \\ Q_{out}^{o} = e_d^p i_q^p - e_q^p i_d^p - e_d^n i_q^n + e_q^n i_d^n \\ P_{out}^{\mathrm{c}} = e_d^p i_d^n + e_q^p i_q^n + e_d^n i_d^p + e_q^n i_q^p = Q_{out}^{\mathrm{s}} \\ P_{out}^{\mathrm{s}} = e_d^p i_q^n - e_q^p i_d^n - e_d^n i_q^p + e_q^n i_d^p = -Q_{out}^{\mathrm{c}} \end{cases} \tag{3}$$

Equation (3) shows that P_{out}^{c} has the same absolute value as Q_{out}^{s}, as well as P_{out}^{s} and Q_{out}^{c}. Therefore, by nullifying the oscillating components of the instantaneous active power, the instantaneous reactive power is also flattened.

Similarly, the instantaneous active power P_{out}^{1} and reactive power Q_{out}^{1} at the inverter pole can be represented by $\mathbf{V}_{dq}^{k}$ and $\mathbf{I}_{dq}^{k}$. By neglecting the unbalanced voltage drop in the LCL filter, P_{out}^{1} and Q_{out}^{1} are almost equal to P_{out} and Q_{out}, respectively. Moreover, P_{out}^{1} is closely linked to the DC-link input power P_{in} as:

$$P_{in} = 2CU_{dc}dU_{dc}/dt + P_{out}^{1} \tag{4}$$

where C and U_{dc} stand for the DC-link capacitance and voltage, respectively. During asymmetrical faults, the two-times frequency component of active power P_{out}^{1} yields a 100-Hz DC-link voltage ripple. Such a pulsating voltage causes detrimental effects on the control system of the grid-tied inverter and even leads to tripping off of the IIREG from the grid.

2.2. Improved FRT Control Strategy

To ensure that the IIREGs ride through the asymmetrical faults, the control strategy based on DVCC for the grid-tie inverter has been widely used. The strategy uses two control loops: four faster inner parallel current loops and a slower outer DC-link voltage control loop. The inner loops regulate the positive and negative output currents of the IIREG injected to the grid, whereas the outer loop acts as a supervisory controller and determines the average active power reference P_o in the inner controller. The control structure enables flexible control of the output current of the IIREGs. Generally, any of the two control targets expressed in Equation (5) can be achieved:

$$\begin{cases} [P_{out}^{o}{}^{*}, Q_{out}^{o}{}^{*}, P_{out}^{s}{}^{*}, P_{out}^{c}{}^{*}] = [P_o, Q_o, 0, 0] \\ [P_{out}^{o}{}^{*}, Q_{out}^{o}{}^{*}, i_d^{n*}, i_q^{n*}] = [P_o, Q_o, 0, 0] \end{cases} \tag{5}$$

where the superscript * denotes the reference value. In Equation (5), the average reactive power Q_0 can be set to meet the FRT requirement. According to Equations (5) and (3), current references i_d^{p*}, i_q^{p*}, i_d^{n*}, and i_q^{n*} can be calculated. In Equation (5), the first sub-expression is to suppress the oscillation of the DC-link voltage by setting $P_{out}^{s}{}^{*} = 0$ and $Q_{out}^{s}{}^{*} = 0$ (Control Goal 1), whereas the second one is to eliminate the negative-sequence current through the inverter ($i_d^{n*} = i_q^{n*} = 0$) (Control Goal 2). Control Goal 1 easily leads to dangerous high current through grid-tie inverter under the severe faults. Control Goal 2 may cause the oscillations in the DC-link voltage. Control Goal 1 and Control Goal 2 are suitable only for distant asymmetrical faults.

To enhance the FRT ability of IIREGs, an improved control strategy is studied in this section, as shown in Figure 2. Compared with the conventional control strategy based on DVCC, the developed FRT strategy can take care of both the inverters' allowable current limit and DC-link voltage fluctuation. A novel current limiter is designed to deal with the inverter over-current problem, and a controller for the DC chopper is improved to insure the DC-link voltage within its acceptable value. The corresponding details are explained next.

The key idea of the novel current limiter is to fully utilize the control ability of the grid-tie inverter within its allowable current limit. The current limiter is activated in the event that the instantaneous maximum current $I_{\max}$ through inverter is greater than the inverter's current constraint $I_{\lim}$. With the limiter activation the positive- and negative-sequence current references are reset as:

$$i_j^{k*\prime} = i_j^{k*} I_{\lim} / I_{\max} = \alpha i_j^{k*} \tag{6}$$

where subscript j denotes the d- or q-axis component. α is a scalar coefficient of the current limiter, and it is less than 1 if $I_{max} > I_{lim}$. I_{max} can be expressed as $I_{max} = \max(I_{am}, I_{bm}, I_{cm})$. I_{am}, I_{bm}, and I_{cm} are the magnitudes of instantaneous currents i_a, i_b, and i_c through the inverter. The instantaneous currents are obtained as follows:

$$\begin{cases} i_a = |\mathbf{I}_{dq}^p| \sin(\omega t + \theta^p) + |\mathbf{I}_{dq}^n| \sin(\omega t + \theta^n) \\ i_b = |\mathbf{I}_{dq}^p| \sin(\omega t - 2\pi/3 + \theta^p) + |\mathbf{I}_{dq}^n| \sin(\omega t + 2\pi/3 + \theta^n) \\ i_c = |\mathbf{I}_{dq}^p| \sin(\omega t + 2\pi/3 + \theta^p) + |\mathbf{I}_{dq}^n| \sin(\omega t - 2\pi/3 + \theta^n) \end{cases} \quad (7)$$

where $|\mathbf{I}_{dq}^k|$ $(k = p, n)$ represent the amplitudes of the positive- and negative-sequence current vector references, respectively. $\theta^p = \arctan(i_q^p / i_d^p)$, and $\theta^n = 2\pi\text{-}\arctan(i_q^n / i_d^n)$ are the phase angles of the positive- and negative-sequence current vectors.

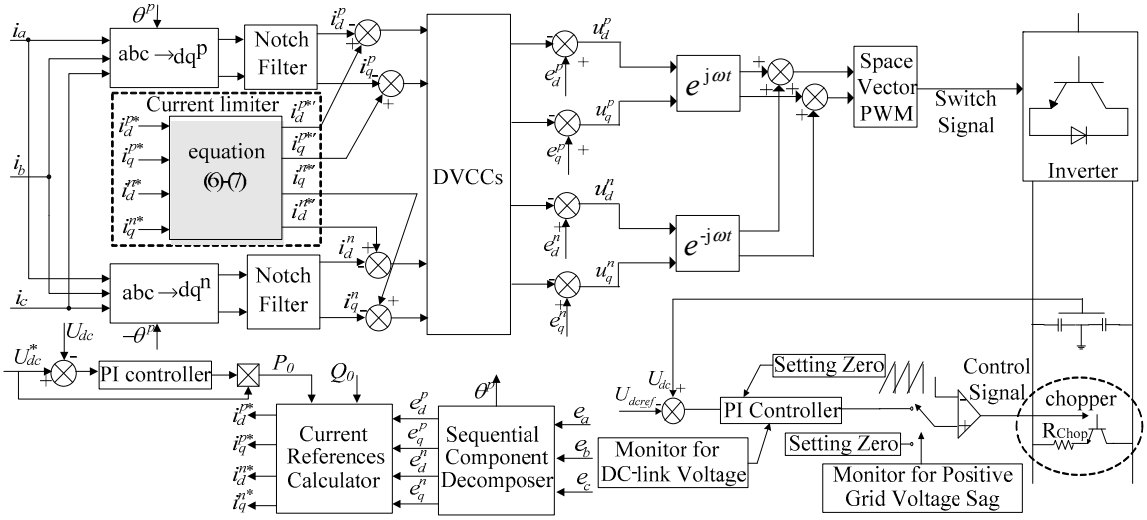

Figure 2. The improved FRT strategy.

By substituting Equation (6) into Equation (5), we find that the oscillating DC-link voltage with Control Goal 1 or negative-sequence current through the inverter with Control Goal 2 can still be eliminated even though the current limiter is activated. In this paper, Control Goal 1 is chosen in order to keep the DC-link voltage within an acceptable range.

Due to the activation of the current limiter, the active power through the inverter is limited. However, the DC-link input power from the wind turbine or solar cell remains unchanged. Consequently, the imbalance between the DC-link input power and output power may cause a dangerous rise in the DC-link voltage. To prevent a DC-link overvoltage, the DC-link chopper is engaged. Although the chopper circuit is widely used in practical wind and solar power systems, its control strategy has not yet been significantly explored in the existing literatures. The control is crucial to solve the DC-link overvoltage problem. The design of such a control system is also one of the novel results of this paper.

Figure 2 shows that the controller for the DC-link chopper is automatically enabled once the positive-sequence component of the grid-side voltage drops below a critical threshold (0.9 per unit (p.u.)). The proportional-integral (PI) controller is employed to timely regulate the surplus power in the DC link and to prevent the DC-link overvoltage risks. To shorten the chopper response time, the integral part of PI controller is activated and reset to the most recent measurement of the DC-link voltage at the time when the DC-link voltage is greater than 1.05 p.u. Moreover, the reference of the PI controller is equal to that of the outer PI controller in the DVCC control loop, which enables the IIREGs to immediately return to the pre-fault state after fault clearance.

With the designed controller for the DC-link chopper, the DC-link voltage can be regulated within its acceptable value. As mentioned above, the current limiter can restrict the current through inverters within the maximum allowable currents. Hence, the improved FRT control strategy can solve both the inverter over-current problem and DC-link over-voltage problem. To test the improved FRT control strategy, the hardware-in-the-loop experiments have been conducted based on the test rig shown in Figure 3.

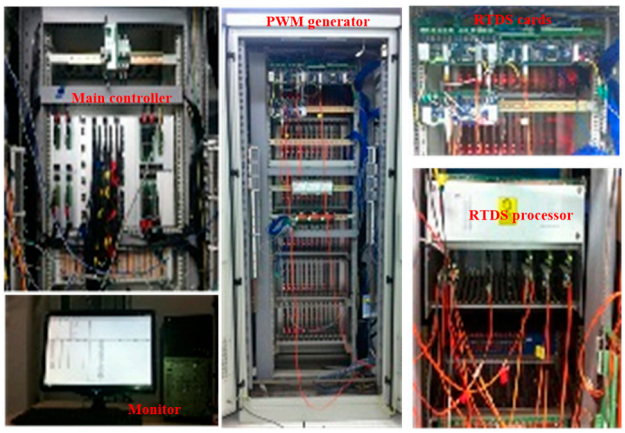

Figure 3. Physical layout of the experimental test bench.

As shown in Figure 7, the test rig consists of main controller, pulse-width-modulated (PWM) generator, real-time digital simulator (RTDS), and monitor. These hardware performance indicators are devised according to the corresponding international standards or the marketable product's design criteria. In the test rig, the main controller is basically composed of the digital signal processor (DSP)/field programmable gate array (FPGA) combined control boards. It can implement the control and protection algorithms of the IIREG system based on the modular programming method. The algorithm codes can be flexibly modified. The PWM generator is used for generating the electrical firing signals for the inverters. RTDS simulator is employed to simulate the main circuit of power grid with the tested IIREG. Monitor can be utilized for starting and stopping the IIREG system, so as to reset the control and protection parameters, and so on.

Based on the experimental test rig, the two cases are as follows.

The first case is to verify the asymmetrical FRT ability of the IIREGs. The IIREG's parameters are shown in the Appendix A. It is assumed that a two-line-to-ground fault (TLGF) occurs between phase-a and b in the collector line at t = 0.6 s and lasts for 0.65 s. The fault causes a 96% imbalance in the grid-side voltage ($\mathbf{E}_{dq}^{p}$ = 0.57 p.u.; $\mathbf{E}_{dq}^{n}$ = 0.55 p.u.). Figure 4 shows the actual test results with the conventional DVCC strategy and improved control strategy. From Figure 4, when the conventional DVCC strategy is applied, during the fault the DC-link voltage and the current through inverter exceed their allowable scopes. The IIREG becomes unstable after the fault. However, the proposed FRT strategy assures the stable operation of IIREG. Both the current through inverter and the voltage in the DC link are kept within their acceptable limits. The result indicates that the proposed control strategy can effectively enlarge the feasible region of riding through the asymmetrical faults.

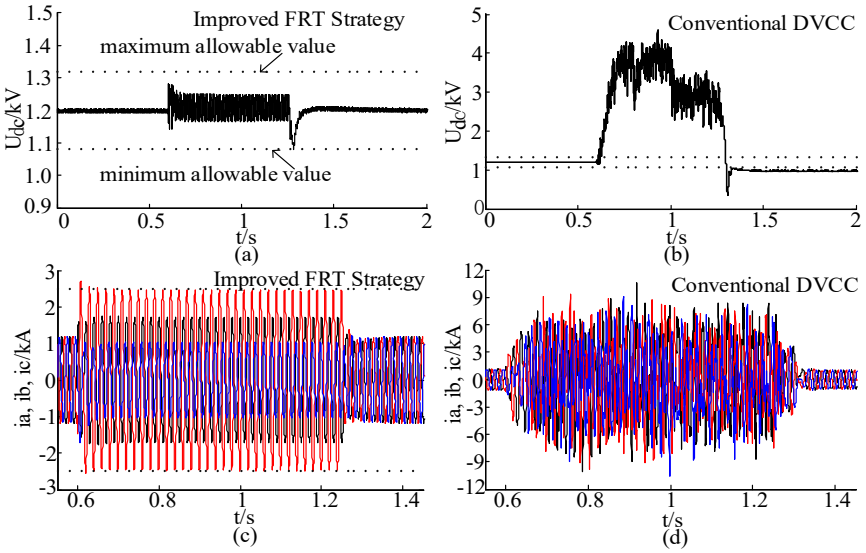

Figure 4. Asymmetrical fault test results with the improved FRT strategy and conventional DVCC strategy; (**a**) The DC-link voltage with the improved FRT strategy; (**b**) The DC-link voltage with conventional DVCC strategy; (**c**) The current through inverter with the improved FRT strategy; (**d**) The current through inverter with conventional DVCC strategy.

The second case is to test the symmetrical FRT ability of the IIREGs. It is assumed that a fault occurs in the collector line at $t = 0.6\ s$ and lasts for $0.65\ s$. After the fault, grid-side voltage falls from 1.02 p.u. to 0.2 p.u. Figure 5 shows the test results with the improved control strategy and conventional FRT strategy.

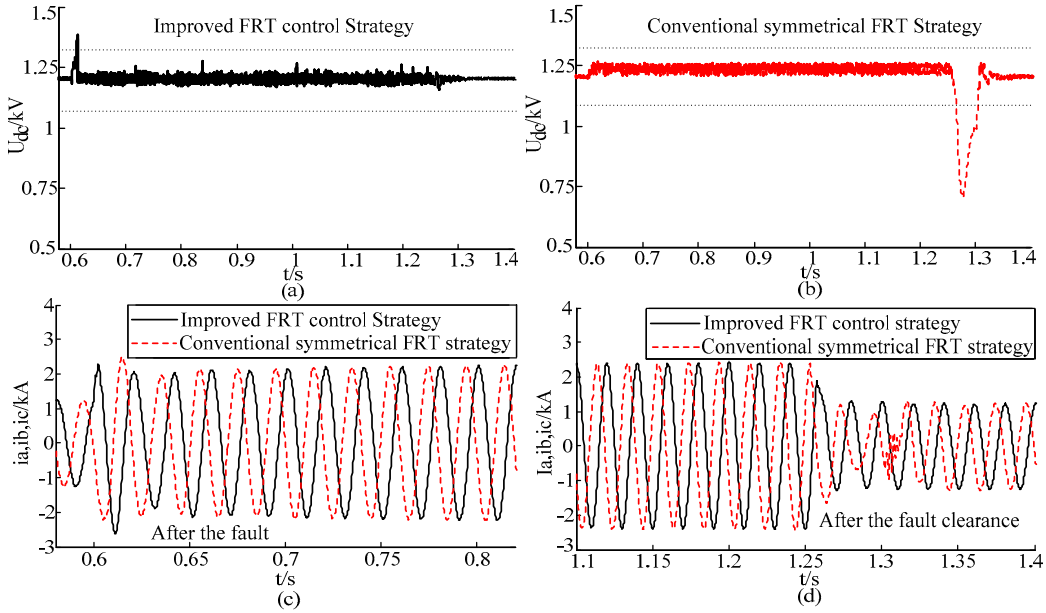

Figure 5. Symmetrical fault test with the improved FRT strategy and conventional control strategy; (**a**) The DC-link voltage with the improved FRT strategy; (**b**) The DC-link voltage with conventional FRT strategy; (**c**) The current through inverter with the improved FRT strategy; (**d**) The current through inverter with conventional FRT strategy.

In Figure 5, the difference between the improved control strategy and conventional strategy is the designed controller for DC-link chopper. Moreover, the conventional strategy can only limit the

balanced current through inverter. From Figure 5, with the effect of two control strategies both DC-link voltage and the current through inverter are within their allowable values after and during the fault. However, once the fault is cleared, the DC-link voltage is changed greatly (from 1.24 kV to 0.71 kV) with the conventional FRT strategy in Figure 5b. As a result, at t = 1.32 s the current through inverter is regulated into a steady-state value in Figure 5c. By comparison, with the effect of improved control strategy, after the fault clearance DC-link voltage and the current through inverter can be quickly restored into their corresponding pre-fault values.

In the test cases, it was established that the proposed FRT strategy can help the IIREGs to ride through the asymmetrical faults that causes a 96% imbalanced grid-side voltage ($|\mathbf{E}_{dq}^{n}|/|\mathbf{E}_{dq}^{p}|$). At the same time, the proposed strategy can also help the IIREGs to ride through the severe symmetrical faults.

3. Theoretical Analysis for IIREGs' Fault Current Characteristics

Due to the instantaneousness of the fault initiation, a transient condition in IIREGs inevitably exists. Different from the CSGs, the transient characteristics of IIREGs are more complicated with multi-factor coupled effects. These factors include not only the integration circuit of IIREGs, but also the FRT control strategy, its controller parameters, and its control goals. As a result, the theoretical study on fault current characteristics of the IIREGs becomes difficult.

In this section, the characteristics of different frequency current from IIREGs are theoretically discussed under the faults. It is commonly known that grid-side voltage of IIREGs is suddenly changed after a fault. The voltage variation can be viewed as the summation of a set of different frequency trigonometric functions. With the impact of different frequency voltages, the output currents of IIREGs include high-frequency and low-frequency components (near the fundamental frequency).

Figure 6a shows the connection circuit of a grid-tied IIREG. The topology is typical, and it has been widely used for the Chinese power grid with the REGs. It is assumed that a fault occurs at the point of common coupling (PCC). Figure 6b shows the flowing path of high frequency fault currents. The currents flow from the fault location into the filter of IIREGs. They are independent of the IIREGs' control. They are related with the passive circuits, i.e., local transformer(s), overhead lines, and underground cables of the collector system, filter, and so on.

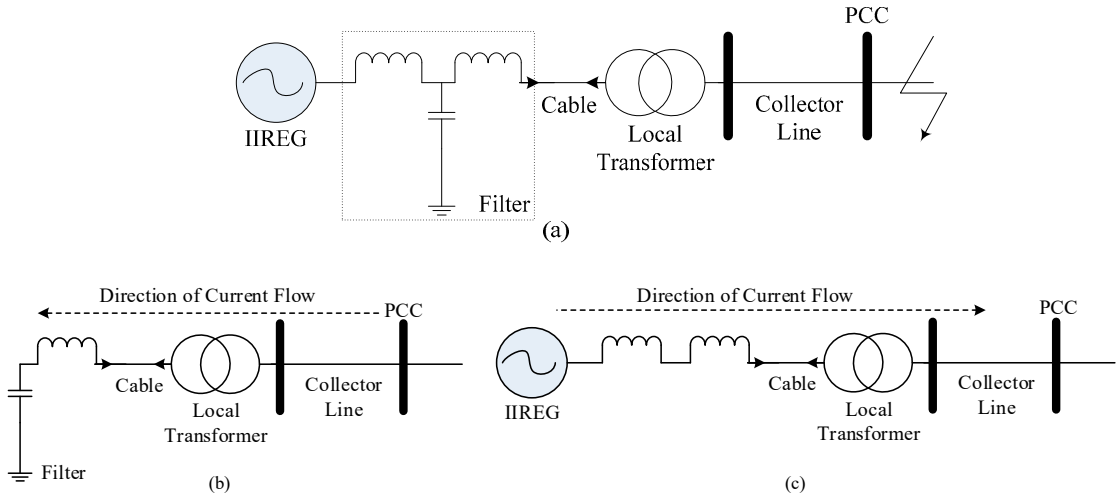

Figure 6. The path of high- and low-frequency fault currents from IIREG; (**a**) Integration topology of an IIRGR; (**b**) The path of the high-frequency fault current; and (**c**) The path of the low-frequency fault current.

As shown in Figure 6c, low frequency components flow from the IIREG into the fault location. They are mainly determined by the IIREGs' control, i.e., the FRT control schemes, its controller parameters, and its control goals. However, they are irrelevant to the aforementioned passive circuits.

Moreover, although the IIREGs' control loops may also generate high-frequency currents due to the fault initiation, the currents flow into the ground through the capacitor of the LCL filter from the IIREG generation units. Thus, the high-frequency currents are non-existent, viewed from the PCC.

Next, the characteristics of different frequency fault currents are analyzed theoretically. To describe the high-frequency currents, the equivalent model of IIREG's passive network is built. Development of the model includes the following steps [33].

Step (1): At PCC, disconnect the IIREG generation units at the AC-side terminals of the corresponding converters.

Step (2): Inject a current signal into the IIREG system. The current signal is the summation of a set of sinusoidal current components at unity amplitudes, zero phase angles, and discrete frequencies that cover a specified frequency bandwidth and specified frequency steps. The frequencies of these currents cover the desired frequency bandwidth. The frequency bandwidth is specified based on the type of EMT studies, e.g., 0 to 50 kHz.

Step (3): Deduce the IIREG terminal voltage. This voltage represents the IIREG equivalent impedances at the frequencies of the injected currents.

Step (4): Decompose the voltage, based on the Fourier analysis, into its components at the frequencies of the injected current components.

Step (5): Fit a rational function of the form:

$$Y(s) = f(s) = \sum_{n=1}^{N} \frac{c_n}{s - a_n} + sh + d \tag{8}$$

to the deduced results of Step (4). In Equation (8), residues c_n and poles a_n can be either real or complex numbers, while d and h are real and can be obtained based on several methods, e.g., the vector fitting method.

According to the aforementioned steps, the equivalent model shown in Equation (8) can be built for the system shown in Figure 6b. Their related parameters are listed in the Appendix A, which are mostly based on the information from industries and the literature. Table 1 shows the residues and poles of the obtained rational function and its time-domain performance indicators.

Table 1. Parameters of the rational function for the IIREG's passive network.

Residues		Poles		Time-Domain Performance Indicators	
Real Part	**Imaginary Part**	**Real Part**	**Imaginary Part**	**Decay Time/ms**	**Oscillating Frequency/Hz**
53.7	2.66	−157.58	±31,628.98	19.04	5033.91
1.68	0.074	−108.59	±2054.53	27.63	326.99
240	143	−18,968.83	±120,144.69	0.16	19,121.62
184	0	−1,931,778.48	0.00	0.00	0.00
−450	0	−5,804,483.19	0.00	0.00	0.00

Based on the conjugate poles in Table 1, the decay time and oscillating frequency of the high-frequency fault current can be calculated. From Table 1, the decay time of 327 Hz current component is about 19.04 ms. And the attenuation time of 5034 Hz current component is approximately 27.63 ms. Other frequency current components are reduced at a very fast rate, so their reduction time can be ignored.

After the high-frequency current decays to zero, the remaining component is the fundamental frequency current. This can be calculated based on the fundamental admittance. According to the equivalent model of IIREG's passive network, the fundamental positive and negative admittance $Y_1 = Y_2 = 4.0 \times 10^{-5} + j8.9 \times 10^{-4}\ Si$ are very small. Thus, the fundamental current is small through the IIREG's passive circuits during the fault.

Figure 7 shows the instantaneous phase-a current from the practical IIREG and its passive circuit when the fault occurs at $t = 0.113\ s$. From Figure 7a, the high-frequency currents from the passive circuit

decay last for only 18.8 ms during the fault. By comparing Figure 7a with Figure 7b, the fundamental current amplitudes through the passive circuit and from the overall IIREG are respectively equal to 0.00062 kA and 0.04613 kA during the steady-state fault periods. The former current is 1.34% that of the latter.

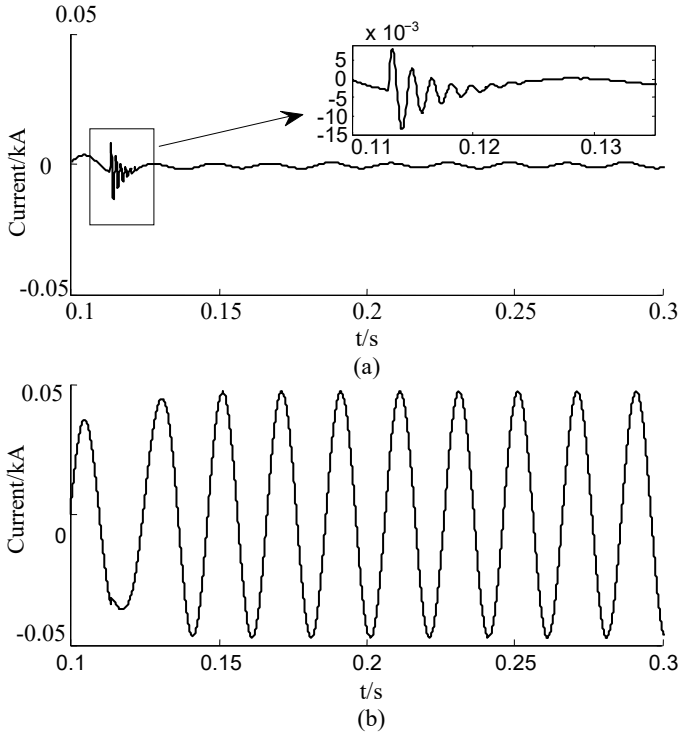

Figure 7. Instantaneous phase-a current when the fault occurs at t = 0.113 s; (**a**) Current through the passive circuit; and (**b**) Current from the practical IIREG.

Therefore, high-frequency fault currents provided by IIREGs last only for 1–2 cycles. The currents are decided by the passive circuits of IIREGs' integration topology. The fundamental fault currents always exist, and they are affected mainly by the IIREGs' control system. In the following sections, the characteristics of fundamental fault currents are discussed.

4. Mathematical Expression of Fundamental Fault Current

In the section, the fundamental fault current expression of IIREGs is derived on the basis of the proposed asymmetrical FRT strategy. It can provide a basis for relay setting calculations of the power grid connected with a large number IIREGs.

4.1. Derivationfor Fundamental Fault Current

Due to the fast response of the gird-connected inverter controller, the IIREGs can quickly reach the steady state under fault conditions. During faults, the steady-state behavior of the IIREGs is strongly dependent on the FRT control. Combining Equations (3) with (5), the positive- and negative-sequence components of the fundamental fault current from the IIREGs with Control Goal 1 are expressed as follows (in a p.u. system):

$$\begin{cases} I_m^p = |\mathbf{I}_{dq}^p| = E_m^p S_o / (E_m^{p\,2} - E_m^{n\,2}) = S_o / (\gamma E_m (1-\beta^2)) \\ I_m^n = |\mathbf{I}_{dq}^n| = E_m^n S_o / (E_m^{p\,2} - E_m^{n\,2}) = \beta S_o / (\gamma E_m (1-\beta^2)) \end{cases} \quad (9)$$

where E_m^p and E_m^n are the positive- and negative-sequence amplitudes of grid-side voltage. γ reflects the drop coefficient of the positive-sequence grid-side voltage. $\beta = E_m^n/E_m^p$ denotes the imbalance degree of grid-side voltage. E_m is the rated voltage magnitude. S_o represents the apparent power injected into the grid. From Equation (9), the IIREGs can generate the negative-sequence currents. The current characteristic is different from that of the CSGs.

By taking into account the deliverable power limit through the inverter, the apparent power S_o derived using the proposed control strategy is expressed as:

$$S_o = \begin{cases} \sqrt{{P_o}^2 + Q_o^2} & \alpha \geq 1 \\ \alpha\sqrt{{P_o}^2 + Q_o^2} & \alpha < 1 \end{cases} \tag{10}$$

In addition, the three phase current amplitudes I_{am}, I_{bm}, and I_{cm} through the inverter can be calculated as:

$$\begin{cases} I_{am} = \sqrt{{I_m^p}^2 + {I_m^n}^2 + 2I_m^p I_m^n \cos(\theta^p - \theta^n)} \\ I_{bm} = \sqrt{{I_m^p}^2 + {I_m^n}^2 + 2I_m^p I_m^n \cos(\theta^p - \theta^n - 4\pi/3)} \\ I_{cm} = \sqrt{{I_m^p}^2 + {I_m^n}^2 + 2I_m^p I_m^n \cos(\theta^p - \theta^n + 4\pi/3)} \end{cases} \tag{11}$$

where phase angles θ^p and θ^n are, respectively, derived as:

$$\begin{cases} \theta^p = \tan^{-1} k_s \\ \theta^n = 2\pi - \tan^{-1}((-k_s + k_u)/(1 + k_s k_u)) \end{cases} \tag{12}$$

where $k_s = Q_o/P_o$ and $k_u = e_q^n/e_d^n$. The phase-angle difference θ_i is expressed as:

$$\theta_i = \theta^p - \theta^n = \tan^{-1} k_u - 2\pi \tag{13}$$

The angle θ_i is closely related with negative-sequence grid-side voltage. Given the positive and negative current amplitude $\mathbf{I}_m^k (k = p, n)$, the three phase current peaks vary periodically with θ_i. If θ_i is equal to 0, $3\pi/4$, or $5\pi/4$, the current magnitude in phases a, b, or c is, respectively, the largest. The peak is equal to the magnitude sum of the positive- and negative-sequence current vectors.

By substituting Equations (10) and (13) into Equation (11), the three phase current amplitudes is also expressed as:

$$\begin{cases} I_{am} = S_o\sqrt{1 + \beta^2 + 2\beta\cos\theta_i}/(\gamma E_m(1 - \beta^2)) \\ I_{bm} = S_o\sqrt{1 + \beta^2 + 2\beta\cos(\theta_i - 4\pi/3)}/(\gamma E_m(1 - \beta^2)) \\ I_{cm} = S_o\sqrt{1 + \beta^2 + 2\beta\cos(\theta_i + 4\pi/3)}/(\gamma E_m(1 - \beta^2)) \end{cases} \tag{14}$$

From Equation (14), it is found that the short-circuit current provided by IIREGs is determined by two factors. The one is closely related with the apparent power delivered to grid and the inverter's ampere constraint. The power is determined by FRT control goal that is a fixed value for the specified grid code. The other is the amplitudes and angles of positive and negative sequence grid-side voltage vectors. These voltage vectors depend on both the equivalent short-circuit parameters of a connected grid and the grid fault conditions. In fact, the equivalent parameters and the fault conditions should be given from the perspective of the study on the relay protection. Thus, the steady-state short-circuit current expression of IIREGs as shown in Equation (14) is independent of the inverter's controllers and its parameters. The fault current values can be obtained without knowing the inverter's control strategies.

4.2. Verification

To verify the fault current expression, the detailed test model is built as shown in Figure 8. The topology is typical, and it has been widely used for the transmission grid with the large-scale IIREGs. The related parameters are listed in the Appendix A, which are mostly based on the information from industries and the literature.

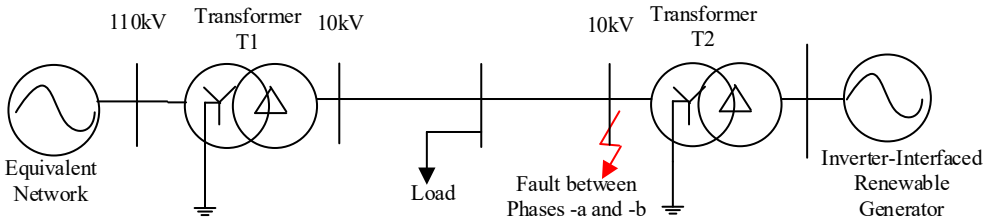

Figure 8. Test bed system with a inverter-interfaced renewable energy generator.

Based on the experimental model in Figure 8, the tests was done using the hardware-in-the-loop as shown in Figure 3. At the same time, according to Equation (14) the fault currents from the IIREG were calculated using the MATLAB software. Table 2 shows the comparison results with different active and reactive power commands. Here, it is assumed that a two-line-to-ground fault (TLGF) occurs between phases-a and -b in bus C at t = 0.6 s and lasts for 0.65 s. Before the fault the IIREG operates at its rated state, and its output current is approximately 1.245 kA.

Table 2. Fault currents of IIREGs with different active and reactive power commands.

	P_o = 1 p.u. Q_o = 1 p.u.			P_o = 1 p.u. Q_o = 0.1 p.u.			P_o = 0 p.u. Q_o = 1 p.u.		
Current Amplitude	I_{am}	I_{bm}	I_{cm}	I_{am}	I_{bm}	I_{cm}	I_{am}	I_{bm}	I_{cm}
Test Results	1.81 kA	2.49 kA	1.25 kA	2.43 kA	2.49 kA	0.31 kA	1.50 kA	2.49 kA	1.55 kA
Calculation Results	1.76 kA	2.45 kA	1.19 kA	2.46 kA	2.46 kA	0.33 kA	1.48 kA	2.44 kA	1.60 kA
Relative Error	−2.76%	−1.60%	−4.80%	1.23%	−1.22%	6.45%	−1.33%	−2.05%	3.22%

From Table 2, it is found that the difference between the calculation results and test results is very small. The maximal error value reaches 6.45%, only when the desired powers of grid-tie inverter are P_o = 1 p.u., Q_o = 0.1 p.u. Under the other power commands, the errors are less than 5%. It is indicated that the proposed IIREG's fault current expression as shown in Equation (14) has high accuracy.

Moreover, compared with the calculated or tested fault currents results, it is found that the relationship among the three-phase current amplitudes is different withvarious active and reactive power commands. With different cases the faulty phase-b current magnitude reaches the inverter's ampere constraint (2 p.u., 2.49 kA) due to the current limiter activation, but the relationship between the phase-a and -c current amplitudes is affected by the actual real and reactive power commands. Therefore, the active and reactive power commands for grid-tie inverter affect not only the amplitude values of IIREG's fault currents but also the relationship of the three-phase current amplitudes. The fault current characteristic of IIREG is different from that of synchronous generators. The fault current of synchronous generators is mainly influenced by the machine equivalent impedance. The impedance is not associated with the generators' active and reactive injections.

5. Conclusions

In order to reveal the IIREGs' fault current characteristics and further deduce the universal fault current calculation model, it is important to study on the FRT control strategy for the IIREGs. Hence, in this paper an advanced FRT control strategy is firstly proposed. In the control strategy, a novel current limiter is designed for restricting the current through inverter. Meanwhile, a controller for the DC-link chopper is improved to keep the DC-link voltage within its allowable value.

The hardware-in-the-loop test results indicate that the proposed strategy can effectively enlarge the feasible region of riding through the faults, including the severe asymmetrical faults (the imbalance of grid-side voltage is about 100%) and serious symmetrical faults (the drop coefficient of the grid-side voltage is approximately 20%).

Based on this, the characteristics of different frequency fault currents from IIREGs are theoretically analyzed after and during the faults. It is revealed that the respective affecting factors of high frequency and fundamental frequency fault current are independent. The high currents are determined mainly by the IIREGs' passive circuits, i.e., local transformer(s), overhead lines, and underground cables of the collector system, filter, and so on. The fundamental fault currents are closely related with FRT goals and the inverter' ampere constraint. The high currents last only for 1~2 cycles after the faults, whereas the fundamental fault currents always exist.

Further, the fundamental fault current calculation model of IIREGs is derived. The deduced short-circuit current expression is determined by two factors. The one is closely related with the apparent power delivered to grid and the inverter's ampere constraint. The apparent power is related only with the FRT control goal, independent of the FRT controller parameters. The FRT control goal is a known value for the specified grid code. The other factor is the grid-side voltage vectors. The voltages vectors can be obtained if the short-circuit equivalent parameters of a connected grid and the grid fault conditions are given. For the fault analyzing or relay setting calculating, the short-circuit parameters and the fault conditions should be treated as the known values. Thus, the fault current contributions from the IIREGs can be calculated without knowing their control strategies. The proposed fault current calculation model is useful for relay-setting calculations of the grid with a large number of IIREGs.

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Nomenclature

Subscript d	d-axis component
Subscript q	q-axis component
Superscript p	Positive sequence component
Superscript n	Negative sequence component
Superscript *	Reference value
Superscript o	Average component
Superscript c	Second harmonic cosine component
Superscript s	Second harmonic sine component
E	Grid-side voltage Vector
I	Output current Vector
e	Instantaneous grid-side voltage
i	Instantaneous output current
E_m	Grid-side voltage amplitude
γ	Voltage drop coefficient
β	Voltage imbalance degree
I_{m}	Output current amplitude
U	AC-side voltage Vector
U_{dc}	DC-link voltage
P_{out}	Active output power of the IIREG
Q_{out}	Reactive output power of the IIREG

P_{out}^1	Active power at the inverter pole
Q_{out}^1	Reactive power at the inverter pole
P_{in}	DC-link input power
P_0	Average reactive power Reference
Q_0	Average reactive power Reference
S_0	Apparent output power
$I_{\max}$	Instantaneous maximum current through inverter
I_{lim}	Inverter's current constraint
α	Scalar coefficient of the current limiter
θ^p	Positive-sequence current angle
θ^n	Negative-sequence current angle
θ_i	Angle difference between θ^p and θ^n
R_1	Inverter-side resistance of the LCL filter
R_2	Grid-side resistance of the LCL filter
ω	Grid frequency
C	DC-link capacitance

Appendix A

Transformer T_1 ratio n = 10.5/2.2 kV; transformer T_2 ratio n = 121/10.5 kV; the line length AB, BC is 5.5 km, 1.6 km; grid frequency ω = 50 Hz; grid-tie inverter: rated capacity S = 1.5 MW, rated current 1.245 kA, ampere constraint 2.49 kA; DC-link capacitor C = 4500 μF, DC-link voltage U_{dc} = 1.2 kV; LCL filter: L_1 = 1100 μH, L_2 = 123.55 μH, C_f = 200 μF, R_f = 0.2484 Ω; inner positive or negative current controller: proportional gain K_{iP} = 0.3285 p.u., integral time constant T_{iI} = 0.0175 p.u.; outer voltage controller: K_{vP} = 0.75 p.u., T_{vI} = 0.875 p.u.

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