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A New Topology of a Fast Proactive Hybrid DC Circuit Breaker for MT-HVDC Grids

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Abstract: One of the major challenges toward the reliable and safe operation of the Multi-Terminal HVDC (MT-HVDC) grids arises from the need for a very fast DC-side protection system to detect, identify, and interrupt the DC faults. Utilizing DC Circuit Breakers (CBs) to isolate the faulty line and using a converter topology to interrupt the DC fault current are the two practical ways to clear the DC fault without causing a large loss of power infeed. This paper presents a new topology of a fast proactive Hybrid DC Circuit Breaker (HDCCB) to isolate the DC faults in MT-HVDC grids in case of fault current interruption, along with lowering the conduction losses and lowering the interruption time. The proposed topology is based on the inverse current injection technique using a diode and a capacitor to enforce the fault current to zero. Also, in case of bidirectional fault current interruption, the diode and capacitor prevent changing their polarities after identifying the direction of fault current, and this can be used to reduce the interruption time accordingly. Different modes of operation of the proposed topology are presented in detail and tested in a simulation-based system. Compared to the conventional DC CB, the proposed topology has increased the breaking current capability, and reduced the interruption time, as well as lowering the on-state switching power losses. To check and verify the performance and efficiency of the proposed topology, a DC-link representing a DC-pole of an MT-HVDC system is simulated and analyzed in the PSCAD/EMTDC environment. The simulation results verify the robustness and effectiveness of the proposed HDCCB in improving the overall performance of MT-HVDC systems and increasing the reliability of the DC grids.

Keywords: DC Circuit Breaker (CB); DC Fault; Hybrid DC Circuit Breaker (HDCCB); Multi-Terminal VSC-HVDC (MT-HVDC) Grids

1. Introduction

Protection of the MT HVDC grids in case of a DC fault is vital to improve the reliability of the power system [1–3]. Conventional Voltage Sourced Converters (VSCs) are not capable of limiting or interrupting the current that flows following a DC-side fault. Also, the high power DC Circuit Breakers (CBs) are not commercially available. Therefore, opening the CB on the AC side is the only possible way to isolate the DC-side fault. Opening all the AC CBs to isolate/clear the DC-side fault in a DC grid with high capacity can lead to a large loss of power infeed. Therefore, clearing the DC fault within the DC grid by opening the AC CBs is practically impossible [4–6].

The consequence of a DC-side fault within an MT-HVDC grid is the sudden increase in the fault current, and that is due to the capacitive behavior of the HVDC grids and low resistance of the DC cables. The fault current should be interrupted in less than 20 ms to limit it within the acceptable levels [7]. Using AC-side CB in the point-to-point VSC-HVDC grids to interrupt the fault current leads to loss of the entire link. Adopting the same strategy for MT-HVDC grids and opening all the AC-side

CBs is a disruptive measure and can cause losing a large amount of power infeed. Therefore, it is mandatory to isolate only the faulty section of MT-HVDC grids. Two measures can be considered to deal with this issue: (1) Using fast-acting DC CBs at both ends of the DC-links. (2) Using fault-blocking converters to open the DC-links in case of a sudden increase in the DC fault current. Moreover, determining the exact location of the DC-side faults within MT-HVDC grids is difficult [8,9]. In the AC grids, impedance relays are used to determine the fault location. However, due to the low resistance of the DC cables compared to the impedance of the AC grids, it is impractical for the impedance relay to determine the fault location in a DC-link within its protective zone. Besides, distinguishing between the AC and DC-side faults is another major challenge in a DC protection system [10,11].

In order to interrupt the fault current, the AC CBs at the high voltage transmission levels require 4-5 cycles (within 80–100 ms). By creating zero crossings of the current, the AC CBs provide interruption with minimal arcing [12]. As there is no zero crossing of the current in DC, the conventional AC CBs are not useful to prevent large DC currents. To overcome this issue, a passive or active resonant circuit can be used to force the current zero crossing. The other way is to bypass or interrupt the fault current using semiconductor switches (Insulated-Gate Bipolar Transistor (IGBTs)), which considering the power losses, it is an expensive strategy. Due to the lack of reactance in the DC circuits, the rate of rise of fault current in the DC grids is higher than the AC grids [13,14]. Thus, the DC CBs must be capable of interrupting the fault currents faster than the AC CBs.

Different CB topologies are studied in the literature. The CBs can be categorized into three types: Mechanical Circuit Breakers (MCBs), Solid-State Circuit Breakers (SSCBs), and Hybrid Circuit Breakers (HCBs) [15,16]. The MCBs consist of the conventional AC CBs with a parallel circuit to generate a current zero crossing [17]. In both passive and active MCBs structures, due to the existence of the parallel circuit, the interruption time of the MCBs is long (30–50 ms), which is not suitable for VSC-HVDC systems. The SSCBs consist of several solid-state switches that can interrupt the fault current faster than the MCBs without the need for a current zero crossing [18–21]. Proper configuration of switches can lead to achieving the desired breaking current capability. To design a bidirectional CB, at least two switches are needed. The SSCBs are faster compared to the MCBs, but their on-state switching losses and total cost are high. The HCBs configurations are the results of the combination of MCBs and SSCBs [22]. The combinations are based on the operation time, breaking current capability, power losses, and total cost. The operation time and breaking current capability of the MCBs are low, but they are cheap. In contrast, the SSCBs are fast, but when it comes to a complicated configuration for the VSC-HVDC systems, they are expensive. Also, because of the existence of permanent resistance, the SSCBs have large power losses compared to the MCBs. The HCBs take advantage of both MCBs and SSCBs, such as fast current interruption and low power losses [23,24].

The first HCB [24], which was based on inverse voltage generation method, provided the advantages of both MCBs and SSCBs. It consisted of a semiconductor-based CB using IGBTs and a bypass circuit developed by the semiconductor-based load communication switches in series with an ultra-fast disconnector. Reducing the fault current level to zero is achieved by generating the arc voltage at a higher level than the source voltage. This topology has a short interruption time than the MCSs and lower on-state switching losses compared to the SSCBs. A detailed analysis of the operating modes of HCBs (reclosing and rebreaking) is performed in [16]. An accurate model considering the coordinated control of the four subunits (two semiconductor values along with two mechanical switches) and the opening and closing sequences of each subunit of the HCB is presented in [23]. This topology is not suitable for MT-HVDC grids, where the fault location is hard to find, and the switches in the auxiliary CB might damage due to the high rate of rise of current. To overcome this issue, a large number of semiconductor switches in the semiconductor-based CB branch is needed, which can increase the cost of implementation and relatively increase the on-state switching losses. To reduce the on-state switching losses of the HCBs, another topology considering multiple thyristors connected in series is proposed in [25]. In this topology, by injecting current stored in the capacitor with the initial charge, a current zero crossing can be generated. The main issue with this topology is the high on-state switching losses

because of the existence of IGBT in the main CB. Moreover, the fault interruption time is increased due to the transferring the fault current from the CB to the auxiliary CB. Besides, using an external power supply to charge the capacitor might lead to an increase in the costs of implementation. This topology provides the bidirectional fault current interruption, but reclosing and rebreaking capabilities of the HCBs is not considered. The topology of the HCBs presented in [26] is provided reclosing and rebreaking capabilities, as well as bidirectional fault current interruption. Reclosing and rebreaking capabilities have prevented the interruption of the power to the connected AC systems, and the auxiliary power source is used to charge the capacitor. Although the polarity of the capacitor can change according to the direction of fault current, it might have delay time to interrupt the fault and consequently, increase of the fault current magnitude.

As MT-HVDC systems can control the active and reactive power independently and in both directions [27], and do not require the installation of separate Flexible AC Transmission System (FACTS) devices, it is necessary to investigate a proper Hybrid DC Circuit Breaker (HDCCB) for MT-HVDC systems with capabilities of reclosing and rebreaking, as well as bidirectional fault current interruption. A new topology of the HDCCB to solve the above-mentioned issues is proposed.

The major contributions of this paper are as follows:

- The proposed topology of the HDCCB is based on the switching technique to minimize the costs of implementation and on-state switching losses, as well as interrupting the fault current in both directions. Also, in this topology, the polarity of the capacitor is based on the direction of fault current, which would lead to reducing the interruption time. Hence, it can be used in MT-HVDC systems.
- The proposed topology has reclosing and rebreaking capabilities without the need for an external power supply, which leads to reducing the overall cost.
- Improving the fault tolerance capability by increasing the maximum breaking current 0.25% compared to the conventional HDCCB, while having approximately the same total dissipated energy of the surge arrestor in the DC CB, and clearing the fault in 16 ms.
- The proposed topology limits the rate of rise of the voltage across the DC CB, reduces the on-state switching losses, and ensures an equal voltage distribution regardless of tolerances in the switching characteristics.
- The proposed topology can improve the overall performance of MT-HVDC systems and increase the reliability of the DC grids.

2. Configuration and Operation of the Proposed Hybrid DC Circuit Breaker

2.1. Configuration of the Proposed Hybrid DC Circuit Breaker

Figure 1 illustrates the overall structure of the proposed HDCCB with bidirectional current interruption capability. This structure consists of two main DC CBs in the main branch, a fast mechanical switch and an auxiliary DC CB in the auxiliary branch, and a residual DC current disconnector. The residual DC current disconnector (in series with a current limiting reactor) is used to entirely isolate the DC circuit.

Figure 2 demonstrates the proposed configuration of the main DC CBs in the main branch. In this configuration, four submodules are considered to be connected back-to-back to isolate the DC current fault. Each submodule includes a diode, D, and a low resistance switch, S, in series and a capacitor, C, in parallel with the diode and switch. The switches are capable of breaking the bidirectional fault current. Also, the polarity of the capacitor changes with respect to the direction of the fault current. In order to protect the back-to-back submodules and prevent the capacitors from overvoltage, a Metal Oxide Varistor, MOV, is used.

The auxiliary DC CB consists of two switches, as shown in Figure 3. This CB matches lower voltage and current capability.

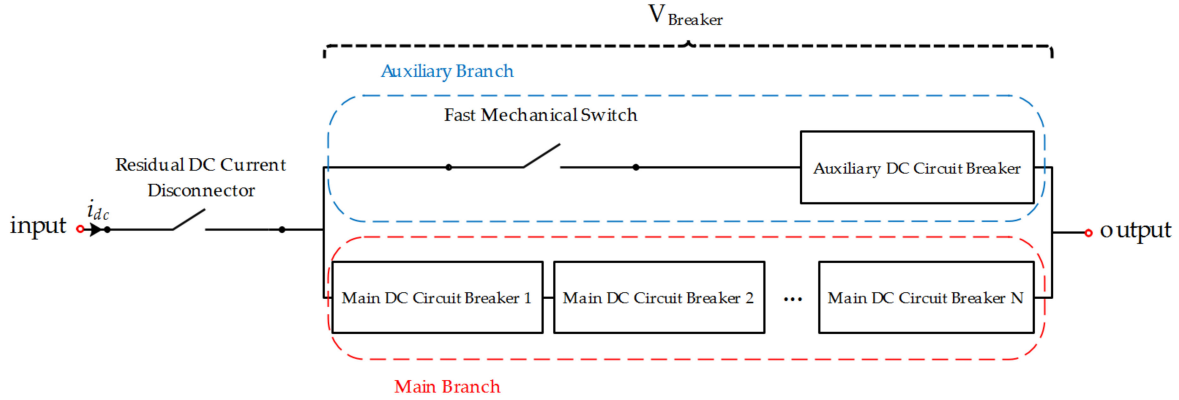

Figure 1. Overall structure of the proposed HDCCB.

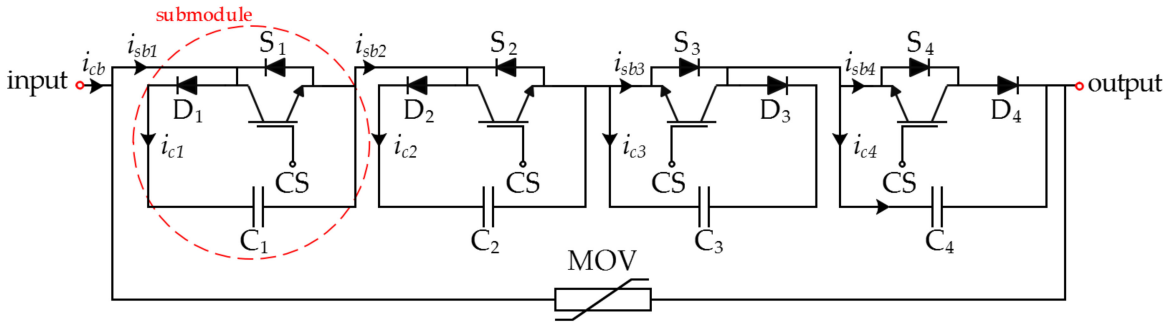

Figure 2. Configuration of the main DC CBs in the main branch.

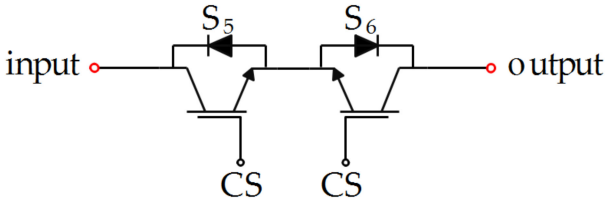

Figure 3. Configuration of the auxiliary DC CB.

2.2. Principle Operation of the Proposed Hybrid DC Circuit Breaker

Predefined states of each component in the submodule determine the operation modes of the proposed HDCCB. Considering the operation modes, the switches can be either turned on or off. During the normal operation, the DC current flows through the auxiliary branch. In case of the DC fault, the auxiliary DC CB commutes the current to the main branch, and the fast mechanical switch opens. During the current breaking, the fast mechanical switch isolates the auxiliary DC CB from the voltage across the main DC CB. As a result, the rating voltage of the auxiliary DC CB reduces. Therefore, the majority of the power losses would be related to the switching losses. The fast mechanical switch opens when zero current and/or low voltage stress can be detected. The recovery voltage of the fast mechanical switch determines by the proactive level of the surge arresters, while both the main and auxiliary DC CBs are open. By connecting several mechanical switches, the operation time exceeds 30 ms. Proper control of the HDCCB leads to minimizing the time delay of the mechanical switching elements. Hence, the operation time of the multiple switches should be less than the time for selective protection. Figure 4 depicts the typical proactive control of the HDCCB. The proactive control system enables when the level of the DC line current exceeds the predefined overcurrent level. In this case, two events are expected: (1) The selective protection sends a trip signal. (2) The DC current of the faulty line reaches the maximum breaking current capability of the main DC CB. In both cases, there would be a time delay for the current breaking of the main DC CB.

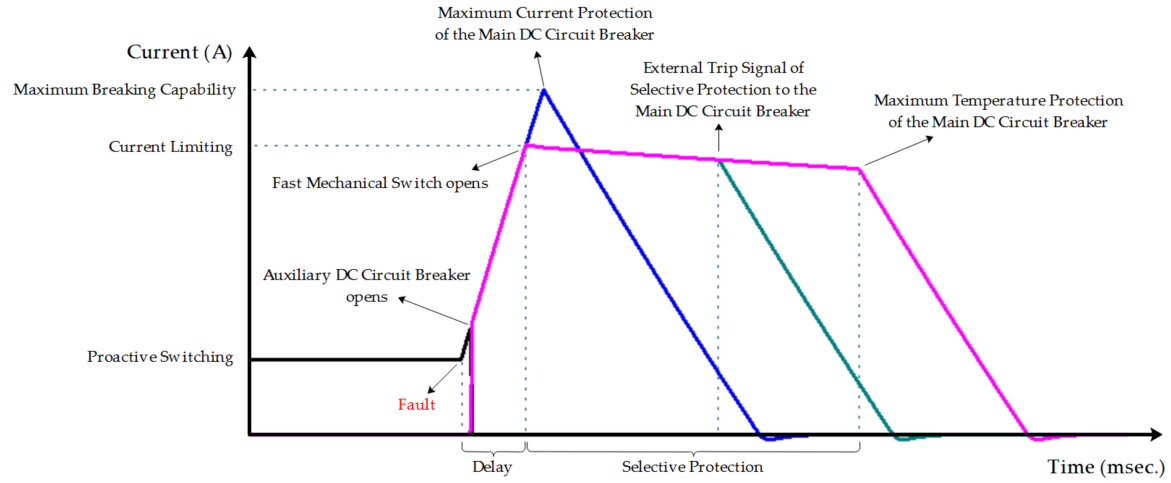

Figure 4. The current waveform of a typical proactive HDCCB.

To extend the operation time until the main DC CB sends the trip signal, the main DC CB may disconnect the line in the current limitation mode prior to the current breaking. To prevent sudden increases in the line current, the voltage drop across the DC reactor should be controlled by the main DC CB. The energy dissipation capability of the surge arrester determines the maximum operation time of the current limiting mode. Also, to allow maintenance on demand while not interrupting the power transfer in the DC grids, scheduled current transfer of the line current from the auxiliary DC CB to the main DC CB is required. Considering the proactive mode, overcurrent in the DC grid can activate the current transfer from the auxiliary branch into the main branch of the DC CB prior to the trip signal of the protection device. Considering the CB failure, the backup CB activates within less than 0.2 ms to avoid large disturbances in the DC grids and maintain the breaking current capability of the backup CB at the reasonable levels. After clearing the fault, the HDCCB returns to its normal operation mode.

According to Figure 2, when the DC CB, which is located at the power receiving, is closed, the power flows from the output of the DC CB, based on the unidirectional conduction ability of the diode that is paralleled with the IGBT in the submodule. When the DC CB, which is placed at the power sending end, is closed, the power flows from the input of the DC CB with the conduction of the IGBT in the submodule. Under the normal operation, the IGBT in the submodule is conducted and cascaded into the circuit. In case of DC fault, the IGBT of the submodule is shut down to prevent the diode and capacitor from being cascaded into the fault loop. By charging the capacitor, the back Electromotive Force (EMF) forces both ends of the equivalent capacitor on the short-circuit path to surpass the peak line voltage on the AC side to block the fault current. The fault tolerance capability can be significantly improved as the diode in the submodule, and the arm inductance in the AC/DC converter station in the DC fault are both shock resistance. This structure limits the rate of rise of the voltage across the DC CB, reduces the on-state switching losses, and guarantees an equal voltage distribution regardless of tolerances in the switching characteristics. Table 1 shows the operation status of the components in each submodule.

Table 1. The operation status of the components in each submodule.

Operation Mode	Diode	IGBT	Capacitor
Mode 1: Power Receiving End	Bypass	No Action	Bypass
Mode 2: Power Sending End	Bypass	Conducted	Bypass
Mode 3: Shut Down	Accessing to the Circuit	Shut Down	Charging

3. Design Parameters in the Proposed Hybrid DC Circuit Breaker

The designed parameters of the proposed HDCCB should be properly determined successfully to interrupt the fault current. Figure 5 illustrates the equivalent circuit of the DC CB in the DC grid in case of a short-circuit fault. As shown in this figure, the AC/DC converter station can be modeled as a DC voltage source, U_{DC}, and the line reactor in the DC grid is replaced by L_{DC} [28].

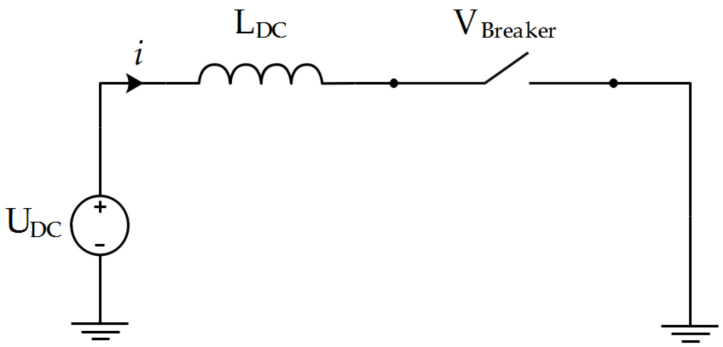

Figure 5. Equivalent circuit of the DC CB in the DC grid.

After the DC fault occurrence, the induced voltage, V_L, is generated by the inductor of the DC grid. Considering that the inter-terminal voltage of the DC CB is $V_{Breaker}$, then:

$$U_{DC} = V_L + V_{Breaker} = L_{DC}\frac{di}{dt} \tag{1}$$

By establishing the transient state of the voltage of the DC CB, V_L reverses, and $V_{Breaker}$ limits by the voltage of MOV, V_{MOV}. Therefore:

$$U_{DC} = V_L + V_{Breaker} = L_{DC}\frac{di}{dt} + V_{MOV} \tag{2}$$

According to Equations (1) and (2), the fault current can be derived as follows:

$$i = \begin{cases} \frac{U_{DC}}{L_{DC}} \cdot t \\ \frac{U_{DC} - V_{MOV}}{L_{DC}} \cdot t \end{cases} \tag{3}$$

Hence, the rate of rise of fault current can be calculated as follows:

$$\frac{di}{dt} = \begin{cases} \frac{U_{DC}}{L_{DC}} \\ \frac{U_{DC} - V_{MOV}}{L_{DC}} \end{cases} \tag{4}$$

Considering the time of the fault, t_{fault}, the maximum breaking current capability of the DC CB is as follows:

$$i_{(max)} = \frac{di}{dt} \cdot t_{fault} = \frac{U_{DC}}{L_{DC}} \cdot t_{fault} \tag{5}$$

In addition, the maximum rate of rise of fault current can be derived as follows:

$$\frac{di}{dt}_{(max)} = \frac{U_{DC}}{L_{DC}} \tag{6}$$

The energy dissipation capability of the HDCCB is from the DC power source and the stored energy in the line reactor. The energy dissipation from the DC power supply can be written as follows:

$$E_{source} = \int U_{DC} \cdot idt = \int U_{DC} \cdot \frac{U_{DC} - V_{MOV}}{L_{DC}} \cdot tdt \tag{7}$$

In addition, the energy dissipation from the line reactor can be written as follows:

$$E_{reactor} = \frac{1}{2} L_{DC} (i_{(max)})^2 \tag{8}$$

The summation of the energy dissipation from the DC power source and the line reactor gives the total energy dissipation of the HDCCB.

$$E_{MOV} = \frac{1}{2} \cdot \frac{U_{DC} V_{MOV}}{U_{MOV} - V_{DC}} \cdot \left(\frac{1}{\frac{di}{dt}_{(max)}} \cdot i_{(max)} \right)^2 \tag{9}$$

4. Results and Discussions

4.1. Simulation Results

In order to check the performance of the proposed HDCCB, a DC-link representing a DC-pole of the VSC-HVDC system is modeled on PSCAD/EMTDC environment, as shown in Figure 6. An HDCCB is located at the end of the DC-link. As one of the most common faults in the VSC-HVDC systems, a single line-to-ground fault on the DC-link is selected for the fault mechanism analysis. It is assumed that the output voltage of the VSC-HVDC converter station, U_{DC}, is constant. Tables 2 and 3 show the main parameters of the DC-link and the specifications of the proposed HDCCB, respectively.

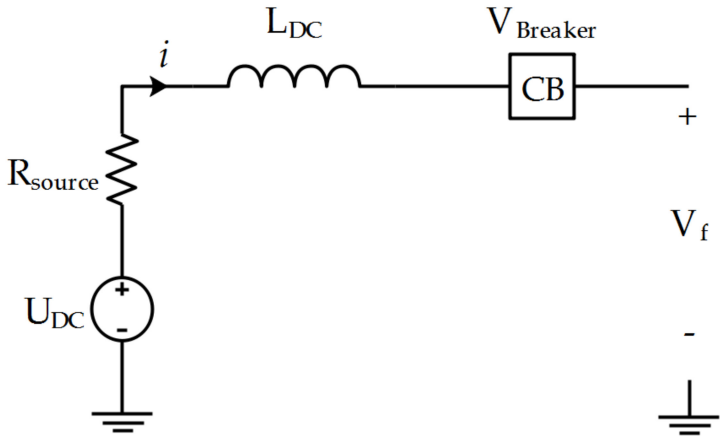

Figure 6. Configuration of the DC-link for fault analysis.

Table 2. DC-link parameters.

Parameter	Value
U_{DC}	320 kV
R_{source}	0.001 Ω
L_{DC}	100 mH

Table 3. Specifications of the proposed HDCCB.

Parameter	Value
Capacitor (C)	6.8 μF
Time delay of residual disconnector	20 ms
Time delay of fast mechanical switch	2 ms
Forward Breakover Voltage (IGBT)	100 kV
Forward Breakover Voltage (Diode)	100 kV

4.1.1. Rated Current Interruption

To give a general perspective about the relation of the designed parameters, considering 2 ms as the breaking time, and the fact that DC line fault is close to the DC switchyard, the maximum rate of rise of fault current is 3.5 kA/ms for a DC reactor of 100 mH in a 320 kV DC power grid with 10% maximum overvoltage. If the rated line current is 2 kA, the minimum required current breaking current capability of the HDCCB should be 9 kA. When there is no fault in the DC grid, the voltage drop across the DC CB is 0.04 V, and the total current passing through the DC grid is 1.6 kA. Figure 7 shows the behavior of the DC line current, and the current passing through the capacitors and switches of the HDCCB after applying a short-circuit DC fault at 5 s. As shown in Figure 7, the breaking time is less than 2.5 ms. The maximum current passing through the capacitors and switches of the HDCCB is 2.3157 kA and 8.0713 kA, respectively. The auxiliary CB opens into 50 µs. At 5.00195 s., the fast mechanical switch opens, where the corresponding value of the current limiting is 8.0713 kA. According to Figure 7, the maximum value of the DC fault current is 8.4425 kV, which is less than the minimum required breaking current capability of the HDCCB and the fault is successfully cleared within 16 ms. Based on the provided results, the maximum breaking current capability of 9 kA is confirmed. It should be noted that in Figure 7, the DC current passing through the line and the DC current of the proposed HDCCB are the same.

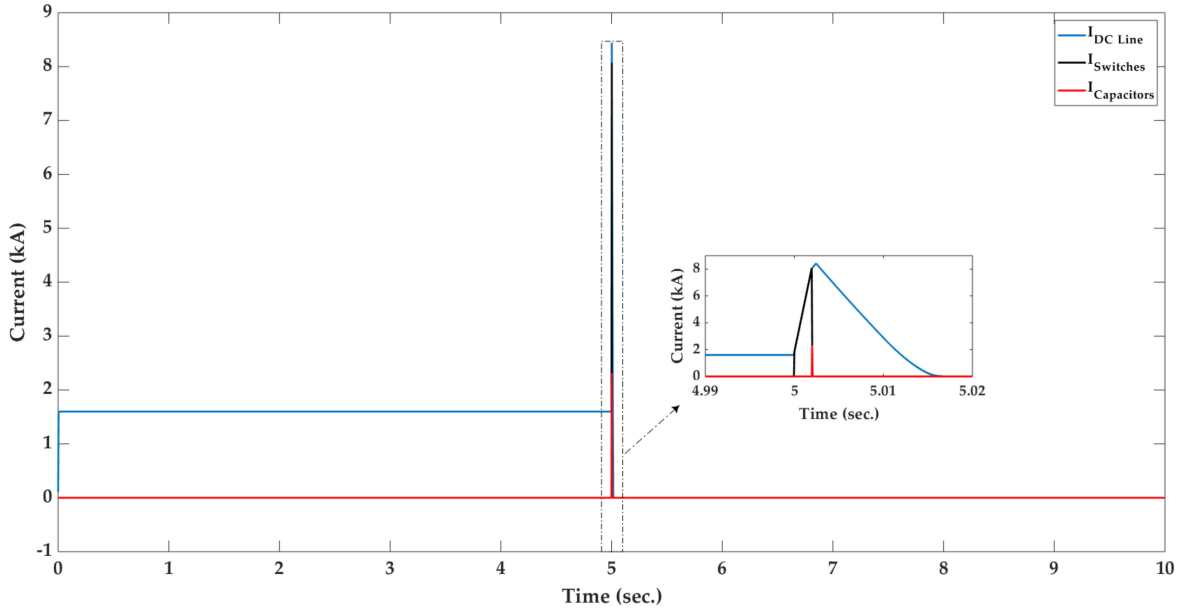

Figure 7. The DC line current, and the current passing through the capacitors and switches of the proposed HDCCB after applying a short-circuit DC fault at 5 s.

As there are some limitations in terms of breaking current capabilities of the IGBTs, by rising the current, voltage drop across the IGBTs increases significantly. To overcome this issue, the press-back IGBTs are used to ensure a reliable short-circuit without mechanical damage and failure of the IGBTs' modules. Therefore, in case of the failure of one of the IGBT modules, the fault can be cleared by the rest of IGBTs.

Figure 8 illustrates the CB voltage and voltage at the fault location (V_{Fault}) after applying a short-circuit DC fault at 5 s. As shown in Figure 8, the voltage across the proposed HDCCB exceeds approximately 180 kV during the current commutation, and the proposed HDCCB successfully clears the fault within 16 ms.

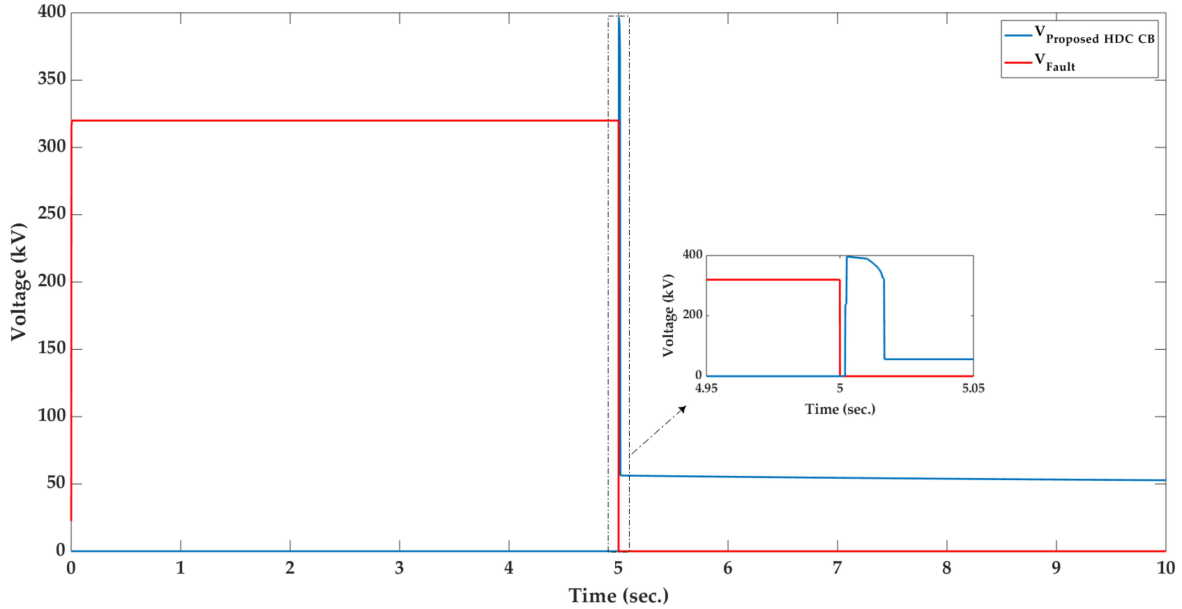

Figure 8. The CB voltage and voltage at the fault location after applying a short-circuit DC fault at 5 s.

By increasing the capacity of the capacitors of the main DC CBs, the maximum breaking current capability of the HDCCB increases. However, due to the discharge time of the capacitors, it takes longer time to entirely clear the DC fault.

Figure 9 demonstrates the dissipated energy of the surge arrestors in the two main DC CBs of the proposed HDCCB. The maximum dissipated energy of the surge arrestors in the main DC CB 1 and 2 is 12.6209 kJ and 7.7952 kJ, respectively.

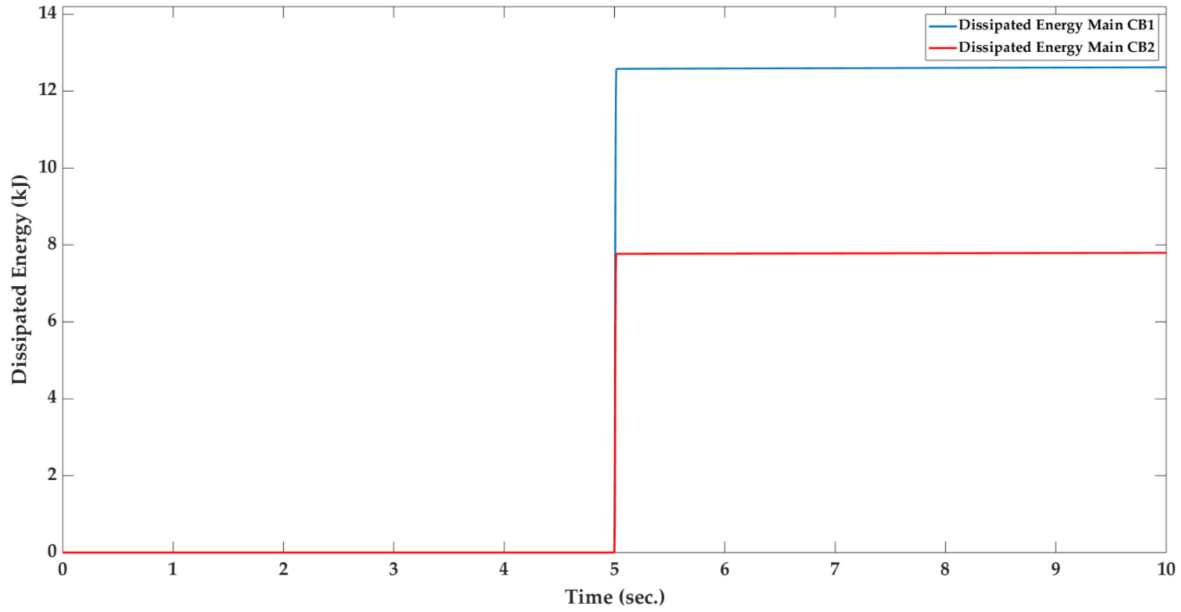

Figure 9. The dissipated energy of the surge arrestors in the two main DC CBs of the proposed HDCCB after applying a short-circuit DC fault at 5 s.

4.1.2. Reverse Current Interruption

In order to demonstrate the reverse current interruption of the proposed HDCCB, the direction of designed CB is reversed, so that the fault current flows in the opposite direction. Figure 10 shows

that the same as the rated current interruption, the maximum breaking current capability of −9 kA is confirmed.

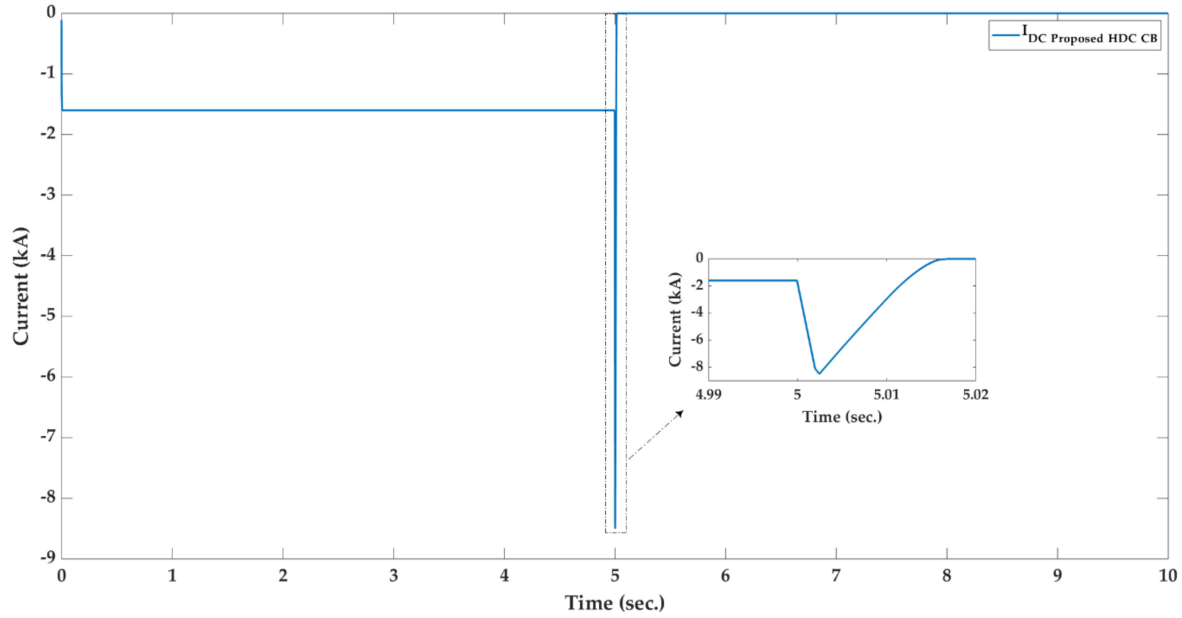

Figure 10. The DC current of the proposed HDCCB after applying a short-circuit DC fault at 5 s after changing the direction of the proposed HDCCB.

Figure 11 illustrates the CB voltage and voltage at the fault location after applying a short-circuit DC fault at 5 s after changing the direction of the proposed HDCCB. As shown in Figure 11, the proposed HDCCB successfully clears the fault within 16 ms.

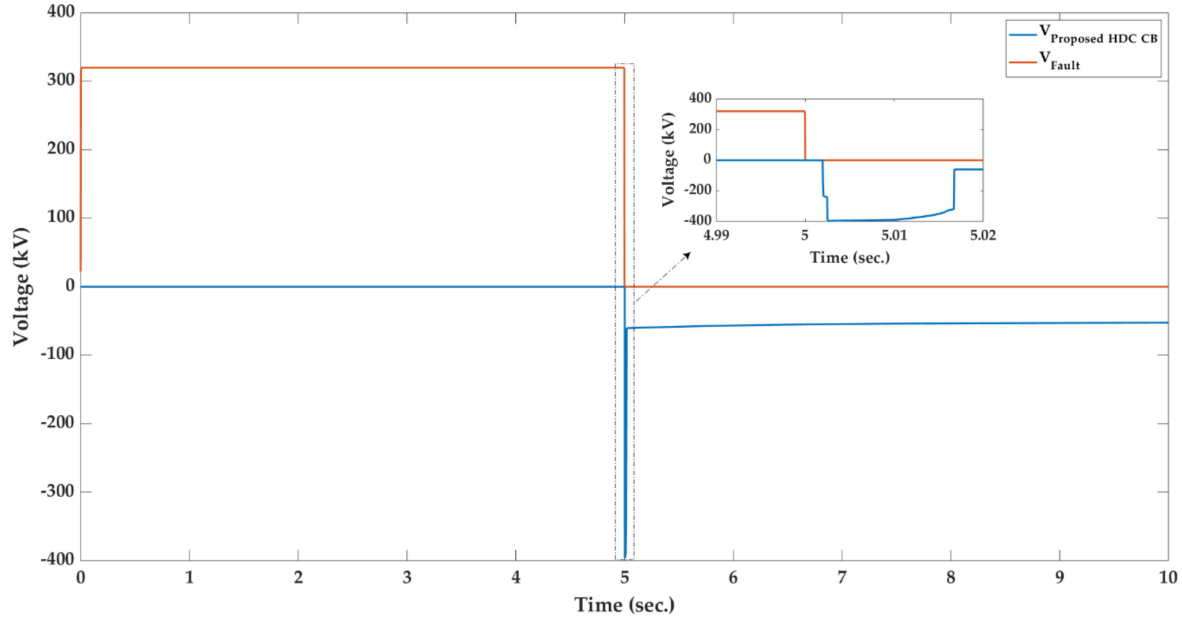

Figure 11. The CB voltage and voltage at the fault location after applying a short-circuit DC fault at 5 s after changing the direction of the proposed HDCCB.

4.1.3. Reclosing and Rebreaking Capabilities

To evaluate reclosing and rebreaking capabilities of the proposed HDCCB, a short time (dead time) between the first trip signal and the closing signal is considered. During this period of the time, there

is no response from the proposed HDCCB to the test system. After the first trip signal, the proposed HDCCB opens and performs the first current interruption. The reclosing signal is sent to the proposed HDCCB 50 ms after the first trip, and the proposed HDCCB attempts to reconnect the source to the line. As the fault is not cleared from the system, the fault current rises as soon as the CB is closed. The second trip signal is sent to the proposed HDCCB 50 ms after the CB is closed, and then the proposed HDCCB performs the second current interruption. After that, the proposed HDCCB remains open to insulate the DC fault. Figures 12–15 show reclosing and rebreaking capabilities of the proposed HDCCB in both the rated and reverse current interruptions. The simulation results validate the reclosing and rebreaking capabilities of the proposed HDCCB in both the rated and reverse current interruptions.

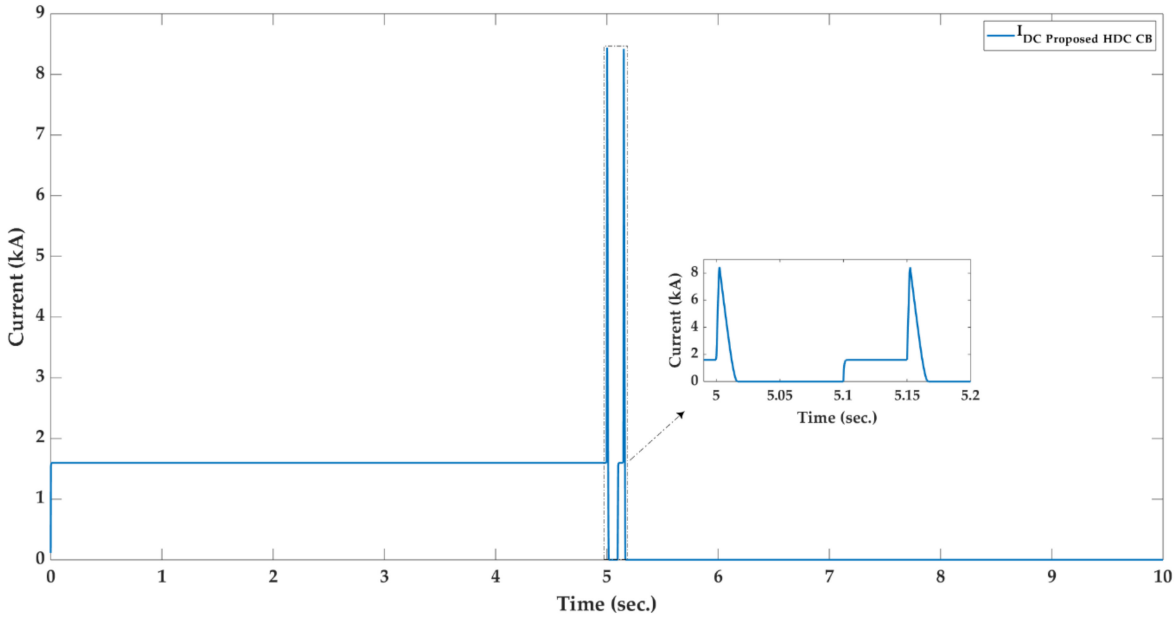

Figure 12. The DC current of the proposed HDCCB in reclosing and rebreaking test in the rated current interruption.

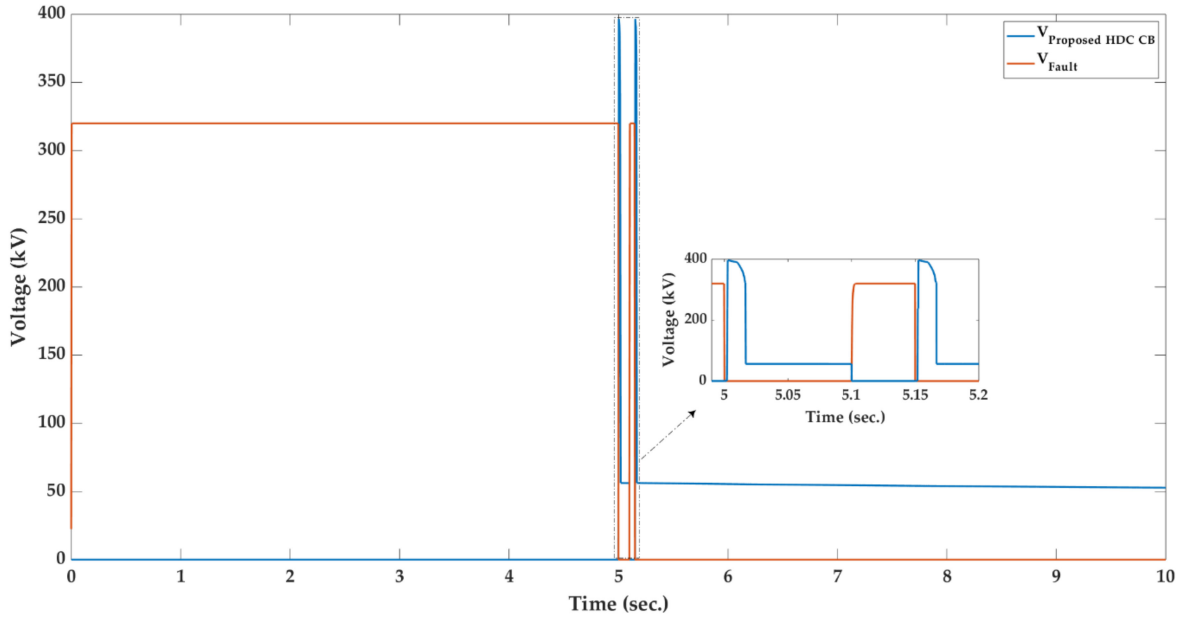

Figure 13. The CB voltage and voltage at the fault location in reclosing and rebreaking test in the rated current interruption.

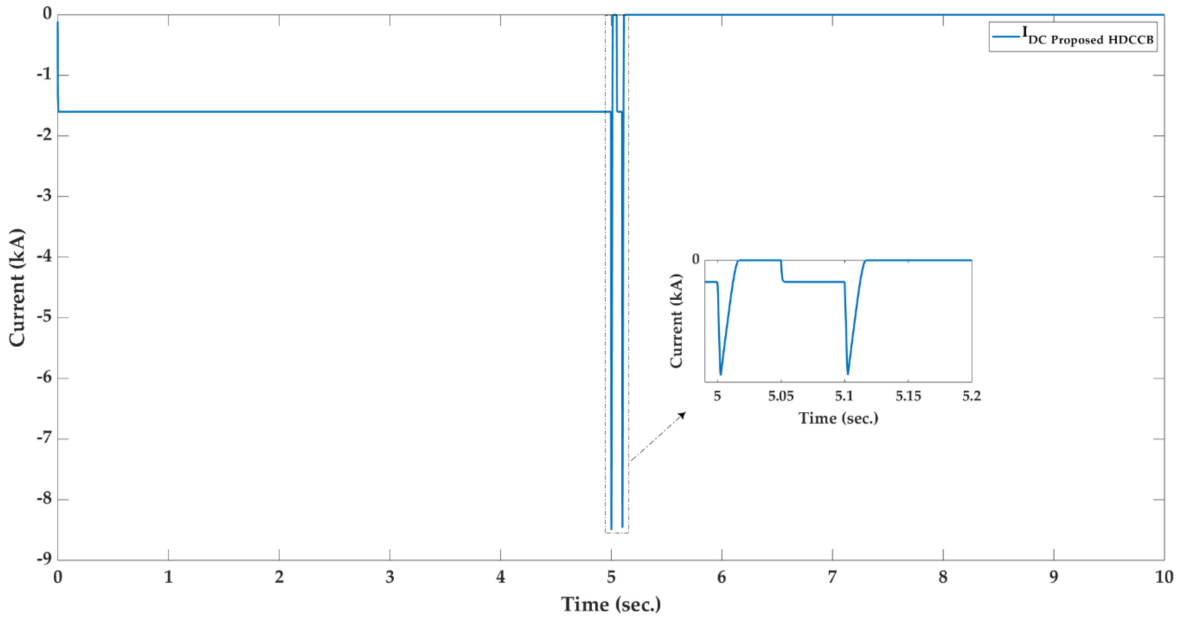

Figure 14. The DC current of the proposed HDCCB in reclosing and rebreaking tests in the reverse current interruption.

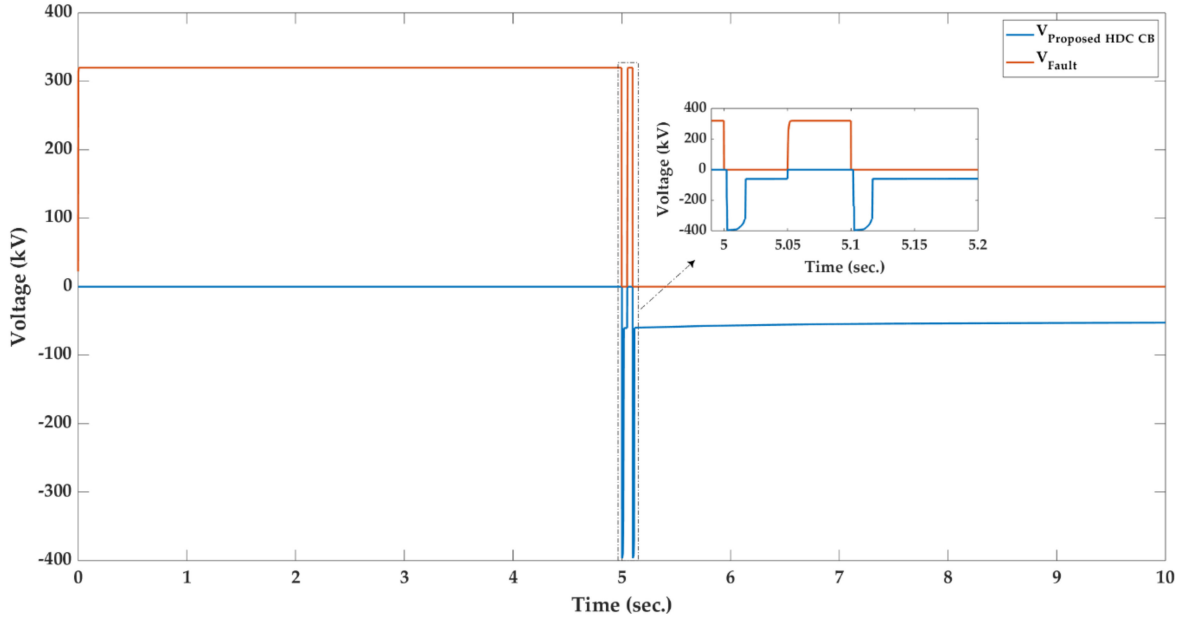

Figure 15. The CB voltage and voltage at the fault location in reclosing and rebreaking test in the reverse current interruption.

4.2. Comparison

To evaluate and compare the performance of the proposed HDCCB over the conventional DC CB in [22,29,30], replication is done, and proper matching is noticed in all cases. Figure 16 illustrates a comparison between the CB voltage responses of the proposed HDCCB and the conventional DC CB. As shown in Figure 16, the voltage response of the proposed HDCCB tracks the voltage of the conventional DC CB. However, due to the fact that the DC capacitors have some charges, the level of DC voltage of the proposed HDCCB after the fault is more than the level of voltage of the conventional DC CB.

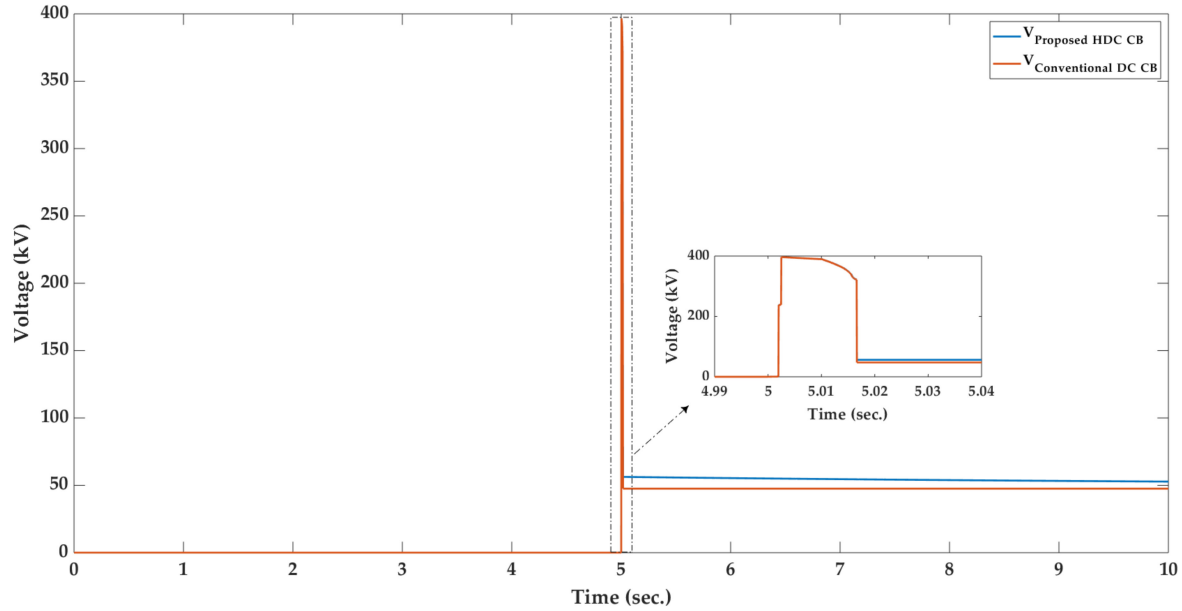

Figure 16. Comparison between the voltage response of the proposed HDCCB and the conventional DC CB after applying a short-circuit DC fault at 5 s.

Figure 17 demonstrates the comparison between the DC current response of the proposed HDCCB and the conventional DC CB after applying a short-circuit DC fault at 5 s. As shown in Figure 17, good matching is observed. The maximum breaking current capability of the proposed HDCCB and conventional DC CB are 8.4425 kA and 8.4207 kA, respectively. Thus, the difference between the maximum breaking current capability of the proposed HDCCB and conventional DC CB is 21.8 A.

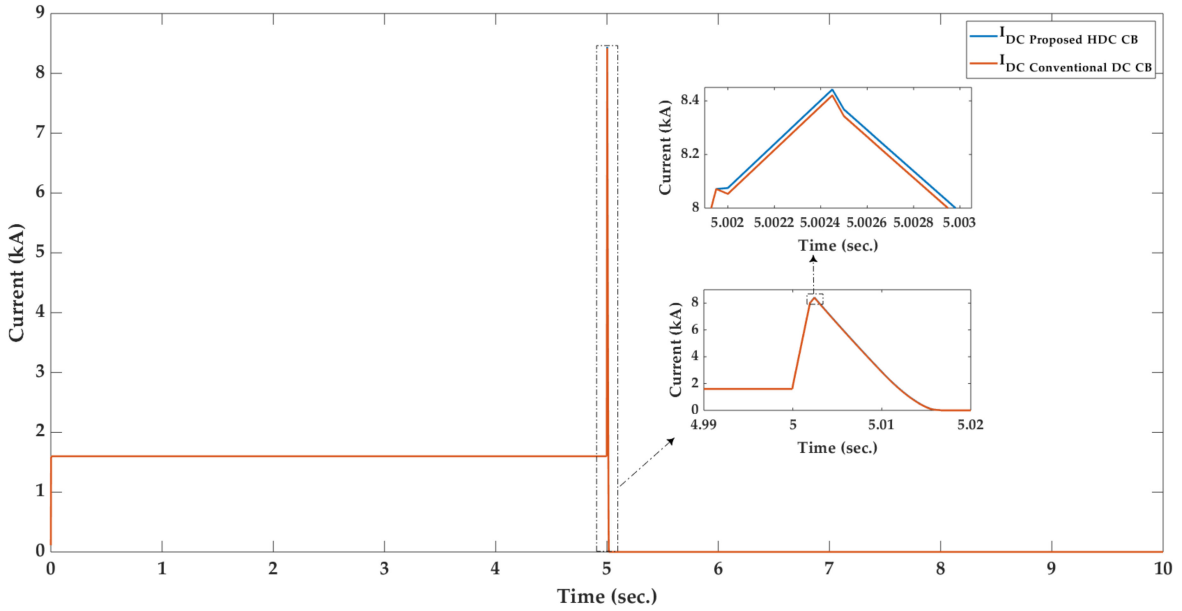

Figure 17. Comparison between the DC current response of the proposed HDCCB and the conventional DC CB after applying a short-circuit DC fault at 5 s.

The maximum dissipated energy of the surge arrestor in the DC CB 1 of the conventional DC CB is 12.6388 kJ, which is 17.9 J more than the corresponding value of the proposed HDCCB. However, because of the capacitor charge, the dissipated energy of the surge arrestor in the DC CB 2 of the conventional DC CB is 7.7952 kJ which is 16.1 J less than the corresponding value of the proposed

HDCCB. But, the total dissipated energy of the surge arrestor of the proposed HDCCB and the conventional DC CB are approximately the same.

5. Conclusions

This paper presents a new topology of a fast proactive Hybrid DC Breaker (HDCCB) to isolate the DC faults in Multi-Terminal VSC-HVDC (MT-HVDC) grids in case of fault current interruption, along with lowering the conduction losses and lowering the interruption time. All modes of operation of the proposed topology are studied. Simulation results verify that compared to the conventional DC CB, the proposed topology has lower interruption time, lower on-state switching losses, and higher breaking current capability. Due to the fact that MT-HVDC systems can share the power among the converter stations independently and in both directions, and considering the fast bidirectional fault current interruption, and reclosing and rebreaking capabilities, the proposed HDCCB can improve the overall performance of MT-HVDC systems and increase the reliability of the DC grids.

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