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Modeling and Application of Controllers for a Photovoltaic Inverter for Operation in a Microgrid

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Abstract: The penetration of renewable energies in the context of distributed generation represents challenges such as maintaining the reliability and stability of the system and considering the random behavior proper of generation and consumption. In this context, microgrids make it possible to manage effectively the generation and consumption of this energy, incorporating, electronic power converters, energy storage systems, and hierarchical control schemes. This paper presents the modeling, design, and application of controllers for a photovoltaic inverter operating in island mode. For this application, the photovoltaic inverter regulates the inverter output voltage via two control configurations implemented to follow the voltage reference imposed by the scheme droop. The first control scheme is configured with a two-degrees-of-freedom controller plus a repetitive controller. In this configuration, the repetitive controller is implemented in the direct loop. The second scheme is configured with an integral proportional controller—proportional controller plus a resonant controller. This configuration is formed by an integral proportional control in the direct loop plus a resonant controller and a proportional controller in the feedback loop. Both control configurations are implemented to improve the inverter disturbance rejection capability when it feeds both linear and non-linear local loads. In addition, these configurations allow the parallel connection of inverters with good performance, using a droop scheme that allows the parallel connection of converters. The tests are carried out by means of simulations using PSIMTM, which shows that, with the implemented controllers, the total harmonic distortion of the inverter output is below 5%, as recommended by the IEEE 519-1992 standard.

Keywords: controllers; photovoltaic inverter; parallel connection; island mode operation; microgrid

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1. Introduction

Centralized generation is still the most common means of power generation and delivery worldwide. It is based on large facilities such as nuclear, hydro-, and thermo-electric power plants, interconnected through a network of high-voltage transmission lines that delivers power unidirectionally to distant end users in densely populated areas. By the same token, isolated, distant communities lack access to this utility due to elevated delivery cost. For these locations, distributed generation (DG) based on renewable energy sources (RES) is a better alternative, because generation takes place at or near the consumption point, lowering both generation and delivery costs [1]. In this case, it is possible to implement autonomous interfaces, able to control whether or not to connect to the utility grid, as physical or economic conditions dictate.

Microgrids [2–4], as they are known, consist of power converters and storage devices powered by a combination of RES like solar panels, fuel cells, and wind micro-turbines that require the use of power inverters to condition the amplitude, frequency, and shape of the voltage signal within standard requirements for harmonic control in electric power systems, regardless of applied load [5–7].

The diversity of RES able to mesh into microgrid power systems, as well as the need for effective and efficient management of both power generation and consumption, poses several challenges arising from the integration of electronic power converters, energy storage systems, and hierarchical control schemes. In particular, the control system must be capable of maintaining the energy balance in the microgrid, a complex task when the powers of the generation and consumption units are different [8]. Several approaches exist to address the integration issues caused by the inherent differences in the electrical characteristics of the microgrid elements. Thus, Baek, Cho, and Yeo (2019) propose a voltage control scheme with an inner repetitive current controller to achieve lower output impedance and better disturbance rejection capability for a UPS system, for which it is important to ensure the output voltage regulation and low total harmonic distortion (THD) under non-linear loads [9]. Jamil et al. (2020) developed a higher-order repetitive controller with phase lead compensator and applied it to the current control of a two-level three-phase grid-connected converter [10]. Jank et al. (2017) presented a comparative analysis of the PID, resonant, and repetitive controller applied to a single-phase half-bridge pulse-width modulation (PWM) inverter, varying the switching frequency and the inductor current ripple. They concluded that both switching frequency and inductor current ripple play a key role in the controller design [11]. Chen et al. (2020) designed a repetitive control for dual-buck full-bridge single-phase inverter to ensure the steady-state performance of the system, and adaptive PI control to speed up the system's dynamic response process [12]. Chen et al. (2020) presented a PID-based repetitive control strategy to achieve high control accuracy for tracking a determined periodic reference signal [13]. Pan et al. (2018) developed a method to suppress current harmonic components caused by non-ideal factors. A new PID controller named R–2DOF PID controller was proposed and used in the control system of the permanent magnet synchronous linear motor (PMSLM) in the miniature microsecond laser cutting system, to suppress PMSLM current harmonics [14]. Patil and More (2019) compared the performance of a Cuk converter with proportional integral controller and a proportional resonant controller [15]. Sreekumar, Danthakani, and Veettil (2018) investigated the implementation of P-R controller in an autonomous DG unit [16]. Torres, Roncero-Sánchez, and Batlle (2018) developed a 2DOF resonant control scheme for voltage-sag compensation in dynamic voltage restorers [17]. Finally, Biricik and Komurcugil (2018) reported a control strategy for PUC inverters based on PI and PR controllers [18].

Other works present control methods to carry out parallel connection of the conversion units [19–21]. In [19], paralleling technique with VSI inverters is implemented. The RMS Current Control technique with droop in output voltage is implemented to inverter control. The LCL filter is used at inverter output for wave shaping and output reduced noise level output. The PI compensator is used in a feedback loop to attain the system stability. In [20], distributed generation units are connected to the microgrid through an interfacing inverter. The interfaced inverter plays the main role in the microgrid operating performance. In this paper, interfaced parallel inverter control using a droop control P-F/Q-V was investigated when the microgrid operated in island mode. In inverter islanding mode operation, droop control should maintain voltage and frequency stability. The droop control for parallel inverters is implemented and the proportional load sharing is obtained from each individual inverter. In [21], a control strategy is proposed to improve load sharing performance in order to reduce the circulating current between inverters parallel connected in microgrids in island mode operation. The control strategy includes a filter parameter estimator, which compensates for any possible uncertainty or deviation in its value. Double

loop feedback control is also adopted, with external voltage and internal current control, providing excellent performance under transient and steady state conditions.

In this work, two control configurations are developed and applied: a two-degree-of-freedom control, plus a repetitive control (2DOF + RC) [22–24], and a proportional–integral–proportional control plus a resonant control (PI-P + ResC) and an integral–proportional control plus a resonant control (PI-P + ResC). The 2DOF controller guarantees the overall stability of the energy conversion system, allowing, at the same time, adequate setpoint tracking and disturbance rejection. This is achieved by the first controller implemented in the direct loop, and a second controller in the feedback loop, under different configurations derived from a proportional integral derivative controller (PID); for example, a PI controller in direct loop and a derivative controller in the feedback loop, obtaining a configuration (PI-D). The design of an integral controller in the direct loop and a derivative proportional control in the feedback loop is also possible, giving rise to a configuration (I-PD). In this work, we propose the design and implementation of a control structure with the following characteristics: a PI + RC controller, implemented in the direct loop, and a P controller implemented in the feedback loop. This configuration ensures that in the direct loop, the PI controller allows good setpoint tracking, and the addition of repetitive control contributes to the disturbances rejection, adding to this task the proportional controller implemented in the feedback loop. The implementation of this control configuration causes the inverter output closed-loop impedance to have a resistive characteristic at low frequencies and an inductive characteristic at high frequencies. Therefore, it is necessary to implement a resistive virtual impedance loop and choose a droop scheme with these characteristics to allow conversion units parallel connection.

Regarding the PI-P + ResC controller, it consists of two control configurations, a proportional integral–proportional controller (PI-P) plus a resonant controller (ResC). This configuration is structured by an integral proportional control in the direct loop plus a resonant controller, and a proportional controller in the feedback loop. As the control configuration described previously, the design of the PI-P controller assures the overall stability of the conversion system, while the resonant control is designed and implemented to improve the disturbances rejection, contributing to the task of the P controller implemented in the feedback loop. This configuration achieves good setpoint tracking and good disturbances rejection, in addition to the fact that a closed-loop impedance with resistive characteristics appears at the inverter output at high frequency. Thus, it is unnecessary to implement a virtual impedance loop and, therefore, we can choose a droop scheme with a resistive character for the inverters parallel connection.

Both configurations are a new proposal to solve the problem of reduction of total harmonic distortion and for inverter connection parallel, allowing a steady state error equal to zero (eee = 0), and the disturbance rejection with linear and non-linear load in the range between 1% and 2.5%, below the 5% required by the IEEE 519-1992 standard.

According to our simulations, good performance of the system is justified considering the following: with the implementation of these regulators, it is possible to have good setpoint tracking and good disturbance rejection, giving rise to a sinusoidal waveform of the voltage signal and maintaining the amplitude close to 230 V RMS, as well as its frequency. The reference voltage signal is obtained through droop schemes that allow the inverters connection in parallel to meet increases in load demand. For the present application, we chose a resistive droop scheme with a virtual impedance loop of the same characteristics that allows the inverters parallel connection and the homogeneous distribution of active and reactive power demanded by the load. The choice was determined considering that, with the implementation of both controllers, the inverter closed-loop impedance presents a resistive characteristic, which shows up in the Bode diagrams.

The present work is organized as follows: Section 2 describes the energy conversion system and the small signal model used to determine the transfer functions for the design of the current and voltage loops controllers. Section 3 describes the design of the controllers for the different control loops of the inverter. Section 4 presents the characteristics and

design of the droop scheme used in the inverter. In Section 5, the analysis of the closed-loop impedance of the inverter with the controllers and the droop scheme employed is given. A description of the results of the simulations performed in PSIM^{TM} [25] is provided in Section 6. In Section 7, the results obtained through experimental tests are presented. In Section 8, the discussion of the results obtained through simulations is presented. Finally, the conclusions are delivered in Section 9.

2. The Inverter System

An inverter schematic diagram implemented, an H-bridge type with bipolar Pulse-Width Modulation (PWM), whose nominal values are given in Table 1, is shown in Figure 1.

Table 1. Inverter Main Parameters.

Parameter	Value
Nominal power of the inverter (P)	440 W
DC_LINK voltage (V_{DC})	400 V
Inverter output voltage (V_o)	230 VRMS
Inverter output frequency (f_o)	50 Hz
Inverter output inductance (L)	9.57 mH
Inverter Output capacitor (C)	600 nF
Damping resistance (R_d)	5 Ω
Inverter switching frequency (f_s)	20 kHz
Load resistance (R_{Load})	170 Ω

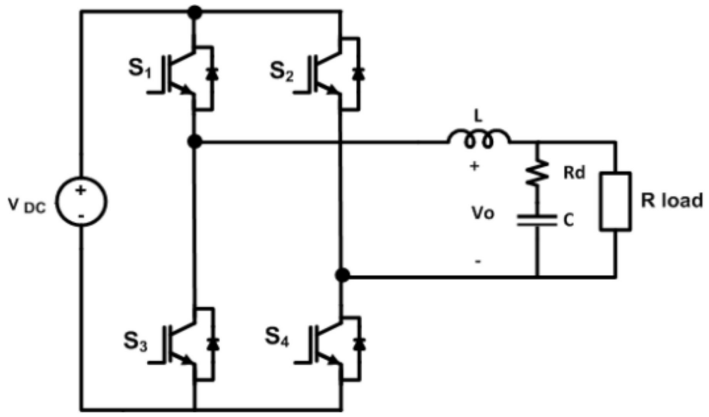

Figure 1. Inverter schematic.

2.1. Small-Signal Model

To implement a feedback linear control from a non-linear circuit such as a power electronic converter, it is necessary to obtain a linear model [26]. To this purpose, it is necessary to identify the transfer functions corresponding to the control variables. The transfer functions are obtained using the commutated PWM model [27].

The small signal model is shown in Figure 2, with small perturbations around the operation point (OP). In this figure $\hat{v}_{DC}$, $\hat{i}_L$, $\hat{d}y\hat{v}_o$, are small-signal terms and represent the inverter input voltage, the inductor current, the duty cycle, and the inverter output voltage, respectively. In addition, work cycle-to-the inductor current $G_{iL\_d}(s)$ and the inductor current-to-voltage output $Gv_o\_I_L$ transfer functions, are obtained.

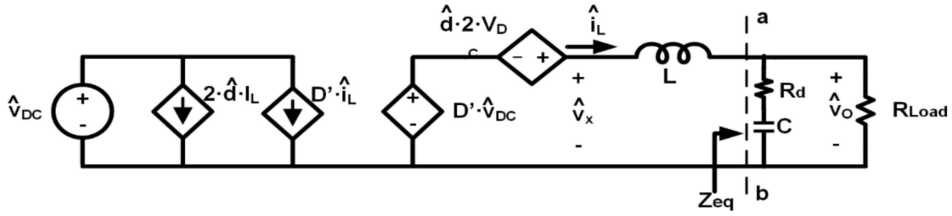

Figure 2. Small signal model of inverter.

2.2. Inverter Output Filter Design

To obtain a sinusoidal output signal with the same voltage and frequency characteristics of the power grid, it is necessary to filter the V_{DC} voltage present between output terminals the inverter single-phase full bridge. The topology used for the inverter is LC, as shown in Figure 3.

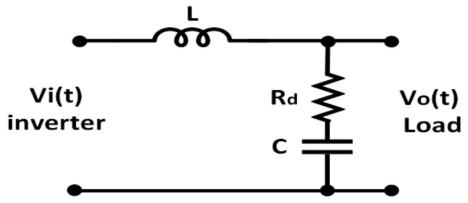

Figure 3. LC filter scheme.

The LC filter has an attenuation of −40 db/decade above the resonant frequency and is generally used in situations where the load impedance around the capacitor is relatively higher for frequencies equal to and/or higher than the switching frequency.

Some characteristics that this filter must present when it is designed are: At the fundamental frequency, the capacitor must absorb little reactive power, so the current in the inverter connected inductor side is hardly increased by the capacitor; at the frequency of the switching harmonics, the capacitor must absorb the harmonics of the inductor current, which must be small.

Based on the above, we proceed to describe the calculation of the filter values that must meet the following conditions: The value of capacitor C is limited to the maximum consumption of reactive power allowed by the inverter.

For this case, if the maximum current in the capacitor is required to be less than 5% of the nominal current at full load, the magnitude is:

$$I_c = 0.05 \cdot I_{load} \tag{1}$$

The capacitor impedance magnitude will be the output voltage divided by the current in the capacitor.

$$Z_c = \frac{V_o}{I_c} = \frac{V_o}{0.05 \cdot \left(\frac{S_{load}}{V_o}\right)} = 2404.5\ \Omega \tag{2}$$

where S_{load} is the load nominal power and Ic the capacitor current.

Since the magnitude of capacitor impedance is, $Z_c = 1/\omega_1 * C$, the value of C is given by:

$$C = \frac{1}{\omega_1 \cdot Z_c} \leq 1.3\ \mu F \tag{3}$$

where ω_1 is the grid frequency expressed in rad/sec.

The inductor can be calculated in terms of its allowable voltage drop when the inverter output voltage is the nominal operating voltage.

If an inductor impedance (Z_L) equal to or less than 10% of the load nominal impedance is required, then:

$$Z_L \leq 0.05 \cdot Z_{load} \tag{4}$$

The inductor impedance L magnitude is defined by $Z_L = \omega_1 \cdot L$, solving for L gives:

$$L = \frac{Z_L}{\omega_1} = \frac{0.1 \cdot Z_{load}}{\omega_1} \leq 19.1 \text{ mH}. \quad (5)$$

The LC filter resonant frequency must be between 10 times the grid frequency and half the switching frequency, to avoid resonance problems in the low and high part of the harmonic spectrum.

$$10 \cdot \omega_1 < \omega_{res} < \frac{\omega_s}{2} \quad (6)$$

where ω_{res} is the LC filter resonant frequency, which is defined by (7) and ω_s the switching frequency.

$$\omega_{res} = \sqrt{\frac{(L + L_g)}{L \cdot L_g \cdot C}} \quad (7)$$

To fulfill the conditions expressed in 1 and 6, a value of C = 600 nF is chosen, and it will be considered that the grid inductance Lg is ten times less than the inductor value inverter connected. One way to increase damping is by adding a resistor in series with the capacitor. It should be noted that selecting a very large resistance R_d will significantly reduce the oscillation at the resonance frequency and system efficiency. An additional criterion that can be included is based on placing a resistor that allows the attenuation of the inverter current control loop oscillation to be below 0 dB.

2.3. Control Scheme

Figure 4 shows the power inverter controls for the inductor current and the output voltage. In this figure, Gv(s) is the voltage controller transfer function, Gs(s) is the transfer current controller transfer function, and RD(s) represents a digital delay from a commutation period (Ts), given in Equation (8).

$$RD(s) = \frac{1 - \left(\frac{s * T_s}{2}\right) + \left(\frac{(s * T_s)^2}{8}\right)}{1 + \left(\frac{s * T_s}{2}\right) + \left(\frac{(s * T_s)^2}{8}\right)}. \quad (8)$$

where F_m is the PWM modulator gain, defined in (9).

$$F_m = \frac{1}{V_{pp-Triangular}} = 1 \quad (9)$$

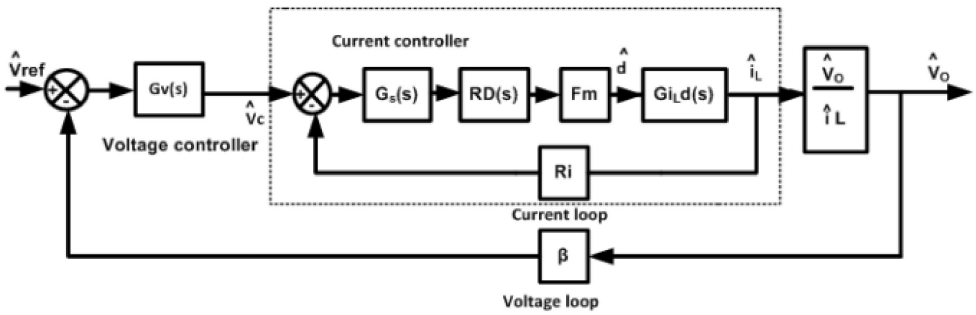

Figure 4. Control scheme diagram.

In Figure 3, R_i = 0.2 and β = 0.006, are the current and voltage sensor gain, respectively.

The main advantage, of this control scheme, is that the transfer function response is flatter than the reference voltage and less distorted than the peak-current control (PCC).

For the current-loop design, it is important the function that relates the output-current and the work-cycle, given by:

$$G_{iL\_d}(s) = \left.\frac{\hat{i}_L}{\hat{d}}\right|_{\hat{v}_{DC}=0} = \frac{2 \cdot V_{DC}}{Z_a + s \cdot L}, \quad (10)$$

where V_{DC} is the voltage in the DC_Link, and Z_a is the load impedance in parallel with the *damping* resistance and the output capacitor:

$$Z_a = \left(R_d + \frac{1}{sC}\right) \parallel R = \frac{(s \cdot C \cdot R_d + 1) \cdot R}{s \cdot C(R_d + R) + 1}, \quad (11)$$

3. Controller Design

3.1. Current Controller Design

The current controller implementation starts with a resonant controller (ResC), or a harmonic controller if its frequencies are multiples of the fundamental [28], and a proportional control (P). Such a controller has the objective of providing in a high gain to the reference signal frequency in the current loop to inhibit the effect of any grid disturbances present. A decision was made to implement a single resonant to the grid frequency. This is justifiable, since the objective of the islanded inverter is to keep the wave-shape, amplitude, and voltage signal frequency delivered to the load, not to the current signal.

In the inverter design, it is advisable to have a crossing frequency in the current loop, ten times smaller than 20 kHz, the inverter commutation frequency, which is about 5 dB gain factor and phase larger than 50 degrees, keeping appropriate stability margins [29]. For the present application, a P + Resonant (P + ResC) controller was chosen, defined by Equation (12).

$$G_S(s) = K_P + \frac{K_h * B_h * s}{s^2 + B_h * s + (\omega_h^2)}, \quad (12)$$

where:

$\omega_h = h * \omega_O$ where h is a resonance with a frequency multiple of the fundamental;
K_h = the peak resonance gain at the frequency ω_h;
B_h = the bandwidth, where the resonance has a gain.

For this application, the following resonant parameter values were established: h = 1, k_h = 100, $B_h = 2 \cdot \pi$, $\omega_0 = 2 \cdot \pi \cdot 50$, and:

$$K_P = \frac{L * \omega_{c\_desired}}{R_i * F_m * 2 * V_{DC}} = 1.34, \quad (13)$$

with $\omega_{c\ desired} = 2\ \pi\ 1800$.

The resonant control parameters, such as the gain at the resonance peak K_h and its bandwidth B_h, are determined so that its input in the current loop has no effect in the system global stability, keeping appropriate values for stability parameters like phase, gain margins, and cross frequency. As for $\omega_{c\_desired}$, this value is chosen to be close to half of the inverters commuting frequency.

The current control loop scheme (Figure 4) is shown in Figure 5. It has a PM: 64.5°, GM: 8.5 dB, and BW: 2.21 kHz, and it is defined by $T_i(s) = G_{iL\_}d(s) \cdot F_m \cdot R_i \cdot G_s(s)$.

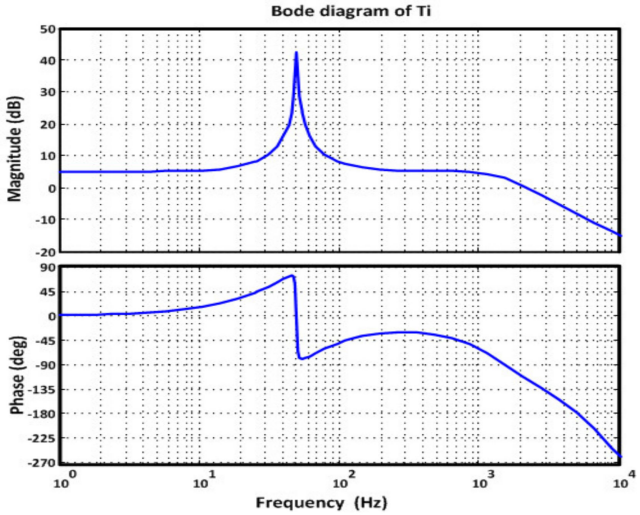

Figure 5. Bode diagram of inverter current loop.

3.2. Voltage Controller Design

The voltage controller design is done with the average current control (ACC) scheme. This controller regulates the inverter output $\hat{v}_o$ and provides a fixed reference for the current controller. The transfer functions of interest for the voltage-loop controller design relate the output voltage with the work cycle, Gvo_d(s), and the output voltage with $\hat{v}_c$, Gvo_vc(s), as determined by Equations (14)–(16):

$$\mathrm{Gv_{o}\_d(s)} = \left.\frac{\hat{\mathrm{v}}_\mathrm{o}}{\hat{\mathrm{d}}}\right|_{\hat{\mathrm{i}}_\mathrm{DC}=\hat{\mathrm{i}}\mathrm{o}=0} = \frac{2\cdot \mathrm{V_{DC}}\cdot \mathrm{Z_a}}{\mathrm{Z_a}+\mathrm{s}\cdot \mathrm{L}}, \tag{14}$$

$$\mathrm{G_{vo\_v_c}(s)} = \frac{\hat{\mathrm{v}}_\mathrm{o}}{\mathrm{i_L}}\cdot\frac{\hat{\mathrm{i}}_\mathrm{L}}{\hat{\mathrm{v}}_\mathrm{C}} = \frac{\hat{\mathrm{v}}_\mathrm{o}}{\hat{\mathrm{d}}}\cdot\left(\frac{\hat{\mathrm{i}}_\mathrm{L}}{\hat{\mathrm{d}}}\right)^{-1}\cdot\frac{\hat{\mathrm{i}}_\mathrm{L}}{\hat{\mathrm{v}}_\mathrm{C}} = \frac{\hat{\mathrm{v}}_\mathrm{o}}{\hat{\mathrm{v}}_\mathrm{C}}, \tag{15}$$

where:

$$\mathrm{G_{iL-Vc}(s)} = \frac{\hat{\mathrm{i}}_\mathrm{L}}{\hat{\mathrm{v}}_\mathrm{c}} = \frac{\mathrm{T_i(s)}}{\mathrm{R_i}\cdot(1+\mathrm{T_i(s)})}, \tag{16}$$

The design incorporates the following control configurations: proportional integral-proportional plus resonant (PI-P + ResC) and two degrees of freedom plus repetitive controller (2DOF + RC). These controllers aim at getting good reference tracking and reducing the harmonic distortion of the output voltage when the inverter feeds linear and nonlinear loads. Considering that the voltage-loop controller sets the reference for the current-loop controller, the former must be designed with a smaller bandwidth.

3.2.1. 2DOF + RC Design

The 2DOF + RC control configuration is made up of two controllers, a two-degree-of-freedom controller (2DOF) plus a repetitive controller (RC). Particularly, the 2DOF controller is initially implemented so that its design guarantees the overall stability of the energy conversion system, allowing at the same time an adequate setpoint tracking and better perturbances rejection. This is achieved by implementing a controller in the direct loop whose objective is to provide an adequate setpoint tracking, the other controller is implemented in the feedback loop and its objective is to improve the disturbances rejection. Particularly, in this work a PI + RC control is implemented in the direct loop and a P controller in the feedback loop. It is highlighted that the repetitive controller that is located in the direct loop, is added to the disturbance rejection task that the controller P attends designed for the feedback loop; which increases the robustness of this control configuration. This control configuration presents at low frequency a closed loop impedance with resistive characteristics, however, at higher frequencies it presents an inductive characteristic. These

characteristics make it necessary to implement a resistive virtual impedance loop and choose a droop scheme with these characteristics, to allow parallel connection of inverters.

The design of the 2DOF + RC controller is based on the scheme of Figure 6 and is subdivided into two stages. In the first stage, the control scheme of two degrees of freedom is designed and finally, in order to improve the level of rejection to disturbances, the RC controller is added. Figure 6 shows the detail of the voltage loop; the current loop is presented as a closed-loop transfer function $Gv_{o}\_v_{c}$. The RC(s) block represents the repetitive controller and C1(s) and C2(s), represent classical controllers.

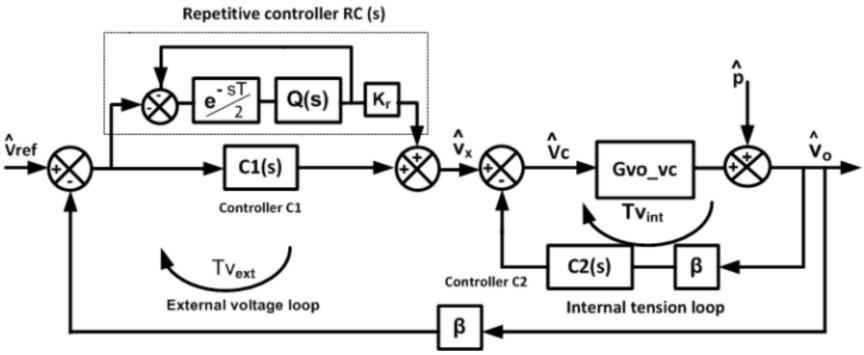

Figure 6. Block diagram for 2DOF + RC control. The current loop is closed.

The 2DOF control configuration aims at designing the C1(s) controller to perform an accurate tracking of the *OP*, and the C2(s) controller to carry on an appropriate level of disturbance rejection; that is, implementing both controllers imply that Equations (17) and (18) are fulfilled, and that the response in both situations quickly dampens, with zero error in steady state.

$$G_{vo\_vref} = \frac{\hat{v}_o}{\hat{v}_{ref}} \approx \frac{1}{\beta}, \tag{17}$$

$$G_{vo\_p} = \frac{\hat{v}_o(s)}{\hat{p}(s)} \approx 0, \tag{18}$$

The design of these controllers must meet the condition in Equation (19) [13].

$$\lim_{s \to 0} \frac{C2(s)}{C1(S)} = 0, \tag{19}$$

For designing purposes, a *PI* controller action is recommended for the C1(s) controller, and a proportional action for the C2(s) controller. These controllers will have the objective of providing the system with an adequate tracking setpoint and disturbance rejection, respectively.

The C1(s) and C2(s) controllers design begins with the closed-loop transfer function that relates the response of the system to the perturbation input in Equation (20). Considering that this response involves both controllers, a simplifying design step is taken by considering Equation (21).

$$G_{vo\_p} = \frac{\hat{v}_o(s)}{\hat{p}(s)} = \frac{1}{1 + C1(s) + C2(s) * Gvo\_vc(s) * \beta}, \tag{20}$$

where:

$$C(s) = C1(s) + C2(s). \tag{21}$$

Then:

$$G_{vo\_p} = \frac{\hat{v}_o(s)}{\hat{p}(s)} = \frac{1}{1 + C(s) * Gvo\_vc(s) * \beta} \tag{22}$$

The designing steps are:

Step 1.

Initially, C(s) is designed for the system to show an appropriate response $\hat{v}_o$ to an input disturbances signal $\hat{p}$, assuming that the input reference is zero.

Given the dynamical features of the power plant under discussion, a PI(s) controller with the structure shown in (23) is proposed as a first approach to the expected solution. This controller is designed with adequate disturbance rejection levels and appropriate stability parameters. Its design is recommended for a frequency two times smaller than the crossing frequency of the current loop.

$$C(s) = PI(s) = K \cdot (s + a)/s. \tag{23}$$

Step 2.

The C1(s) controller design has the main objective of providing the system with an adequate tracking setpoint, assuming that the perturbation input is zero. This design is based on Equation (24) that relates the system response $\hat{v}_o$ with the reference input $\hat{v}_{ref}$.

$$G_{vo\_vref} = \frac{\hat{v}_o}{\hat{v}_{ref}} = \frac{Gvo\_vc * C1(s)}{1 + C1(s) + C2(s) * Gvo\_vc(s) * \beta} \tag{24}$$

In turn, Equation (24) may be rewritten as (25).

$$G_{vo\_vref} = \frac{\hat{v}_o}{\hat{v}_{ref}} = \frac{Gvo\_vc * C1(s)}{1 + C(s) * Gvo\_vc(s) * \beta} \tag{25}$$

Once the C(s) and C1(s) controllers have been designed, we design C2(s). Solving C2(s) from Equation (21), the design features of the C2(s) controller get determined from Equation (26).

$$C2(s) = C(s) - C1(s), \tag{26}$$

Following this strategy and checking that the conditions imposed by Equations (17)–(19) are met, the controllers C1(s) and C2(s) are designed. In the event that they are not met, we return to Step 1, and a new controller C(s) is proposed. This new scheme must contain an integral part that guarantees the disturbances rejection. A proposal for this second iteration can be of the form.

$$C(s) = k \frac{(s + a)(s + b)}{s(s + c)}, \tag{27}$$

Considering the above conditions, the C1(s) and C2(s) controllers have the following values:

$$C1(s) = 0.10988 * \frac{s + 5700}{s}, \tag{28}$$

$$C2(s) = 3144 * \frac{1}{s + 8200}, \tag{29}$$

On the other hand, in order to improve the level of rejection of disturbances, ensuring that the global stability of the system is not affected, it is proposed to design a repetitive RC(s) controller. Its design is based on Equations (30) and (31).

$$RC(s) = \frac{Q(s) \cdot e^{-sT}}{1 - Q(s) \cdot e^{-sT}} * Kr, \tag{30}$$

$$Q(s) = \frac{1}{\frac{s^2}{\omega_q^2} + \frac{2\varepsilon}{\omega_q} s + 1}. \tag{31}$$

where:

Q(s) = represents a low-pass filter of infinite response, to second order pulse;
e^{-sT} = represents a delay;
$T = 0.02$ s;

$\omega_q = 2 * \pi * f_q$ (rad/seg) (cut frequency);
$\varepsilon = 0.707$ (damping factor);
f_q = 400 Hz;
Kr = 0.5 (repetitive controller gain).

The f_q and Kr terms are chosen to provide adequate stability levels.

Applying block algebra to Figure 6, the gain in the voltage-loop 2DOF plus Repetitive Controller (2DOF + RC) is expressed by (32):

$$Tv(s) = [C1(s) + RC(s) + C2(s)] \cdot G_{vo\_vc} \cdot \beta, \quad (32)$$

On the other hand, the voltage loop gain considering a PI plus RC controller is:

$$Tv(s) = [C1(s) + RC(s)] \cdot G_{vo\_vc} \cdot \beta \quad (33)$$

In Figure 7, voltage loop open-loop gain Bode diagram with 2DOF + RC control and with PI + RC controller is shown, observing that for similar Nyquist stability design criteria ((crossover frequency) fc = 978 Hz, (phase margin) PM = 92.5°, (Gain margin) GM = 6.2 dB); the 2DOF + RC controller has a higher gain at the load harmonics frequency, which guarantees a higher disturbances rejection. This behavior is observed in the blue graph, where it is justified that for the fundamental frequency (50 Hz), 3rd, 5th, 7th, and 9th load harmonic, the gains that are presented are higher; another important aspect is that the resulting phase with the 2DOF + RC controller design presents a resistive characteristic close to 0°, which contrasts with the PI + RC controller phase, which at frequencies close to 1 kHz presents an inductive character, which results in to present a lower disturbances.

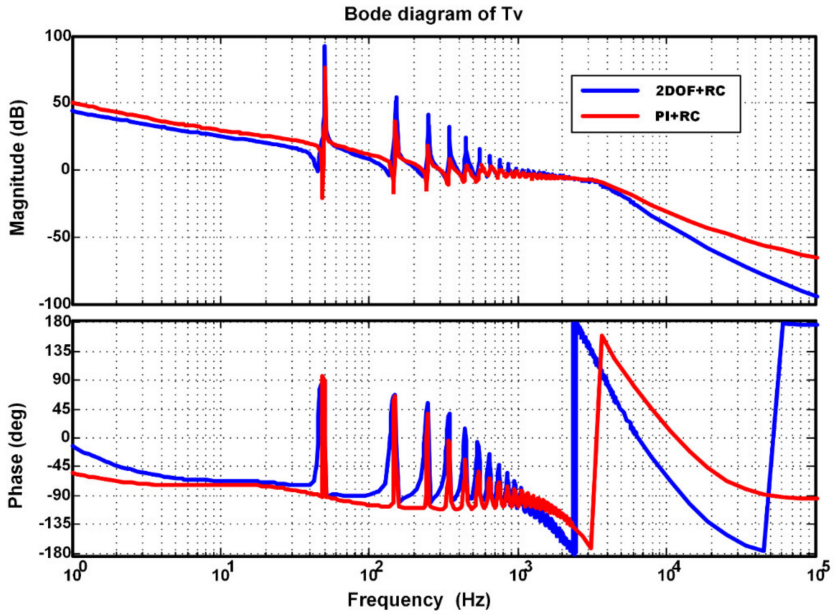

Figure 7. Bode diagram of the voltage loop using 2DOF + CR and PI + RC controller.

3.2.2. PI-P + ResC

The PI-P + ResC control configuration consists of a proportional–integral–proportional (PI-P) controller plus a resonant controller. This configuration contains an integral proportional control in the direct loop, plus a resonant controller and a proportional controller in the feedback loop. As in the previous control configuration, the PI-P controller is designed to warrant the overall stability of the conversion system and the resonant control is designed and implemented to improve upon the disturbances rejection, helping in the task performed by the P controller, implemented in the feedback loop. Particularly, this control configuration presents a closed-loop impedance with resistive characteristics at the

inverter output, in a wider frequency range than with the previous controller; thus, it is not necessary to implement a virtual impedance loop and a resistive droop scheme can be chosen directly.

A schematic of the PI-P + resonant controller is shown in Figure 8. The purpose of this controller is to provide the system with adequate disturbance rejection for linear and non-linear loads, while keeping accurate tracking and considering that the energy conversion units should be parallel connected to take care of load surges. The detail of this design is published elsewhere [30].

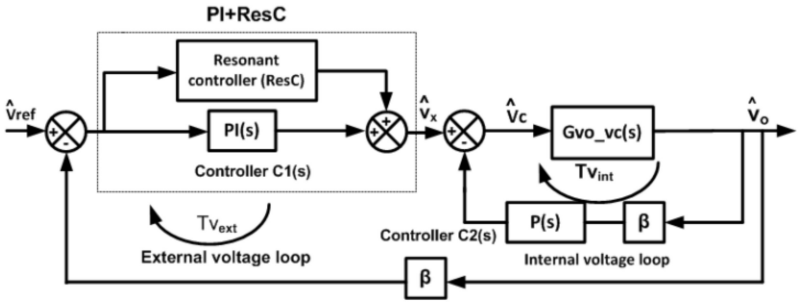

Figure 8. Block diagram for PI-P + ResC.

The basic idea of PI-P control is to prevent large control signals that can cause saturation phenomena within the system. Adding the resonant driver improves the disturbances rejection due to the presence of non-linear loads, keep good track of the set point.

Controller C2(s) was adjusted to have adequate rejection of disturbances following the recommendation that its bandwidth be less than that of the current loop.

$$C2(s) = 0.3, \tag{34}$$

On the other hand, the controller C1 aims to present good setpoint tracking with status error null stationary. For this application, the controller that meets this characteristic is as follows.

$$C1(s) = 0.080266 \cdot \frac{s + 11600}{s}, \tag{35}$$

The next step is to design the resonant controller. As shown in Figure 8, this is in parallel with the control C1 (s). This controller is designed so that its insertion does not affect the overall stability of the system and its objective is to contribute to the disturbances rejection and to provide a high gain in harmonic frequencies produced by the load.

The resonant controller design parameters of Equation (36) are given in Table 2.

$$ResC = \sum_{h=1}^{11} \frac{K_h * B_h * s}{s^2 + B_h * s + (\omega_h^2)}, \tag{36}$$

Table 2. Resonant controller parameters.

Harmonic	K_h		B_h	
1	K1	50	B1	2·π·0.3
3	K3	35	B3	2·π·0.9
5	K5	20	B5	2·π·1.5
7	K7	20	B7	2·π·2.1
9	K9	20	B9	2·π·2.7
11	K11	20	B11	2·π·3.3

The voltage-loop gain Tv(s) for PI-P + ResC is given by:

$$T_{V(s)ext} = [C1(s) + ResC] * G_{int}(s) * \beta, \quad (37)$$

On the other hand, the voltage loop gain considering a PI plus ResC controller is.

$$T_{V(s)ext} = [C1(s) + ResC] * \beta \quad (38)$$

Figure 9 shows voltage loop open-loop gain Bode diagram of PI-P + ResC control and the of PI + ResC controller, observing that with equal Nyquist stability design criteria: (phase margin 58.2°, gain margin 7.6 dB and bandwidth of 980 Hz); in the PI-P + ResC control configuration; more resonant can be designed. Particularly, resonant are implemented at the signal fundamental frequency and the load harmonics: 3rd, 5th, 7th, 9th, and 11th. This contrasts with the resonant number that can be implemented with the PI + RC control configuration; that is, for the same crossover frequency, only resonant at voltage signal fundamental frequency and load frequency harmonics could be implemented: 3rd, 5th, and 7th. An important aspect is that both configurations have a resistive phase with a phase close to 0°. This finally allows that the configuration PI-P + ResC presents a greater disturbances rejection.

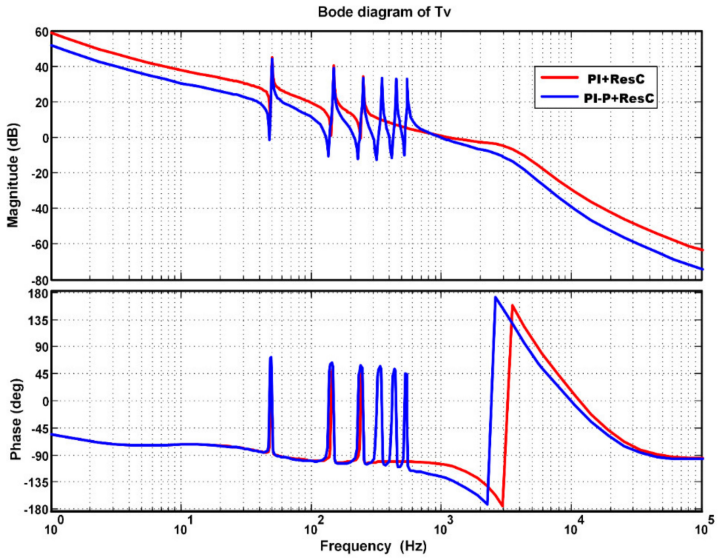

Figure 9. Bode diagram of the voltage loop using PI-P + ResC and PI + ResC controller.

4. Droop Schemes

This scheme has two advantages, the first one being the setting of a dynamic voltage reference responsive to the active and reactive power of the load demand. This is based on the possibility of connecting several inverters in parallel, without the need of using concentrated control or master–slave control. The second advantage is that it is not necessary to send control signals throughout different communication channels [31]. The behavior of the droop scheme is represented by Equations (39) and (40).

$$f - f_0 = -k_p(Pa - P_0), \quad (39)$$

$$U - U_0 = -k_q(Q - Q_0), \quad (40)$$

where:

f_0 = frequency nominal;
U_0 = nominal voltage;
P_0 = active power of the inverter at the reference point;
Q_0 = reactive power of the inverter at the reference point.

The frequency and voltage features of the *droop* control are functions of the active and reactive power demanded by the load. Equations (35) and (36) show that adjusting active power *Pa* and reactive power Q modify voltage amplitude and frequency, respectively.

5. Impedances

5.1. Inverters Output Impedance

The power distribution amongst converters units is directly affected by the inverter output impedance closed-circuit and defines the droop control strategy to use in the inverter parallel connection units. In addition, an adequate design of output impedance may reduce the impact of unbalance in the line impedance. When Z_{olc} is only inductive (Z_{olc} = jX), the phase is 90° and 0° when Z_{olc} is only resistive.

For this application, a droop scheme with resistive characteristics was chosen, considering that the calculations of the inverter closed-loop output-impedance pointed towards such feature. That is, with the inverter current and voltage loop controller implementation [32].

5.2. Virtual Impedance Loop

The traditional *droop* method is inadequate if the inverters parallel connected share non-linear loads, since the control units must consider the harmonics of the current signal, while balancing the active and reactive power [33–35]. Under this assumption, novel and fast control loops have been proposed, called virtual impedance loops. These controllers adjust the inverter output impedance closed-circuit to warrant their impedances to be resistive [36] or, sometimes, inductive [37]. Figure 10 exhibits a block-diagram that shows the inverters control-loops, including the virtual impedance loop.

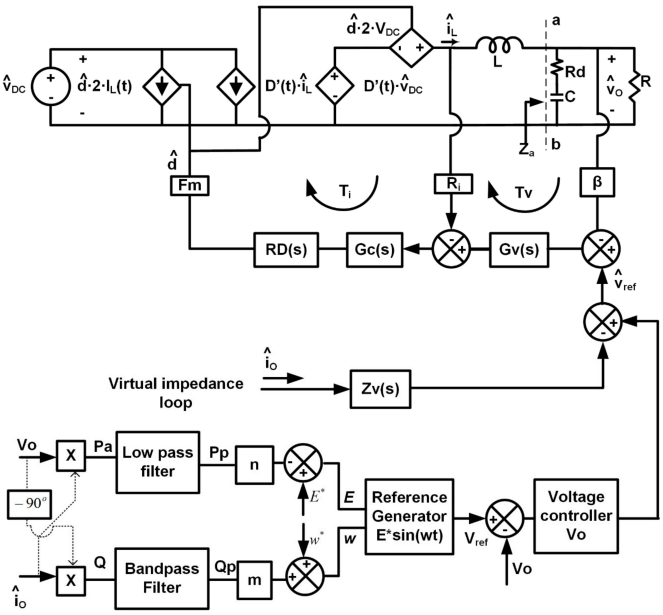

Figure 10. Small-signal model and block diagram of the closed loop system.

To be able to estimate the inverters closed-loop/open-loop output impedance ($Z_{O\_LC}(s)$ and $Z_{O\_LA}(s)$, respectively), it is necessary to start from the small signal analysis, as shown in Figure 10.

The transfer function $Z_{O\_LA}(s)$ is obtained making $\hat{v}_{DC} = \hat{v}_C = 0$; i.e., assuming that there are no voltage variations in the DC_Link. Za(s) in Equation (41) is the impedance connected to the right of the inverters output-filter inductor.

$$Z_a(s) = \frac{R \cdot (s \cdot C \cdot R_d + 1)}{s \cdot C \cdot (R_d + R) + 1}, \quad (41)$$

Applying Kirchhoff's laws to the small-signal model in Figure 10, considering that $\hat{v}_{DC} = 0$, Equation (42) is obtained:

$$Z_{O\_LA} = \frac{\hat{v}_o}{\hat{i}_o}, \tag{42}$$

where $\hat{i}_o$ represents the current perturbation at the inverter's output. When the voltage loop is open ($\hat{v}_C = 0$) and Equation (43), may be obtained from Figure 9.

$$\hat{d} = K(s) \cdot \hat{i}_L, \tag{43}$$

where, $K(s) = -Fm \cdot Ri \cdot Gs(s) \cdot RD(s)$.

$$\hat{v}_o = (\hat{i}_L - \hat{i}_o) \cdot Z_a, \tag{44}$$

Considering:

$$2V_{DC} \cdot K(s) \cdot \hat{i}_L = s \cdot L \cdot \hat{i}_L + \hat{v}_o, \tag{45}$$

Solving $\hat{i}_L$ from (45):

$$\hat{i}_L = \frac{\hat{v}_o}{2V_{DC} \cdot K(s) - s \cdot L}, \tag{46}$$

Substituting (46) in (44), gives:

$$\hat{v}_o = \left(\frac{\hat{v}_o}{2V_{DC} \cdot K(s) - s \cdot L} - \hat{i}_o \right) \cdot Z_a, \tag{47}$$

From Equation (48), the following expression results:

$$\hat{v}_o \cdot \left(1 - \frac{Z_a}{2V_{DC} \cdot K(s) - s \cdot L} \right) = -\hat{i}_o \cdot Z_a, \tag{48}$$

Finally, from Equation (49) the open-loop inverter's output impedance is given by:

$$Z_{O_{LA}}(s) = \left. \frac{\hat{v}_o}{\hat{i}_o} \right|_{\hat{v}_C = 0} = \frac{-Z_a (2V_{dc} \cdot K(s) - s \cdot L)}{2V_{dc} \cdot K(s) - s \cdot L - Z_a}, \tag{49}$$

The inverter output impedance closed loop is given in Equation (50), where Tv(s) represents the different gains in the voltage loops obtained by applying the controllers used for this purpose.

$$Z_{O\_LC}(s) = \left. \frac{\hat{v}_o}{\hat{i}_o} \right|_{\hat{V}_{DC} = \hat{v}_{Ref} = 0} = \frac{Z_{o-LA}(s)}{1 + T_V(s)}, \tag{50}$$

From Figure 10, it is possible to determine the virtual impedance loop that is obtained with (51).

$$Z_{O\_LC\_}Z_V(s) = Z_{O\_LC}(s) + Z_V(s) * G_{vo\_vref}(s), \tag{51}$$

where

$$G_{vo\_vref}(s) = \frac{1}{\beta} \cdot \frac{T_V(s)}{1 + T_V(s)}, \tag{52}$$

The value of $Z_{V(s)}$ must be larger than $Z_{O\_LC}(s)$ and the maximum line impedance expected. For the present application, the value assigned to the virtual impedance was $Z_{V(s)} = R = 0.2$.

Applying Equations (42) and (43), and using Bode diagrams, the inverter's closed-loop output impedance characteristic is obtained, with or without virtual impedance, for each of the controllers implemented in the voltage loop and the controller in the current loop.

Figure 11 evinces the effect of the two implemented controllers. The P + ResC controller, implemented in the current loops, and 2DOF + RC controller, implemented in the

voltage loops; without implementing the virtual impedance loop, at low frequency, the inverter's closed-loop output impedance exhibits a resistive characteristic, i.e., the phase angle is almost zero up to the fourth harmonic and then increases. In contrast, when the virtual impedance is implemented, a resistive characteristic extends over a larger range of frequency and harmonics may appear due to the load. This feature of the impedance produces less distortion to the inverter's output voltage when feeding non-linear loads, forcing a resistive *droop* scheme for the converters in-parallel connection. Simulations performed in PSIM^{TM} support these results.

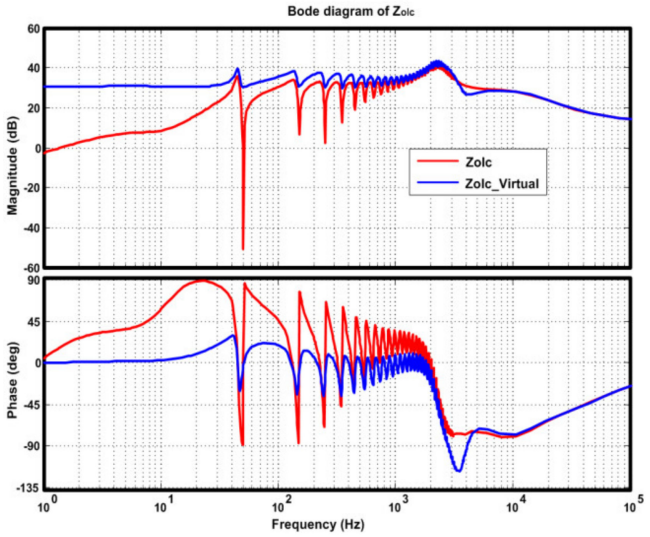

Figure 11. Bode diagram of the closed loop impedance Zo_lc with 2DOF + RC controller.

Figure 12 shows the effect of the P + ResC controller, implemented in the current loops, and PI-P + ResC controller, implemented in the voltage loops. The inverter's closed-loop output impedance is practically constant, for the fundamental frequency and harmonics of the load's current, implying a resistive behavior with phase close to 0°. It is highlighted that the observed behavior for the inverter's closed-loop output impedance occurred without implementing a virtual impedance loop. For this reason, the in-parallel connection loop was omitted. The simulations performed in PSIM^{TM} justify this procedure.

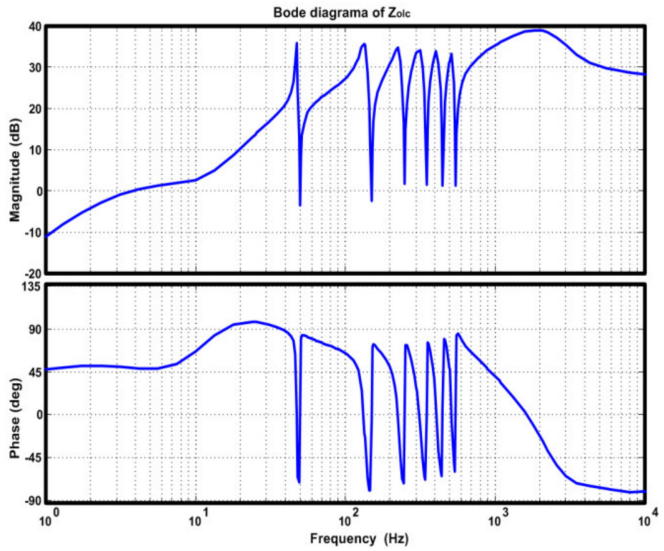

Figure 12. Bode diagram of the closed loop impedance Zo_lc with PI-P + ResC.

6. Simulation Result

The simulations were carried on by implementing the diagram in Figure 13, in the PSIM^{TM} simulator, showing the schematic of two inverters connected in parallel, with a *droop* scheme and resistive virtual impedance loop.

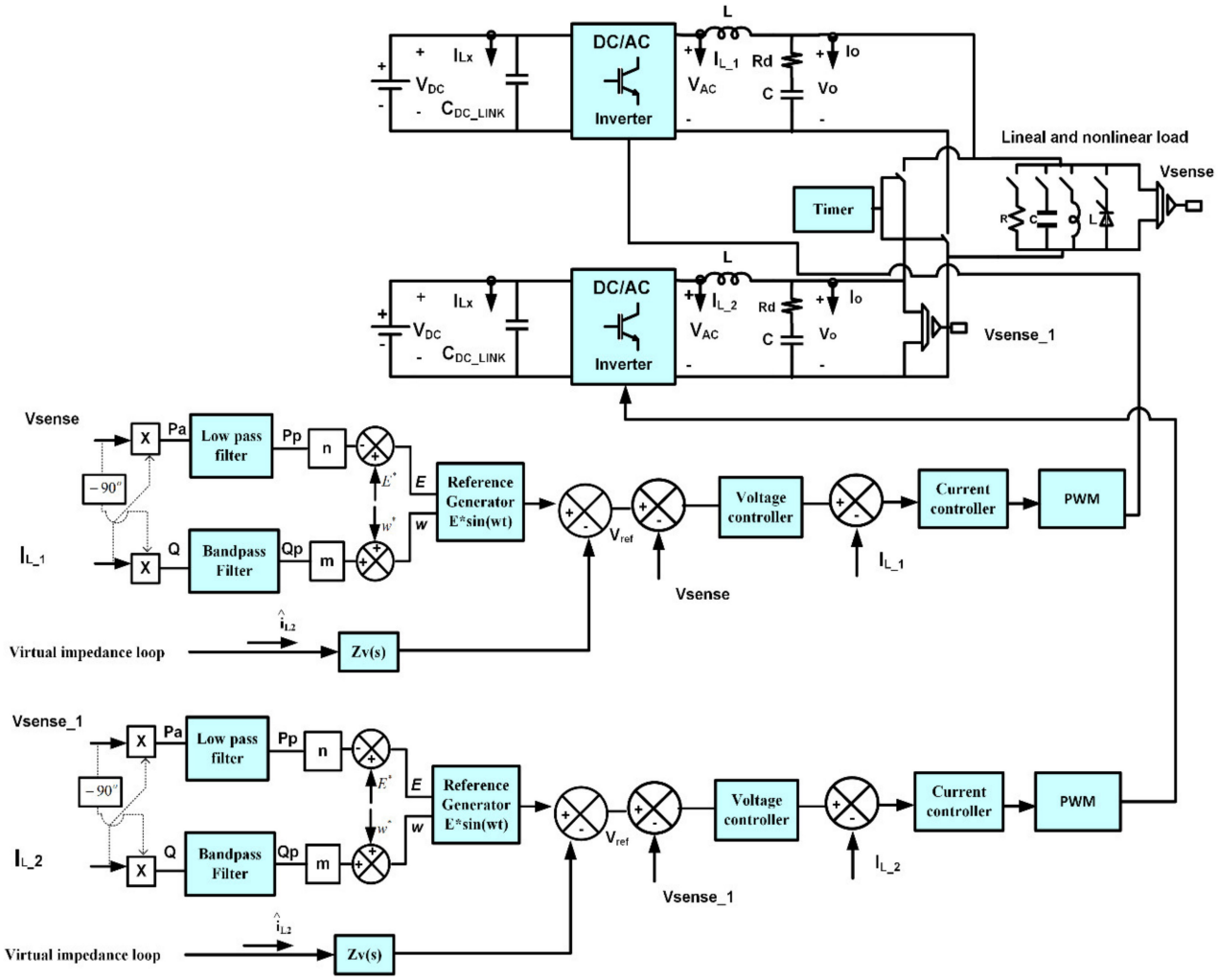

Figure 13. Schematic of two inverters connected in parallel.

The testing was performed using a resistive linear load of 170 Ω, and with a non-linear load consisting of a mono-phasic full-wave rectifying bridge, interconnected with a 96 μF capacitor and a 680 Ω resistance. This load presents a crest factor CF = 4.6.

Figure 14 shows the waveforms of the output voltage and current signals of the inverter island mode operation with the implementation of the P + ResC controller in its current loop and the PI + ResC controller in its voltage loop; the simulation is done by feeding the non-linear load mentioned above. In this figure, the voltage signal presents a distortion of 4.6%, which is justified since its waveform in the maximum and minimum peaks is not sinusoidal, presenting an amplitude of 225 V RMS value that is less than the expected one that corresponds to 230 V RMS. Additionally, the current signal has a characteristics waveform of the non-linear load. The total harmonic distortion is below the 5% recommended according to IEEE 519-1992.

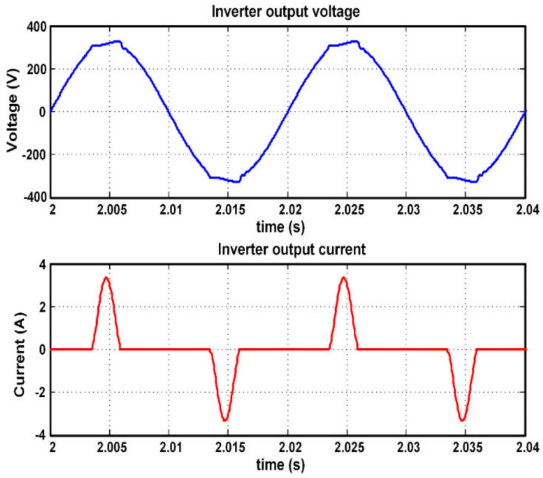

Figure 14. Waveforms of the current and voltage signal obtained with the PI + RC controller implementation in the voltage loop.

Figure 15 shows the waveforms of the output voltage and current signals of the inverter island mode operating with the implementation of the P + ResC controller in its current loop and the PI-P + ResC controller in its current loop and tension; the simulation is done by feeding the non-linear load mentioned above. In this figure, the voltage signal presents a distortion of 2.5%, which is justified since its waveform in the maximum and minimum peaks presents a more sinusoidal behavior compared to that obtained with the controller application previously presenting; being its amplitude of 229 V RMS; A value that is higher than that obtained with the previous controller implementation and is very close to the one expected, 230 V RMS. Additionally, the current presents a waveform typical of the non-linear load, being evident that the total harmonic distortion is well below the 5% that is recommended according to the IEEE 519-1992 standard.

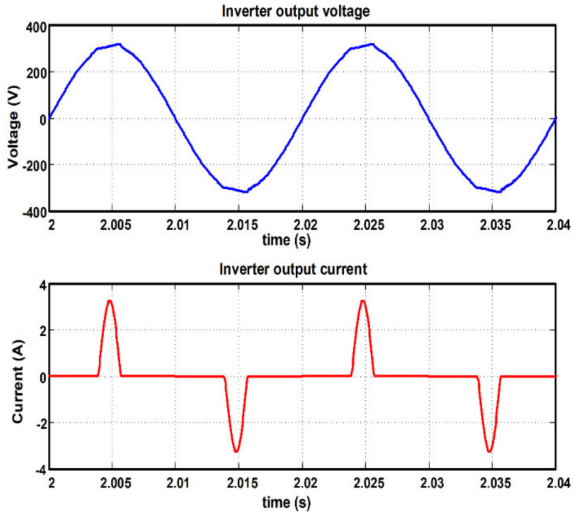

Figure 15. Waveforms of the current and voltage signal, obtained with the PI-P + ResC controller implementation in the voltage loop.

Figure 16 shows the waveforms of the output voltage and current signals of the inverter island mode operation with the implementation of the P + ResC controller in its current loop and the PI + RC controller in its voltage loop; the simulation is done by feeding the non-linear load mentioned above. In this figure, the voltage signal presents a distortion of 4.8%, which is justified since its waveform in the maximum and minimum peaks is not sinusoidal, presenting an amplitude of 226 V RMS value that is less than

the expected one that corresponds to 230 V RMS. Additionally, the current signal has a characteristics waveform of the non-linear load. The total harmonic distortion is below the 5% recommended according to IEEE 519-1992.

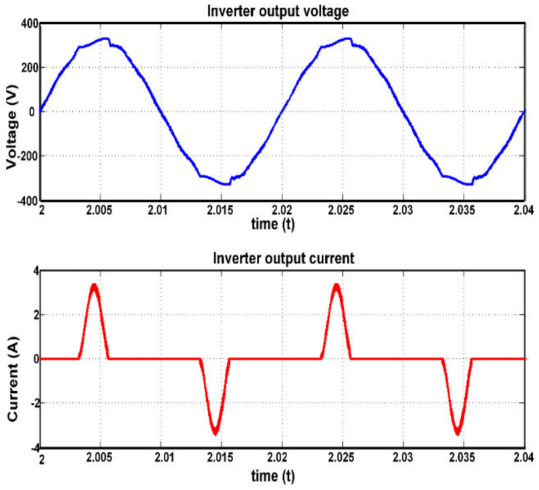

Figure 16. Waveforms of the current and voltage signal, obtained with the PI + RC controller implementation in the voltage loop.

Figure 17 shows the waveforms of the output voltage and current signals of the inverter island mode operating with the implementation of the P + ResC controller in its current loop and the 2DOF + RC controller in its current loop and tension; the simulation is done by feeding the non-linear load mentioned above. In this figure, the voltage signal presents a distortion of 2.5%, which is justified since its waveform in the maximum and minimum peaks presents a more sinusoidal behavior compared to that obtained with the controllers application introduced earlier (PI + ResC, PI-P + ResC and PI + RC), obtaining with the 2DOF + RC controller an amplitude in the voltage signal of 230 V RMS, a value that is greater than that obtained with the controllers implementation previous, this being the expected value. Additionally, the current presents a waveform that corresponds to the non-linear load, being evident that the total harmonic distortion is well below the 5% that is recommended according to the IEEE 519-1992 standard.

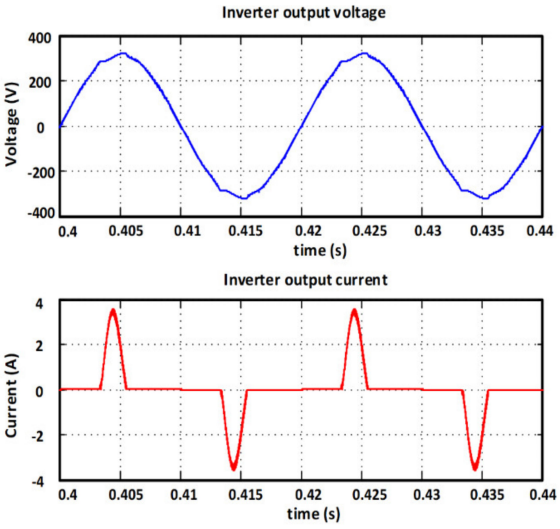

Figure 17. Waveforms of the current and voltage signal, obtained with the 2DOF + RC controller implementation in the voltage loop.

Figure 18 shows the wave shapes of voltage, current, active, and reactive power obtained with the in-parallel connection of two inverters feeding a nominal purely resistive load. The simulation was carried on with the P + ResC controller implemented in the current loop and 2DOF + RC controller implemented in the voltage loop, and a resistive virtual impedance loop. Both inverters share the load and active power, with a suitable transient response at the time of their interconnection. These results are equivalent to those obtained by applying the PI-P + ResC controllers and, therefore, are omitted.

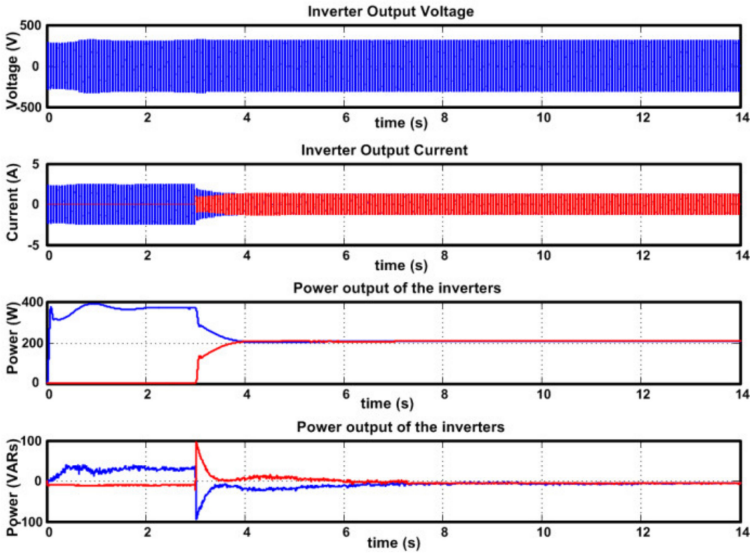

Figure 18. 2DOF + RC controller waveforms. From top to bottom: voltage, current, and power output of the inverters, with voltage loop and feeding resistive load.

Figure 19 shows a zoom-in in the time scale (12 to 12.2) of the wave shapes of the voltage, current, and power in Figure 18. The wave shape of the inverters' output voltage is kept, with an adequate balance of load and reactive power between them. These results are equivalent to those obtained by applying the PI-P + ResC controller. The simulations performed are left out.

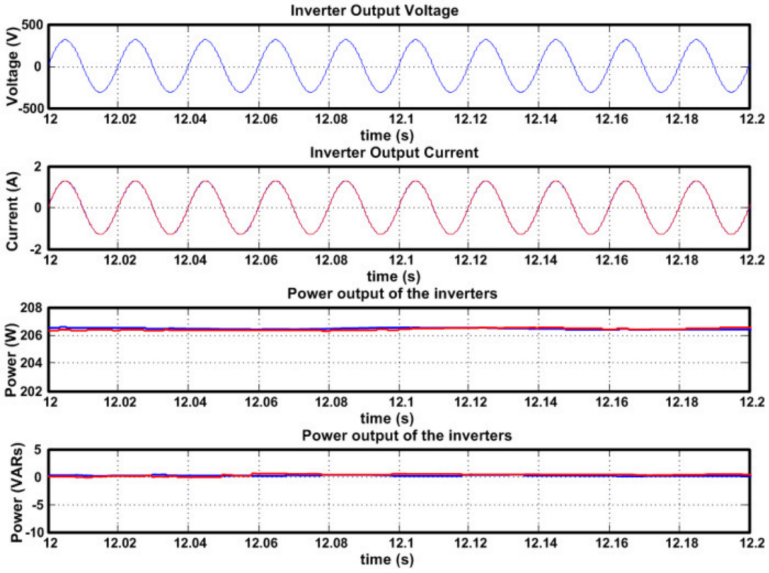

Figure 19. 2DOF + RC controller waveforms. From top to bottom: voltage, current, and power output of the inverters, with voltage loop, feeding resistive load and THDv = 1.2%.

Figure 20 shows the wave shapes of current, voltage and active power, of two inverters feeding a non-linear load. The load has a nominal value equal to one third of the total inverter's power. This simulation was carried on with the P + ResC controller implemented in the current loop, and 2DOF + RC controller, implemented in the voltage loops and a resistive virtual impedance loop. In the simulation, an appropriate transitory response at the interconnection was observed, a balanced share of load and active power between both inverters.

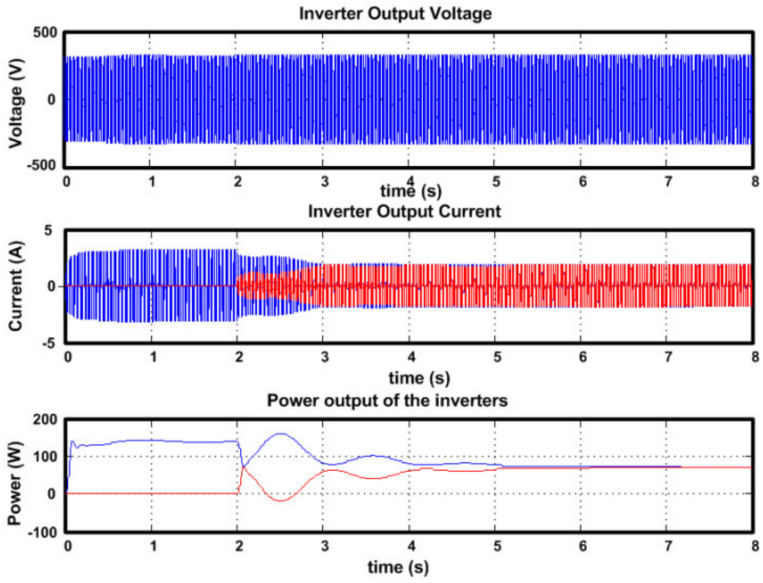

Figure 20. 2DOF + RC controller waveforms. From top to bottom: voltage, current, and power output of the inverters, with voltage loop and feeding nonlinear load.

Figure 21 shows a zoom-in of Figure 20 in the time scale (6 to 6.2) of the wave shapes of the voltage, current, and output power. In Figure 21, the output voltage signal shows a small distortion. However, the proposed control still provides a better wave shape in the output voltage of the inverters than the previously introduced controllers. Like before, the load and active power shares appear adequately balanced between both inverters.

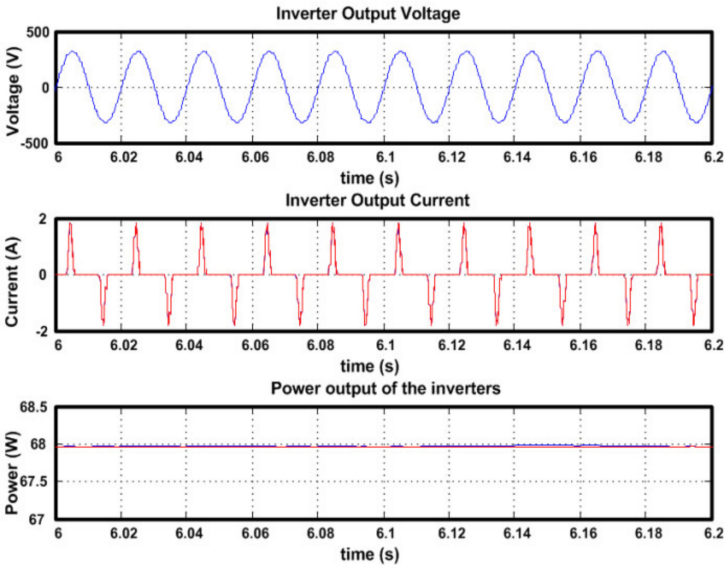

Figure 21. 2DOF + RC controller waveforms in detail, of Figure 15. From top to bottom: voltage, current, and power output of the inverters, in the time scale (6 to 6.2) and THDv = 2.1%.

Figure 22 shows the waveforms obtained from the simulation of the P + ResC and PI-P + ResC controllers, with an in-parallel configuration of two inverters feeding a non-linear load equivalent to one third of the inverter's total nominal power, without implementing a virtual impedance loop. It is possible to observe a balanced share of load and active power between inverters and an appropriate transient response when interconnected.

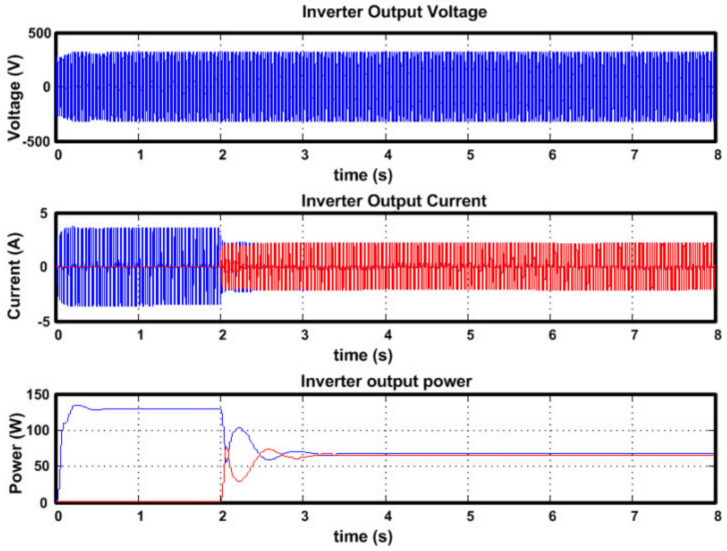

Figure 22. PI-P + ResC controller waveforms. From top to bottom: voltage, current, and power output of the inverters, with voltage loop and feeding non-linear loads.

Figure 23 shows a zoom-in of Figure 22 in the time scale (6 to 6.2) of the wave shapes of the voltage, current, and output power. The obtained signal is quite similar to the 2DOF + RC controller, because the output voltage signal also shows a small distortion. According to Figures 15 and 17, which means that implementing either the 2DOF + RC or the PI-P + ResC controllers in the voltage loop, produces an appropriate voltage waveshape at the inverters' output, with load and active and reactive powers balanced between both inverters.

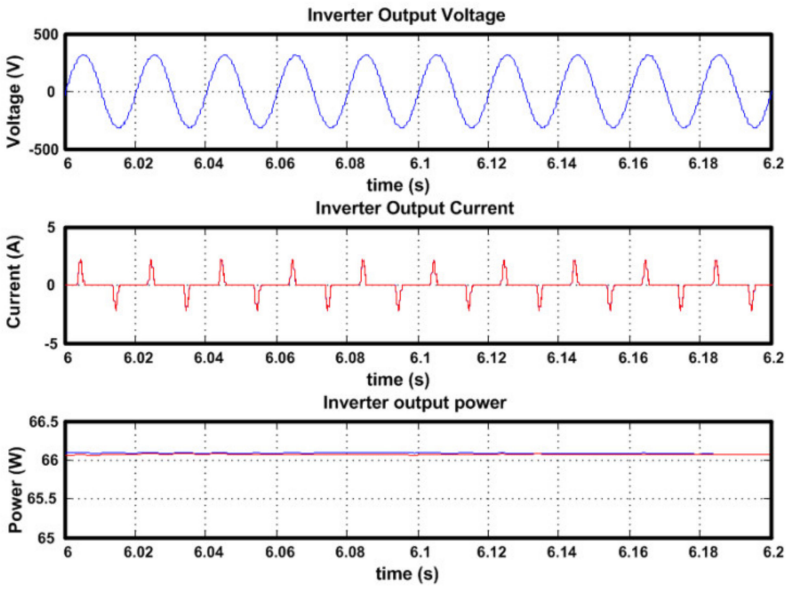

Figure 23. PI-P + ResC controller waveforms. From top to bottom: voltage, current, and power output of the inverters, with voltage loop and feeding non-linear loads, THDv = 2.5%.

7. Experimental Results

Inverter experimental tests performance feeding a non-linear load are reported, with the 2DOF + RC and PI-P + ResC controller implementation, as well as a parallel connection test of two inverters.

Experimental measurements have been carried out on the 440 W inverter described in Section 2. The controllers were implemented on a TMS320F28335 processor with a sampling frequency of 40 kHz. The sampling frequency is justified by applying the sampling theorem. The results obtained through simulations are like those obtained using experimental tests, so its presentation was not considered in this work.

The tests were performed with a resistive linear load of 170 Ω, and with a nonlinear load composed by a single-phase diode rectifier with a filter capacitance of Cf = 90 μF and a resistance of 680 Ω. It is worth pointing out that the rectifier has no input inductance, so that a highly nonlinear load results with a crest factor of CF = 4.2 and S = 130 VA when connected to an ideal sinusoidal mains voltage of 230 VRMS.

Figure 24, shows the experimental response of the output voltage and output current when the inverter powers the non-linear load using the 2DOF + RC controller. This graph shows a voltage signal with a total harmonic distortion THDv = 2.2%, a value that is below the 5% recommended by the IEEE 519-1992 standard. It is important to mention that the crest factor (CF) of this load corresponds to a value of 4.2, value that is considered high for a non-linear load. An important aspect is that the voltage signal has an amplitude of 228.5 V RMS, when the expected nominal value according to the converter operating power is 230 V RMS; which justifies the good performance of the controller. Additionally, the current signal has a characteristic form derived from the properties of the non-linear load.

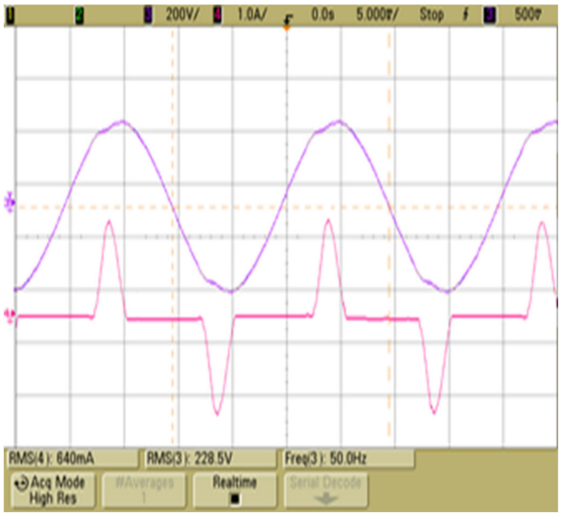

Figure 24. Inverter output voltage with nonlinear load, R2DOF (top, 200 V/div) and Inverter output current with nonlinear load, 2DOF+RC control (bottom, 1 A/div). Time scale = 5 ms/div. THDv = 2.2%.

Figure 25, shows the experimental response of the output voltage and output current when the inverter powers the non-linear load using the PI-P + ResC controller. This graph shows a voltage signal with a total harmonic distortion THDv = 2.6%, a value that is below the 5% recommended by the IEEE 519-1992 standard. It is important to mention that the crest factor (CF) of this load corresponds to a value of 4.2, value that is considered high for a non-linear load. An important aspect is that the voltage signal has an amplitude of 228.7 V RMS, when the expected nominal value according to the converter operating power is 230 V RMS, which justifies the good performance of the controller. Additionally, the current signal has a characteristic form derived from the properties of the non-linear load.

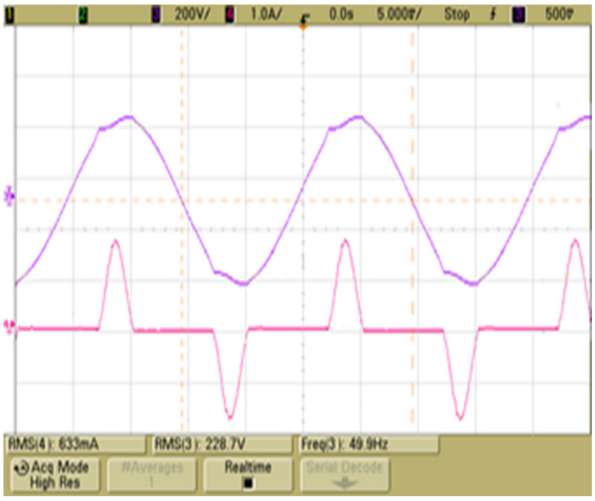

Figure 25. Inverter output voltage with nonlinear load, PI-P + ResC control (top, 200 V/div) and Inverter output current with nonlinear load, PI-P + ResC control (bottom, 1 A/div). Time scale = 5 ms/div. THDv = 2.6%.

Table 3 summarizes the inverter output voltage THDv using the four controllers feeding nonlinear loads. To load changes controllers, exhibit a good performance.

Table 3. Inverter Output Voltage THDv.

Controller	Load	THDv (%)
2DOF + RC	Nonlinear	2.2
PI-P + ResC	Nonlinear	2.6

Figure 26, PW3198, the HIOKI network analyzer was used to display the voltage and current waveforms of two inverters connected in parallel, feeding a 170 Ω resistive load. This graph shows that the two inverters share the load in a homogeneous way, supplying currents of the same intensity with values close to 1.9 A. RMS, which justifies that both inverters are synchronized and in phase. Additionally, it is observed how the voltage signal maintains its amplitude with a value close to 230 V RMS, with a sinusoidal waveform, which proves the good performance of the designed controllers.

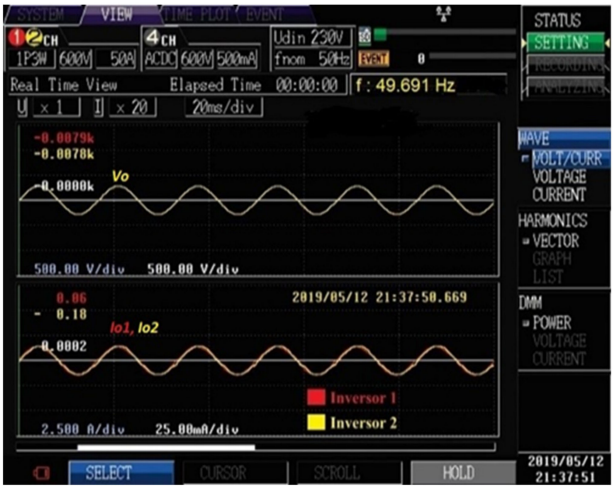

Figure 26. Waveforms of Output voltage v_O (first graph, 500 V/div), and output current of two inverters connected in parallel in grid-disconnected operation io (second graph, 3 A/div).

8. Results Discussion

This work presents the design and development of two control techniques for the grid-disconnected mode operation of an inverter. The objective of these two controllers is to provide better disturbances rejection when the converter supplies both linear and non-linear local loads. With its implementation through simulations and experimental tests, total harmonic distortion values were obtained in the voltage signal (THDv) between 1.0% and 2.5%, which represents an effective performance considering the recommendations of the IEEE 519-1992 standard, which must be less than 5%. Likewise, the parallel connection of power converters is effectively ensured. The simulations show that, at the time of interconnection and in the event of load changes, the transients present are less than 20% above the reference. Regarding the works presented in the literature, it is evident that different authors propose control strategies to reduce harmonic distortion with results close to those found in this work (THDv = 2%). Other authors propose strategies that allow the parallel connection of energy conversion units presented, with good performance. However, in this work, both strategies are proposed and implemented; that is, solutions for both the parallel connection of converters and regulators for the reduction of THDv, when the converter feeds linear and non-linear loads.

The 2DOF + RC is more robust than a repetitive controller considering that the former is designed with two controllers, one for the direct loop, and one for the feedback loop. Particularly, in the feedback loop, a controller is designed to provide larger system disturbances rejection, and the other, in the direct loop, is designed to have good setpoint tracking and contribute to the disturbance rejection task, in contrast with less robust repetitive control schemes that are normally designed in the direct loop.

The PI-P + ResC control configuration consists of two controllers: a PI + ResC controller for the direct loop and another P controller for the feedback loop. Particularly, the PI + ResC controller is designed for good setpoint tracking and the P controller for better disturbances rejection. Therefore, this control structure turns out to be more robust and presents better performance than a resonant controller, which is normally designed for direct control loop.

9. Conclusions

In the literature, control configurations have been applied to solve harmonic distortion problems for both current and voltage signals in converter applications operating in grid-connected and islanded modes. Some of these works use control configurations like resonant, repetitive, PID, control of sliding modes, and others, performing within the regulations aforementioned. In this work, two control configurations are developed and applied. The first one is configured with a control of two-degrees-of-freedom plus a repetitive control (2DOF + RC), and the second is configured with a proportional integral–proportional control plus a resonant control (PI-P + ResC). Both configurations are a new proposal in the suitable solution for problems of reduction of harmonic distortion and parallel inverter connection. These configurations combine two different control schemes in their structure to improve upon their performance. What characterizes both configurations is that a controller is implemented in the direct loop and another controller in the feedback loop, which allows to improve the performance of the converter, presenting an adequate set point tracking and, at the same time, improving the system disturbance rejection. Specifically, both control configurations allow for a steady state error equal to zero (eee = 0) and the disturbance rejection with linear and non-linear load is in the range between 1% and 2.5%, below the recommended by regulations IEEE 519-1992, which is 5%. In particular, by means of the implementation through simulations and experimental tests presented in this work, good performance of the system is justified, considering that with the implementation of these regulators, it is possible to have good set point tracking and good disturbances rejection. This causes the amplitude of the voltage signal to present values close to 230 V RMS, at 50 Hz. Additionally, inverters are successfully paralleled in response to increases in load demand. The reference voltage signal is obtained through droop schemes that allow the inverters connection in parallel to meet increases in load

demand. Particularly, for this application, a resistive droop scheme was chosen with a virtual impedance loop of the same characteristics that allows the inverters parallel connection and the homogeneous distribution of active and reactive power demanded by the load. Their choice was determined considering that with the implementation of both controllers, the inverter closed-loop impedance presents a resistive characteristic.

The controller showed the capacity to reduce the Total Harmonic Distortion (THDv) of the inverter's output below the 5% recommended by the IEEE 519-1992. THDv values of 1.2, 2.2, and 2.5% were obtained for in-parallel connected inverters feeding either a linear or non-linear load. It is worth noticing that if the PI-P + ResC controller is implemented, it is not necessary to use a virtual impedance loop.

In this work, methods are specifically described and developed so that experts in this area of knowledge can implement with certainty control strategies that allow improving the disturbances rejection in power electronic converters. Particularly, as already mentioned, for converter island mode operation. In addition, the criteria and strategies are established to effectively carry out the parallel connection of converters to meet load demands.

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References

1. Trebolle, D.; Gómez, T. Reliability Options in Distribution Planning Using Distributed Generation. *IEEE Lat. Am. Trans.* **2010**, *8*, 557–564. [CrossRef]
2. Carballo, R.; Nunez, R.; Kurtz, V.H.; Botteron, F. Design and Implementation of a Three-Phase DC-AC Converter for Microgrids Based on Renewable Energy Sources. *IEEE Lat. Am. Trans.* **2013**, *11*, 112–118. [CrossRef]
3. Del Carpio Huayllas, T.E.; Ramos, D.S.; Vasquez Arnez, R.L. Microgrid Systems: Main Incentive Policies and Performance Constraints Evaluation for their Integration to the Network. *IEEE Lat. Am. Trans.* **2014**, *12*, 1078–1085. [CrossRef]
4. Trujillo, C.L.; Velasco, D.; Figueres, E.; Garcerá, G. Analysis of active islanding detection methods for grid-connected microinverters for renewable energy processing. *Appl. Energy* **2010**, *87*, 3591–3605. [CrossRef]
5. Gomez, J.C.; Vaschetti, J.; Coyos, C.; Ibarlucea, C. Distributed Generation: Impact on Protections and Power Quality. *IEEE Lat. Am. Trans.* **2013**, *11*, 460–465. [CrossRef]
6. The Institute of Electrical and Electronics Engineers. *IEEE STD 519-1992. IEEE Recommended Practices and Requirements for Harmonic Control in Electric Power Systems*; The Institute of Electrical and Electronics Engineers: New York, NY, USA, 1993; ISBN 1-55937-239-7.
7. Converters, S.P. *IEEE Guide for Harmonic Control and Reactive Compensation of Static Power Converters*; IEEE: Piscataway, NJ, USA, 1981.
8. Hossain, M.A.; Pota, H.R.; Hossain, M.J.; Blaabjerg, F. Evolution of microgrids with converter-interfaced generations: Challenges and opportunities. *Int. J. Electr. Power Energy Syst.* **2019**, *109*, 160–186. [CrossRef]
9. Baek, S.; Cho, Y.; Yeo, S. Improved Voltage Control Scheme for Single-Phase UPS Inverter with Repetitive Current Controller. In Proceedings of the 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 29 September–3 October 2019; pp. 1482–1487. [CrossRef]
10. Jamil, M.; Waris, A.; Gilani, S.O.; Khawaja, B.A.; Khan, M.N.; Raza, A. Design of Robust Higher-Order Repetitive Controller Using Phase Lead Compensator. *IEEE Access* **2020**, *8*, 30603–30614. [CrossRef]
11. Jank, H.; Venturini, W.A.; Meurer, A.P.; Bisogno, F.; Martins, M.L.S.; Rech, C. Comparative analysis of PID, resonant and repetitive controllers applied to a single-phase PWM inverter. In Proceedings of the 2017 Brazilian Power Electronics Conference (COBEP), Juiz de Fora, Brazil, 19–22 November 2017; pp. 1–6.
12. Chen, W.; Cai, F.; Lin, Q.; Wang, W. Improved PI and Repetitive Controller for Dual-Buck Inverter. In Proceedings of the 2020 39th Chinese Control Conference (CCC), Shenyang, China, 27–29 July 2020; pp. 6157–6161.
13. Chen, Z.; Zha, H.; Peng, K.; Yang, J.; Yan, J. A Design Method of Optimal PID-Based Repetitive Control Systems. *IEEE Access* **2020**, *8*, 139625–139633. [CrossRef]

14. Pan, Z.; Dong, F.; Zhao, J.; Wang, L.; Wang, H.; Feng, Y. Combined Resonant Controller and Two-Degree-of-Freedom PID Controller for PMSLM Current Harmonics Suppression. *IEEE Trans. Ind. Electron.* **2018**, *65*, 7558–7568. [CrossRef]
15. Patil, T.D.; More, D.S. Comparative analysis of Cuk converter with proportional integral controller & proportional resonant controller. In Proceedings of the 2019 International Conference on Communication and Electronics Systems (ICCES), Coimbatore, India, 17–19 July 2019; pp. 1654–1659.
16. Sreekumar, P.; Danthakani, R.; Veettil, S.P. Implementation of proportional-resonant controller in an autonomous distributed generation unit. In Proceedings of the 2018 Advances in Science and Engineering Technology International Conferences (ASET), Abu Dhabi, UAE, 6 February–5 April 2018; pp. 1–5.
17. Torres, A.P.; Roncero-Sánchez, P.; Batlle, V.F. A Two Degrees of Freedom Resonant Control Scheme for Voltage-Sag Compensation in Dynamic Voltage Restorers. *IEEE Trans. Power Electron.* **2018**, *33*, 4852–4867. [CrossRef]
18. Iricik, S.; Komurcugil, H. Proportional-Integral and Proportional-Resonant Based Control Strategy for PUC Inverters. In Proceedings of the IECON 2018—44th Annual Conference of the IEEE Industrial Electronics Society, Washington, DC, USA, 21–23 October 2018; pp. 3369–3373.
19. Kishan, V.K.; Puthra, P.P.; Reddy, K.N. Paralleling of inverters with dynamic load sharing. In Proceedings of the 2016 IEEE 7th Power India International Conference (PIICON), Bikaner, India, 25–27 November 2016; pp. 1–6. [CrossRef]
20. Raj, D.C.; Gaonkar, D.N. Frequency and voltage droop control of parallel inverters in microgrid. In Proceedings of the 2016 2nd International Conference on Control, Instrumentation, Energy & Communication (CIEC), Kolkata, India, 28–30 January 2016; pp. 407–411. [CrossRef]
21. Sarvghadi, P.; Monfared, M. Load sharing control of parallel inverters with uncertainty in the output filter impedances for islanding operation of AC micro-grid. In Proceedings of the 2017 Conference on Electrical Power Distribution Networks Conference (EPDC), Semnan, Iran, 19–20 April 2017; pp. 55–61. [CrossRef]
22. Araki, M.; Taguchi, H. Tutorial Paper Two-Degree-of-Freedom PID Controllers. *Int. J. Control Autom. Syst.* **2003**, *1*, 4.
23. Broberg, H.L.; Molyet, R.G. Reduction of repetitive errors in tracking of periodic signals: Theory and application of repetitive control. *First IEEE Conf. Control Appl.* **1992**, *2*, 1116–1121.
24. Ogata, K.; Yang, Y. *Modern Control Engineering*, 4th ed.; Prentice Hall: Upper Saddle River, NJ, USA, 2001.
25. *PSIM 7.0, Users Guide*; Powersim Inc.: Maryland, MD, USA, 2006.
26. Mohan, N.; Underland, T.M.; Robbins, W.P. *Power Electronics: Converters, Applications, and Design*, 3th ed.; John Wiley & Sons: Hoboken, NJ, USA, 2003.
27. Vorperian, V. Simplified analysis of PWM converters using model of PWM switch. II. Continuous conduction mode. *IEEE Trans. Aerosp. Electron. Syst.* **1990**, *26*, 490–496. [CrossRef]
28. Zmood, D.N.; Holmes, D.G. Stationary frame current regulation of PWM inverters with zero steady-state error. *IEEE Trans. Power Electron.* **2003**, *18*, 814–822. [CrossRef]
29. Benavent, J.M.; Figueres, E.; Garcera, G.; Pascual, M. Robust model-following regulator for average current-mode control of boost DC-DC converters. In Proceedings of the IEEE International Symposium on Industrial Electronics, Dubrovnik, Croatia, 20–23 June 2005; Volume 2, pp. 715–720.
30. Ortega Gonzalez, R.; Sosa Saavedra, J.C.; Carranza Castillo, O.; Garcia Ortega, V. Comparison controllers for inverter operating in island mode in microgrids with linear and nonlinear loads. *IEEE Lat. Am. Trans.* **2014**, *12*, 1441–1448. [CrossRef]
31. Kawabata, T.; Higashino, S. Parallel operation of voltage source inverters. *IEEE Trans. Ind. Appl.* **1988**, *24*, 281–287. [CrossRef]
32. Guerrero, J.M.; de Vicuña, L.G.; Matas, J.; Miret, J.; Castilla, M. Output impedance design for parallel-connected UPS inverters. In Proceedings of the IEEE International Symposium on Industrial Electronics (ISIE'04), Ajaccio, France, 4–7 May 2004.
33. Jensen, U.B.; Blaabjerg, F.; Enjeti, P.N. Sharing of nonlinear load in parallel connected three-phase converters. In Proceedings of the IEEE Industry Applications Annual Meeting (IAS'00), Rome, Italy, 8–10 October 2000; Volume 4, pp. 2338–2344.
34. Zhong, Q.C.; Blaabjerg, F.; Guerrero, J.M.; Hornik, T. Reduction of voltage harmonics for parallel-operated inverters. In Proceedings of the IEEE Energy Conversion Congress and Exposition, Phoenix, AZ, USA, 17–22 September 2011; pp. 473–478.
35. Borup, U.; Blaabjerg, F.; Enjeti, P.N. Sharing of nonlinear load in parallel-connected three-phase converters. *IEEE Trans. Ind. Appl.* **2001**, *37*, 1817–1823. [CrossRef]
36. Guerrero, J.M.; Berbel, N.; Matas, J.; de Vicuna, L.G.; Miret, J. Decentralized Control for Parallel Operation of Distributed Generation Inverters in Microgrids Using Resistive Output Impedance. In Proceedings of the 32nd Annual Conference on IEEE Industrial Electronics, IECON, Paris, France, 6–10 November 2006; pp. 5149–5154.
37. Guerrero, J.M.; de Vicuña, L.G.; Matas, J.; Miret, J.; Castilla, M. Output impedance design of parallel-connected UPS inverters with wireless load-sharing control. *IEEE Trans. Ind. Electron.* **2005**, *52*, 1126–1135. [CrossRef]