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Mathematical Modeling and Analysis of Capacitor Voltage Balancing for Power Converters with Fewer Switches

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Abstract: The multilevel inverter (MLI) has been developed as a powerful power conversion scheme for several processes, including renewable energy, transmission systems, and electric drives. It has become popular across medium- to high-power operations due to its many advantages, including minimum harmonic content, low switching losses, and reduced electromagnetic interference (EMI). In this paper, the capacitor voltage balancing technique-based pulse width modulation (PWM) has been proposed. The proposed PWM strategy offers several advantages, such as high-quality output waveforms with reduced harmonic distortion, improved efficiency, and better control over the output voltage. The Xilinx ISE 10.1 software was used for synthesizing, and the VHDL code was written for the proposed method. MATLAB software was used to simulate and hardware was used to verify the proposed system. The SPARTAN 3E FPGA was used for the generation of the PWM. This paper developed a 2 kW single-phase 15-level inverter that created an AC wave from the DC input voltage, with a total harmonic distortion (THD) of 8.02%, which was less than the THD achieved from other conventional MLI. The results indicate that MLI topologies with low total harmonic currents, fewer switches, and higher output voltage levels are better stabilized during load disturbance circumstances.

Keywords: renewable energy; power converter; total harmonic distortion; modeling; capacitor voltage

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1. Introduction

Global warming is a major environmental issue affecting the entire world. It refers to the gradual increase in the Earth's average surface temperature caused by the buildup of greenhouse gases in the atmosphere. The primary cause of global warming is human activity, particularly burning fossil fuels for energy and transportation, deforestation, and industrial processes. The impacts of global warming are far-reaching and can be felt worldwide [1,2]. Reducing greenhouse gas emissions is the most efficient approach to address global warming. It can be achieved through various strategies, such as transitioning to clean and renewable energy sources, improving energy efficiency, promoting public transportation, and implementing policies to reduce emissions from industries and agriculture [3].

A solar PV system converts sunlight into electricity using solar panels. Solar PV systems are becoming increasingly popular as a clean and sustainable alternative to traditional energy sources. A typical solar PV system consists of solar panels, an inverter, and a battery bank (optional). Solar panels consist of photovoltaic cells that convert sunlight into DC. An inverter converts the DC to AC, which powers household appliances and electronics. This output is influenced by solar radiation and temperature and is not steady [4,5]. Therefore,

it is important to obtain the most power possible out of solar PV, which is achieved by maximum power point tracking (MPPT) [6], for a PV panel to operate effectively even under numerous climatic changes throughout an annual calculation [7].

The use of an MPPT controller with this DC-to-DC converter offers several benefits. By ensuring that the solar panels operate at their maximum efficiency, the system can generate more energy, reducing the size of the solar panel array required to meet energy demands. Using a DC-to-DC converter also improves the system's efficiency by reducing losses in the power conversion process. It can lead to a more cost-effective and reliable solar PV system.

Since they have been around for over 50 years, multilevel inverters (MLIs) are gaining popularity in industrial settings as one of the fascinating ways to deploy medium- to high-power converters. Multilevel inverters are an important technology in power electronics that have gained significant attention in recent years due to their potential to provide high voltage and power quality to various applications. A multilevel inverter consists of several power electronic switches arranged in a specific configuration to produce multiple output voltage levels. The configuration for MLI depends on the number of levels and clamping used to achieve these levels.

An analytical indication for improving the quality of the alternating voltage is provided by MLI topologies [8]. Over traditional two-level inverters, MLIs offer several benefits, including a greater basic voltage at the output, reduced typical mode voltage and switch loss, less EMI, and less THD. Power electronic applications are crucial for the multilayer inverter to convert a direct current source. Several issues exist with the three-phase alternating machine and system supply PWM signaling approaches [9]. Since low-level inverters contain nonlinear elements such as MOSFET and IGBT, they may also produce waveforms with harmonics using pulse-width modulation (PWM) [10]. Nonlinear impacts such as distortion caused by harmonics develop on the outputs of load when the amount of the element has risen on the inverter. Studies have considered nonlinear impacts to reduce the impact of harmonic distortion on the operating loads of PWM inverters [11].

The cascaded H-bridge MLI consists of a succession of H-bridge inverters connected in a cascaded configuration. Each H-bridge inverter has four switches (upper arm = 2 and lower arm = 2) that switch the voltage to produce the needed DC output voltage waveform. The number of levels for the inverter is determined by the number of H-bridge modules used [12]. Increasing the DC-link voltage results in greater electromagnetic interference and voltage stress on power semiconductor devices [13]. Topologies that employ multiple levels of inverters can decrease the voltage stress of switches and EMI in the system, thus replacing the two-level inverter [14]. The cascaded H-bridge MLI offers various benefits over conventional inverters, including reduced harmonic distortion, improved voltage quality, lower EMI, higher efficiency, and a modular design. These advantages make it well suited for various applications such as renewable energy systems, motor drives, and electric vehicles.

PWM technology removes and lowers harmonics at the inverter output while controlling the output voltage. PWM serves the dual purpose of reducing or eliminating harmonics and controlling the voltage inside the inverter without an additional hardware price. With developments in MLIs, innovative modulation methods are increasingly necessary for these devices. Each modulation approach has negative and positive influences on the converter architecture and scope. The categorization of the modulation schemes for MLIs based on the difference between high- and low-frequency shifting is represented in [15]. Level shifting and phase shifting modulation schemes are two categories of PWM systems based on the waveform. To create high-quality output voltage waveforms, level shift modulated methods are commonly used in many applications [16,17].

Capacitor voltage balance (CVB) represents one of the most important problems for MLIs due to the modular design. The two primary forms of capacitor-voltage-balancing methods are arm regulation [18] and specific capacitor regulation [19]. The first approach, which necessitates a closed-loop regulation for each capacitor, must be revised for MMCs with many capacitors. The latter is the sorting and selection (SAS) approach and uses all

the capacitors in an arm. It sorts the capacitor voltages and chooses included or skipped sub-modules (SMs) by the signal of the arm current.

This PWM scheme provides periodic unneeded activation of the switches and supplies to turn up the initial level while producing a high-level voltage. The additional supply and switch action reduces the switch's lifetime and results in power loss. A new fraction sinus PWM improvement with a gap is presented in [20] on a three-phase signal processing approach. The dual DC to DC converter featuring a reverse connection for the MLI is suggested [21]. Ref. [22] discusses investigating the primary PWM operation instances and frequencies that influence this zero-crossing point.

An MLI with the fewest possible power electronic switching elements was proposed in this study. It used a multilayer inverter created in [23,24] and modified somewhat. By utilizing the inverter's series/parallel switches, the proposed MLI introduced an auxiliary network with four diodes and a toggle switch. In contrast to the traditional cascaded H-bridge inverters, just two independent source voltages were required to generate an equal number of voltage levels. Compared with existing techniques, the proposed inverter used fewer switching elements and had lower harmonics in the output voltage waveforms. The applicability of grid-tied photovoltaic systems, hybrid electric cars, etc., could be expanded using the proposed MLI design. In this proposed system, the RL load was considered from the inverter with the values of 100 Ω and 30 mH, respectively, for 11 and 15 levels of the inverter. In addition, the bottom and top inverter voltages for 11 levels were 65 V and 130 V, and those for 15 levels were 47 V and 94 V. Mathematical analyses, computer simulations, and experimental findings are provided to prove the proposed cascaded MLI's viability.

The field programmable gate arrays (FPGAs) used to implement various PWM regulators have grown progressively over the past few years. Because of their flexibility compared with other digital signal processors (DSPs), they are becoming the leading devices for employing various PWMs.

The main objective of this paper is to develop a CVB-based PWM technique for 11- and 15-level inverters. This investigation offers a new MLI design that uses two DC sources and eight power electronic components to generate 11 and 15 levels. Based on the measured findings, the proposed MLI offers high-quality, consistent output waveforms with a decreased THD. In hardware, PWM generation was carried out using SPARTAN 3 A FPGA kit.

The paper's structure is as follows: Section 2 presents the cascaded H-bridge MLI that is being proposed. Section 3 discusses the problems with the proposed inverter's capacitor voltage balancing. Section 4 illustrates the PWM pulse modeling for the proposed cascaded MLI. In Section 5, the outcomes of the proposed system are analyzed. Furthermore, Section 6 provides an overview of the conclusions drawn from this paper.

2. Proposed Cascaded H-Bridge MLI

The proposed inverter had a top and bottom inverter in which the top inverter's primary switches were triggered with high frequency, while the bottom inverter was triggered with low frequency, as shown in Figure 1. The top three-level inverter had four switches with output levels of 0, $+V_{dc}$, and $-V_{dc.}$ The bottom inverter had four basic primary switches and a second bidirectional switch, which could be increased to increase the overall level of the inverter.

2.1. Modes of Operation

Figure 2 illustrates the suggested bottom inverter's operating modes, comprising four IGBT switches and two bidirectional switches. The green color indicates the conduction of switches and capacitors [25].

Switching mode 1, depicted in Figure 2a, involved turning on switches PS_5 and PS_6 while turning off the remaining switches. This configuration produced a voltage output of 0 [26].

The system had seven different switching modes.

In switching mode 1, switches PS_5 and PS_6 were on, while the others were off, producing a voltage of 0 (Figure 2a).

In switching mode 1, switches PS_7 and PS_8 were on, while the others were off, producing a voltage of 0 (Figure 2b).

Switching mode 2 involved switches PS_8 and SS_2 being on and the others being off, resulting in a voltage of 2 V_{dc0} (Figure 2c).

Switching mode 3 entailed turning on switches PS_8 and SS_1 while keeping the others off, generating a voltage of 4 V_{dc0} (Figure 2d).

In switching mode 4, switches PS_5 and PS_8 were on, and the rest were off, yielding a voltage of 6 V_{dc0} (Figure 2e).

In switching mode 5, switches PS_6 and SS_1 were on, while the others were off, producing a voltage of -2 V_{dc0} (Figure 2f).

Switching mode 6 involved switches PS_6 and SS_2 being on and the others being off, resulting in a voltage of -4 V_{dc0} (Figure 2g).

Finally, in switching mode 7, switches PS_6 and PS_7 were on, while the rest were off, generating a voltage of -6 V_{dc0} (Figure 2h).

The various modes of operation of the proposed MLI are represented in Figure 2. The switching modes of the H-bridge inverter are illustrated in Table 1. It describes various active and non-active modes of IGBT switches.

To maintain a frequency of 50 Hz over a total period of 0.02 s, Figure 3 displays the projected seven-stage output of the suggested bottom inverter. Figures 4–7 display the direction of current flow during the charging and discharging cycles of capacitors C_1, C_2, and C_3. The dotted line indicates the charging phase, while the dashed line represents the discharging phase of the capacitors [26,27].

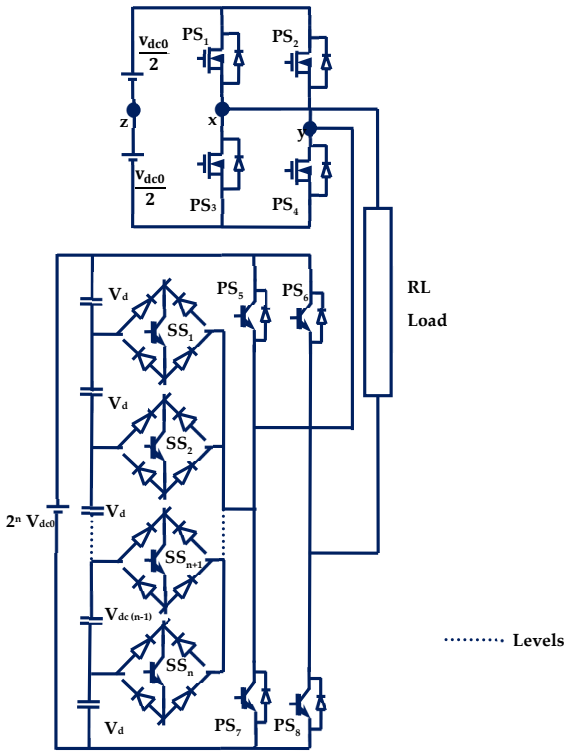

Figure 1. Proposed cascaded H-bridge multilevel inverter.

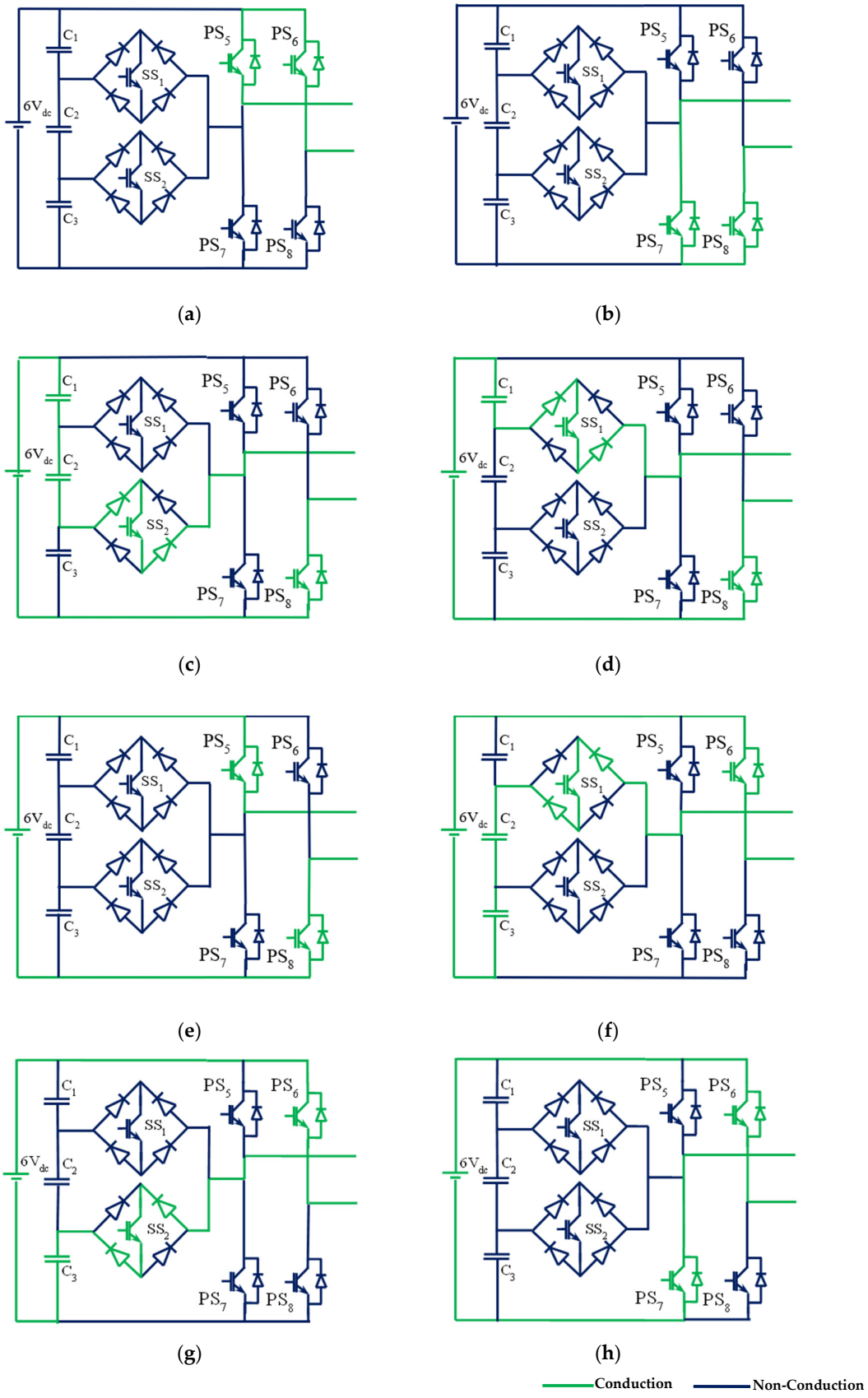

Figure 2. Mode of operation.

Table 1. Switching modes of bottom H-bridge inverter.

Switching Mode	PS5	PS6	PS7	PS8	SS1	SS2	Voltage Obtained	Reference
1	✓	✓	✖	✖	✖	✖	0	Figure 2a
	✖	✖	✓	✓	✖	✖	0	Figure 2b
2	✖	✖	✖	✓	✖	✓	2 V_{dc0}	Figure 2c
3	✖	✖	✖	✓	✓	✖	4 V_{dc0}	Figure 2d
4	✓	✖	✖	✓	✖	✖	6 V_{dc0}	Figure 2e
5	✖	✓	✖	✖	✓	✖	−2 V_{dc0}	Figure 2f
6	✖	✓	✖	✖	✖	✓	−4 V_{dc0}	Figure 2g
7	✖	✓	✓	✖	✖	✖	−6 V_{dc0}	Figure 2h
			✖—OFF | ✓—ON					

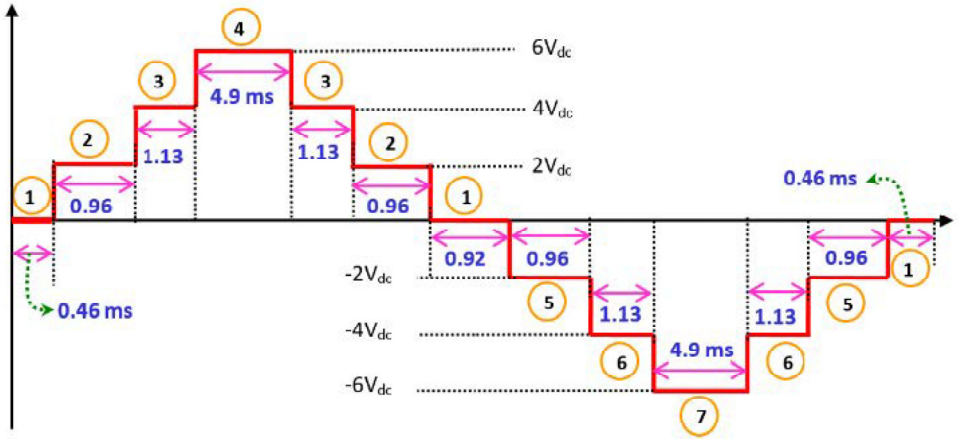

Figure 3. Predicted seven-stage output voltage waveform.

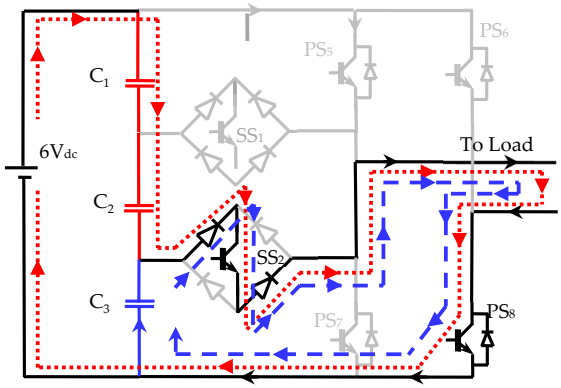

Figure 4. Direction of current flow path during mode 2 (Charging, Discharging).

2.2. Capacitor States of Bottom H Bridge Inverter

During mode 2, capacitors C_1 and C_2 were charged, and capacitors C_3 discharged. Similarly, in mode 3, capacitor C_1 charged, while capacitors C_2 and C_3 discharged, as depicted in Figure 5. During mode 5, capacitor C_1 discharged, whereas capacitors C_2 and C_3 charged.

Likewise, during mode 6, C_1 and C_2 discharged, whereas C_3 charged. Table 2 provides a detailed account of each capacitor's charging and discharging duration [28].

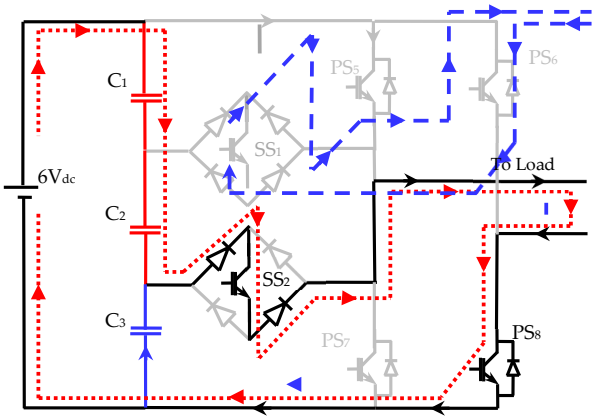

Figure 5. Direction of current flow path during mode 3 (Charging, Discharging).

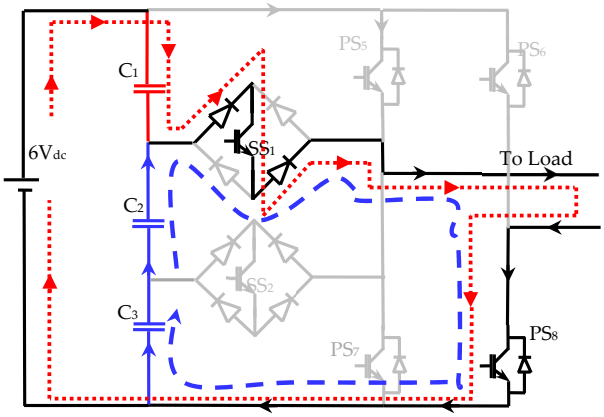

Figure 6. Direction of current flow path during mode 5 (Charging, Discharging).

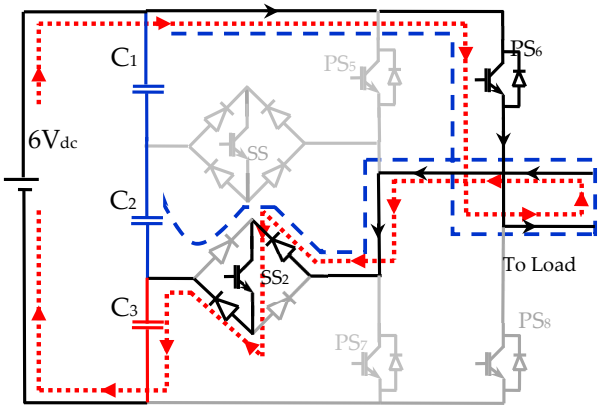

Figure 7. Direction of current flow path during mode 6 (Charging, Discharging).

From Table 2, it is concluded that

- C_1 and C_3 total charging time = 4.18 milli seconds;
- C_1 and C_3 total discharging time = 4.18 milli seconds;
- C_2 total charging time = 3.84 milli seconds;
- C_2 total discharging time = 4.52 milli seconds.

The capacitor charging and discharging times should typically be equal to be balanced. According to the information above, capacitors C_1 and C_3 had equal charging and discharging times for cycles of 20 ms and were, therefore, balanced. However, capacitor C_2 did not have an equal charging and discharging time and needed to be balanced. So, the solution

for this problem, the capacitor balancing process, was required in this proposed seven-level inverter's charging and discharging duration [28].

Table 2. Capacitor charging and discharging status of capacitors.

Switching Mode	PS_5	PS_6	PS_7	PS_8	SS_1	SS_2	Status of Capacitors			Time Duration
							C_1	C_2	C_3	
1	✓	✓	✗	✗	✗	✗	UC	UC	UC	1.84 ms
	✗	✗	✓	✓	✗	✗	UC	UC	UC	
2	✗	✗	✗	✓	✗	✓	↑	↑	↓	1.92 ms
3	✗	✗	✗	✓	✓	✗	↑	↓	↓	2.26 ms
4	✓	✗	✗	✓	✗	✗	UC	UC	UC	4.9 ms
5	✗	✓	✗	✗	✓	✗	↓	↑	↑	1.92 ms
6	✗	✓	✗	✗	✗	✓	↓	↓	↑	2.26 ms
7	✗	✓	✓	✗	✗	✗	UC	UC	UC	4.9 ms
✗—OFF | ✓—ON | UC—Unchanged										20 ms

3. Capacitor Voltage Balancing in the Proposed Inverter

The seven-level inverter was proposed to eliminate the capacitor voltage balancing problem in capacitor C_2. Thus, the total voltage in the capacitor over 20 ms became positive [16]. It could be implemented during modes 3 and 6, where the capacitor C_2 voltage decreased. Figure 8 shows the proposed capacitor voltage balancing technique, a modified switching technique. During switching stages 3 and 5, it was apparent that the proposed inverter voltage may switch among two levels.

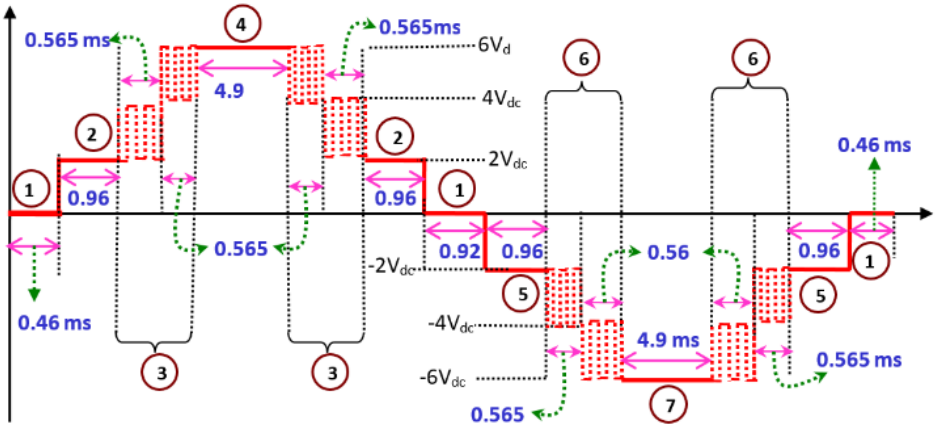

Figure 8. Proposed modified switching technique cascading top and bottom inverter.

During mode 3, the inverter voltage was shifted among 2 V_{dc} and 4 V_{dc} for the first part of the time interval and among 4 V_{dc} and 6 V_{dc} during the next part of the time interval. This reduced the discharging time of C_2 in mode 3. Because of this switching, the voltage was either in 2 V_{dc} or 6 V_{dc}, increasing the charging time of capacitor C_2. The cascaded output of the top- and bottom-level inverter is shown in Figure 9. The low switching frequency inverter (LSFI) and high switching frequency inverter (HSFI) voltages were immediately coupled to produce the load voltage. It can also be seen in Figure 9 (the magnified area) that at switching state 3 of the lower inverter, the HSFI should flip in the opposite direction of the LSFI. This was critical for switching the load voltage among 4 V_{dc} and 5 V_{dc}, as well as 5 V_{dc} and 6 V_{dc}. C_2 will begin charging in addition to C_1 and C_3 if the changed switching architecture powers the proposed inverter. As a result, the voltage over

C_2 must be monitored, and depending on its current value, either the generalized reduced switching method or the altered modulation strategy must be employed.

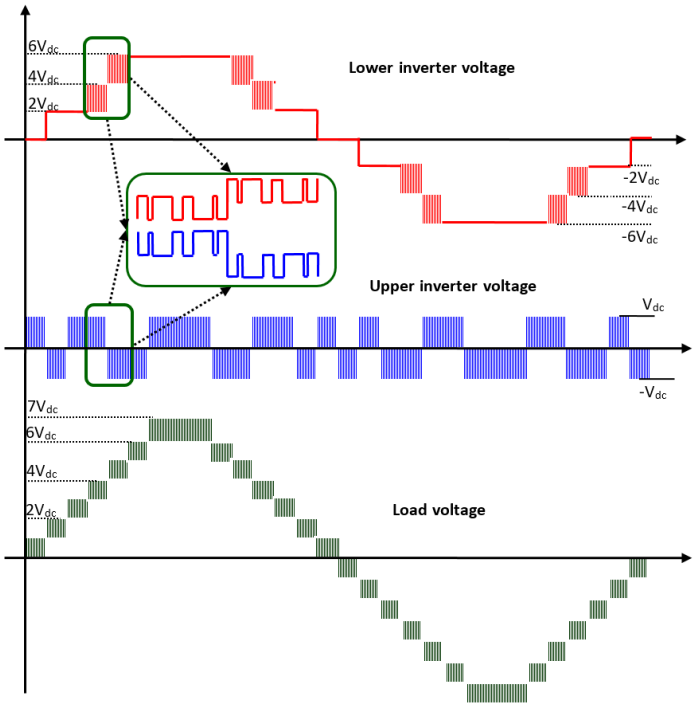

Figure 9. Top and bottom voltage waveforms and cascaded output by using modified switching technique.

4. Modeling of PWM Pulses for Proposed Cascaded Multilevel Inverter

To produce the reference waveform for the top inverter, the following Equations (1) and (2) were utilized [17]:

$$U_{ref} = A\sin(\omega t) \tag{1}$$

$$U_{ref,s} = \frac{U_{ref}}{7} \tag{2}$$

$$Z_1 = \begin{cases} 1 & \text{if } U_{ref} > 0 \\ 0 & \text{if } U_{ref} < 0 \end{cases} \tag{3}$$

$$\begin{aligned} V_{bottom,expected} &= \left(round\left(\frac{|U_{ref,s}|}{0.4} \right) * 0.4 * Z_1 \right) \\ &+ \left(round\left(\frac{|U_{ref,s}|}{-0.4} \right) * 0.4 * Z_1 \right) \end{aligned} \tag{4}$$

$$V_{top,ref} = 7 * \left(U_{ref,s} - V_{bottom,expected} \right) \tag{5}$$

Equation (3) describes the zero-crossing detector, while Equation (4) represents the projected output of the bottom inverter (V_{bottom}). Equation (5) provides a mathematical expression for the reference waveform of the top inverter. The following equations must construct and describe the reference waveform to provide the PWM for the bottom inverter:

$$V_{bottom,ref} = round\left(\frac{\left| U_{ref,S} \right|}{0.4} \right) \tag{6}$$

After generating the reference waveform, it was divided into various waves R_y.

$$X = \frac{(N-11)}{4} + 2 \tag{7}$$

where N = 11, 15, 19, 23

$$\mathrm{R}_y = \begin{cases} 1 & \text{if } U_{bottom,ref} > y \\ 0 & \text{if } U_{bottom,ref} < y \end{cases} \tag{8}$$

The total number of secondary switches required for an N-level inverter was determined after dividing by the number of different signals.

$$NAS = \frac{(N-11)}{4} + 12 \tag{9}$$

where N = 11, 15, 19, 23 . . .

The turn-on and turn-off operation of the primary switches (*PSs*) of the bottom inverter was determined by the following equations:

$$PS_5(t) = \left[\overline{\mathrm{R}_1} + \overline{\mathrm{R}_y}\right] * (Z_1) \tag{10}$$

$$PS_6(t) = \left[\mathrm{R}_1 + \overline{Z_1}\right] + \left[\overline{\mathrm{R}_1} * Z_1\right] \tag{11}$$

$$PS_7(t) = \left[\overline{\mathrm{R}_1} + \mathrm{R}_y\right] * Z_1 \tag{12}$$

$$PS_8(t) = [\mathrm{R}_1 + Z_1] + \left[\overline{\mathrm{R}_1} * \overline{Z_1}\right] \tag{13}$$

where y = X, + stands for logical OR, and * stands for multiplication. The following expression determines how the bottom inverter's secondary switches operate when they are turned on and off:

Step 1. Form a set:

$$\mathrm{R} = \left[\mathrm{R}_1, \mathrm{R}_2, \mathrm{R}_3, \mathrm{R}_4, \ldots .. \quad \mathrm{R}_{y-3}, \mathrm{R}_{y-2}, \mathrm{R}_{y-1}, \quad \mathrm{R}_y\right] \tag{14}$$

Step 2. Write the permutation P on R :

$$P = \begin{bmatrix} \mathrm{R}_1 & \mathrm{R}_2 & \mathrm{R}_3 & \ldots & \mathrm{R}_{y-2} & \mathrm{R}_{y-1} & \mathrm{R}_y \\ \mathrm{R}_2 & \mathrm{R}_3 & \mathrm{R}_4 & \ldots & \mathrm{R}_{y-1} & \mathrm{R}_y & \mathrm{R}_1 \end{bmatrix} \tag{15}$$

Step 3. Eliminate the final column in the above permutation P_1 and rework as

$$P_1 = \begin{bmatrix} \mathrm{R}_1 & \mathrm{R}_2 & \mathrm{R}_3 & \ldots & \mathrm{R}_{y-3} & \mathrm{R}_{y-2} & \mathrm{R}_{y-1} \\ \mathrm{R}_2 & \mathrm{R}_3 & \mathrm{R}_4 & \ldots & \mathrm{R}_{y-2} & \mathrm{R}_{y-1} & \mathrm{R}_1 \end{bmatrix} \tag{16}$$

Step 4. We can develop the switching signals for the secondary switches calculated from the above equation. The first and last columns of the matrix are responsible for establishing the switching patterns for the initial and final secondary switches, respectively. The equations for SS_1 and SS_n are also included.

$$SS_1(t) = \left((\mathrm{R}_1 \oplus \mathrm{R}_2) * \overline{Z_1}\right) + \left(\left(\mathrm{R}_{y-1} \oplus \mathrm{R}_y\right) * Z_1\right) \tag{17}$$

$$SS_n(t) = \left((\mathrm{R}_1 \oplus \mathrm{R}_2) * Z_1\right) + \left(\left(\mathrm{R}_{y-1} \oplus \mathrm{R}_y\right) * \overline{Z_1}\right) \tag{18}$$

where the XOR (exclusive OR) operation is represented as $\oplus$. In a similar manner, the second column of the permutation matrix P_1 was used to generate the switching patterns for SS_2, while the second column from the end was used for $SS_{(n-1)}$. The expressions were as follows:

$$SS_2(t) = \left((\mathrm{R}_2 \oplus \mathrm{R}_3) * \overline{Z_1}\right) + \left(\left(\mathrm{R}_{y-2} \oplus \mathrm{R}_{y-1}\right) * Z_1\right) \tag{19}$$

$$SS_{n-1}(t) = \left((\mathrm{R}_2 \oplus \mathrm{R}_3) * Z_1\right) + \left(\left(\mathrm{R}_{y-2} \oplus \mathrm{R}_{y-1}\right) * \overline{Z_1}\right) \tag{20}$$

The switching states and expected output of the proposed fifteen-level inverter are represented in Table 3. It shows the top and bottom H-bridge switches in an active and non-active mode. The primary switches PS_1 and PS_3 were turned on and off by comparing the

MR01 reference waveform with the triangular carrier wave, and PS_2 and PS_4 were turned on and off by comparing the MR02 reference waveform with the triangular carrier wave, as shown in Figure 10. The resulting voltage Vyz was obtained from the waveform. The primary switches of the lower inverter from PS_5 to PS_8 were turned on and off concerning Equations (10)–(13), and the secondary switches SS_1 and SS_1 were turned on and off regarding Equations (17)–(19) as represented in the switching signals.

Table 3. Switching states and expected output of 15-level inverter.

Top H Bridge Switches				Bottom H Bridge Switches						Mode	Output Load Voltage $V_{dc1} = V_{dc2} = V_{dc3} = 2V_{dc0}$ *i.e.*, $\left[\frac{V_{dcn}}{V_{dc0}} = 2\right]$		
PS_1	PS_2	PS_3	PS_4	PS_5	PS_6	PS_7	PS_8	SS_1	SS_2		V_{top}	V_{bottom}	$V_{total} = V_{top} + V_{bottom}$
✓	✖	✖	✓	✓	✖	✖	✓	✖	✖	I	$0 \leftrightarrow V_{dc0}$	$6\ V_{dc0}$	$6V_{dc0} \leftrightarrow 7V_{dc0}$
✖	✓	✓	✖	✓	✖	✖	✓	✖	✖	II	$-V_{dc0} \leftrightarrow 0$	$6\ V_{dc0}$	$5V_{dc0} \leftrightarrow 6V_{dc0}$
✓	✖	✖	✓	✖	✖	✖	✓	✓	✖	III	$0 \leftrightarrow -V_{dc0}$	$4V_{dc0} \leftrightarrow 6V_d$	$4V_{dc0} \leftrightarrow 5V_{dc0}$
✖	✓	✓	✖	✖	✖	✖	✓	✓	✖	IV	$V_{dc0} \leftrightarrow 0$	$2V_{dc0} \leftrightarrow 4V_d$	$3V_{dc0} \leftrightarrow 4V_{dc0}$
✓	✖	✖	✓	✖	✖	✖	✓	✖	✓	V	$0 \leftrightarrow V_{dc0}$	$2\ V_{dc0}$	$2V_{dc0} \leftrightarrow 3V_{dc0}$
✖	✓	✓	✖	✖	✖	✖	✓	✖	✓	VI	$-V_{dc0} \leftrightarrow 0$	$2\ V_{dc0}$	$V_{dc0} \leftrightarrow 2V_{dc0}$
✓	✖	✖	✓	✓	✓	✖	✖	✖	✖	VII	$0 \leftrightarrow V_{dc0}$	0	$0 \leftrightarrow V_{dc0}$
✖	✓	✓	✖	✖	✖	✓	✓	✖	✖	VIII	$0 \leftrightarrow -V_{dc0}$	0	$0 \leftrightarrow -V_{dc0}$
✓	✖	✖	✓	✖	✓	✖	✖	✓	✖	IX	$V_{dc0} \leftrightarrow 0$	$-2\ V_{dc0}$	$-V_{dc0} \leftrightarrow -2V_{dc0}$
✖	✓	✓	✖	✖	✓	✖	✖	✓	✖	X	$0 \leftrightarrow -V_{dc0}$	$-2\ V_{dc0}$	$-2V_{dc0} \leftrightarrow -3V_{dc0}$
✓	✖	✖	✓	✖	✓	✖	✖	✖	✓	XI	$-V_{dc0} \leftrightarrow 0$	$-2V_{dc0} \leftrightarrow -$	$-3V_{dc0} \leftrightarrow -4V_{dc0}$
✖	✓	✓	✖	✖	✓	✖	✖	✖	✓	XII	$0 \leftrightarrow V_{dc0}$	$-4V_{dc0} \leftrightarrow -$	$-4V_{dc0} \leftrightarrow -5V_{dc0}$
✓	✖	✖	✓	✖	✓	✓	✖	✖	✖	XIII	$V_{dc0} \leftrightarrow 0$	$-6\ V_{dc0}$	$-5V_{dc0} \leftrightarrow -6V_{dc0}$
✖	✓	✓	✖	✖	✓	✓	✖	✖	✖	XIV	$0 \leftrightarrow -V_{dc0}$	$-6\ V_{dc0}$	$-6V_{dc0} \leftrightarrow -7V_{dc0}$

✖—OFF | ✓—ON

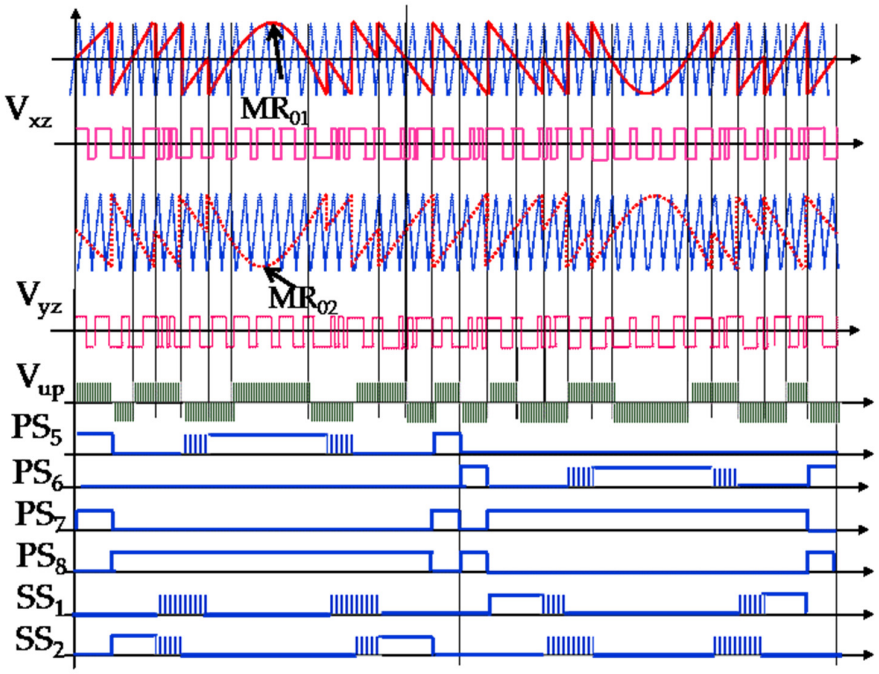

Figure 10. Generated PWM switching signals for switches.

5. Results and Discussion

This section presents the simulation and experimental results of the proposed MLI. The simulation parameters used for the 15 levels are represented in Table 4. The simulation was conducted in MATLAB 2021a Simulink with a resistive load. Simulations were performed for the proposed inverter in MATLAB/Simulink to verify the inverter configuration. The simulations up to 15 levels used the algorithm outlined in Section 4, which could be expanded to every additional level needed. The setting up for both the simulation and the experiment was identical. Figures 11 and 12 illustrate the generated high-frequency PWM pulses for the top inverter primary switches PS1 to PS4. The bottom inverter was run at a low frequency, whereas the top inverter operated at a high switching rate identical to the carrier frequency (10 kHz). Figures 13 and 14 illustrate the generated low-frequency PWM pulses for the bottom inverter primary switches PS5 to PS8. Figure 15 illustrates the low-frequency PWM pulses generated for the bottom inverter secondary switches SS1 and SS2. The upper and lower inverter waveforms for a 15-level inverter and the final waveforms had a modulation index of 1. The output voltage levels fell as the quantity of "m" continued to decrease the resulting output voltage across the load, and the voltage output at the top inverter, the voltage output at the bottom inverter, and the load current waveform are displayed in Figure 16. The previously mentioned results were reached by assuming that each capacitor in the H-bridge inverter had its own independent DC source. Nevertheless, the generalized PWM switching approach and the improved modulation technique were employed to provide the proposed H-bridge inverter with one independent DC source.

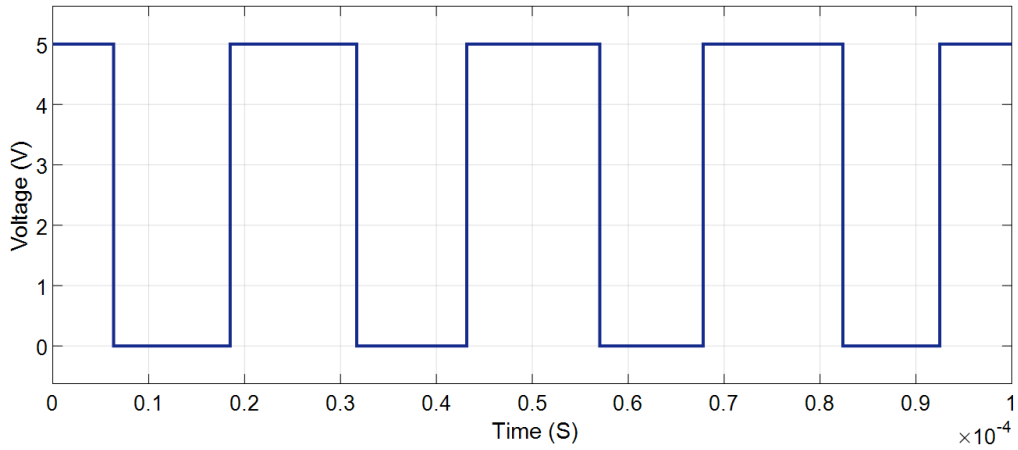

Figure 11. High-frequency top inverter PWM for PS_1 and PS_3.

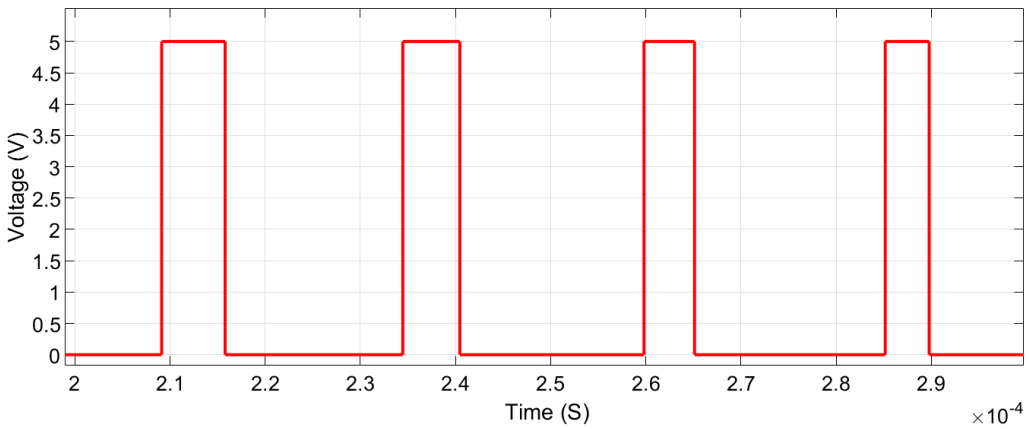

Figure 12. High-frequency top inverter PWM for PS_2 and PS_4.

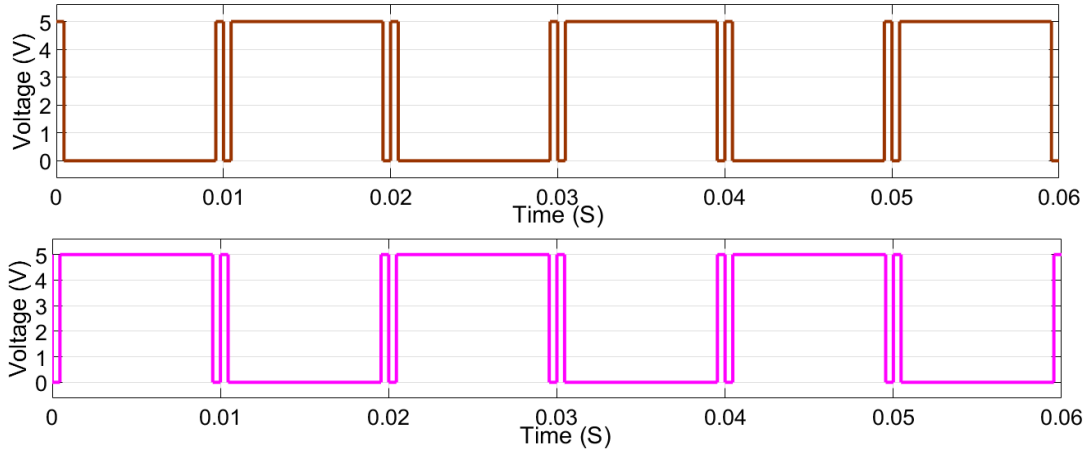

Figure 13. Low-frequency bottom inverter PWM for PS_5 and PS_7.

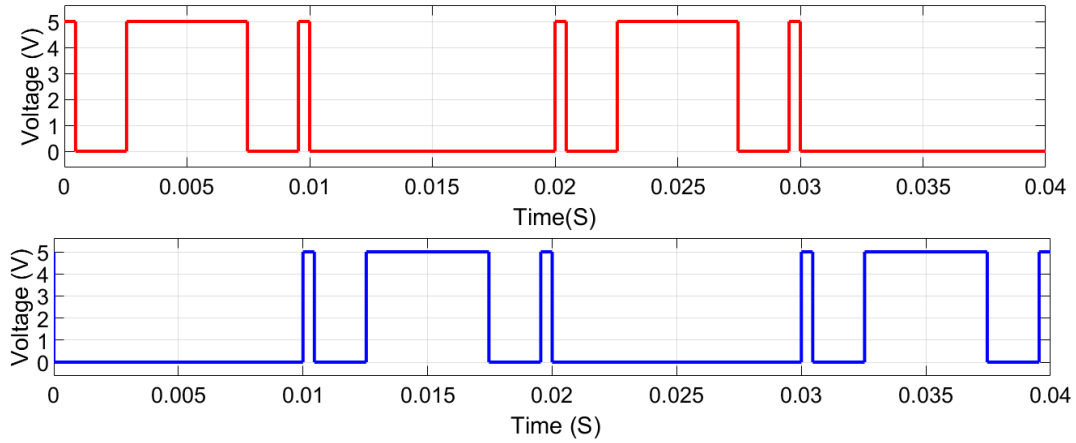

Figure 14. Low-frequency bottom inverter PWM for PS_6 and PS_8.

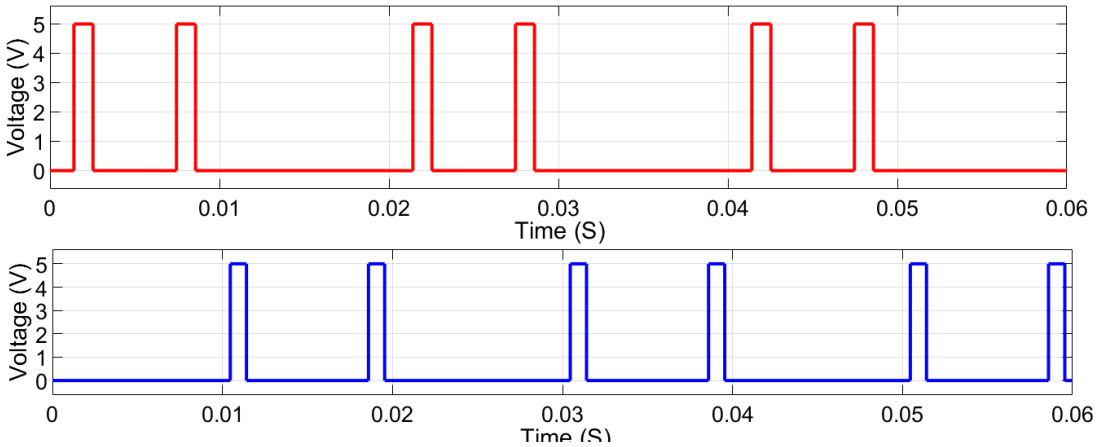

Figure 15. Bottom inverter PWM for SS_1 and SS_2.

Figure 17 shows the output voltages at the capacitors without implementing the CVB approach. When using the generalized PWM method, it can be seen that although the C_1 and C_3's capacitor voltages continually charged, C_2 drained continuously. Figure 18 shows the output voltages at the capacitors with the implementation of the CVB algorithm. It depicts the voltages across the proposed MLI's capacitors. At the same time, it was powered by an integrated conventional and improved switching approach, showing how closely spaced the capacitor voltages were to one another.

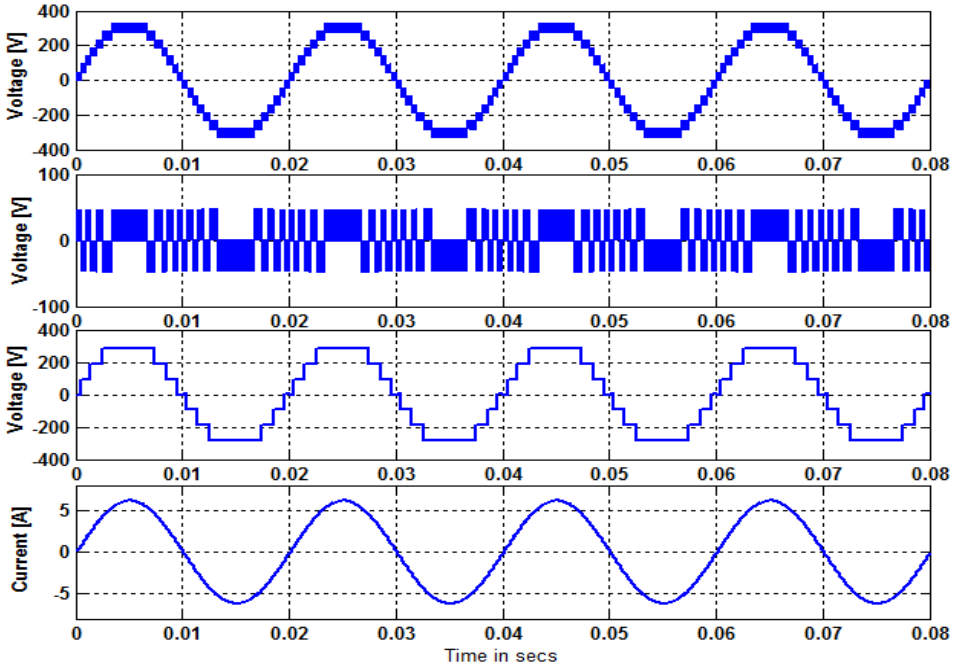

Figure 16. The 15-level inverter: (**a**) Obtained output voltage across the load. (**b**) Obtained voltage at the top inverter. (**c**) Obtained voltage at the bottom inverter. (**d**) Obtained load current waveform.

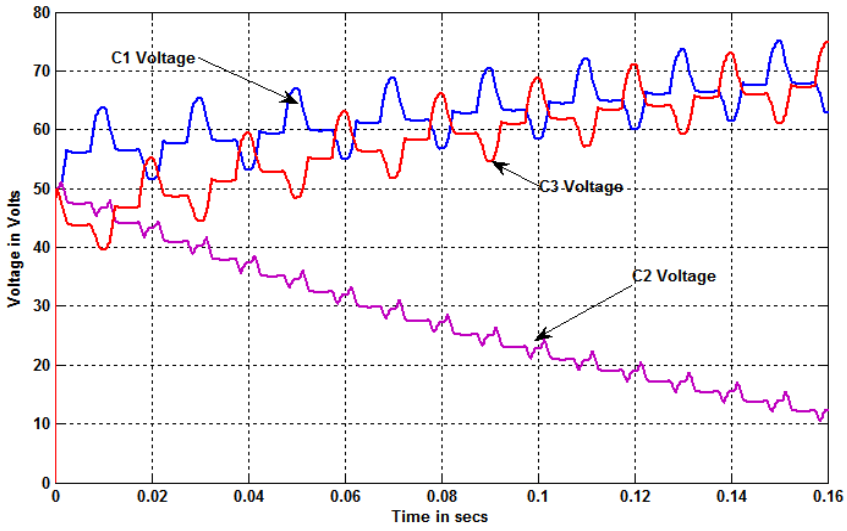

Figure 17. Capacitor voltage at the bottom inverter without balancing.

Table 4. Simulation parameters.

PARAMETERS	LEVEL 11	LEVEL 15
Top inverter voltage	65 V	47 V
Bottom inverter voltage	130 V	94 V
Load resistance = 100 Ω and load inductance = 30 mH.		

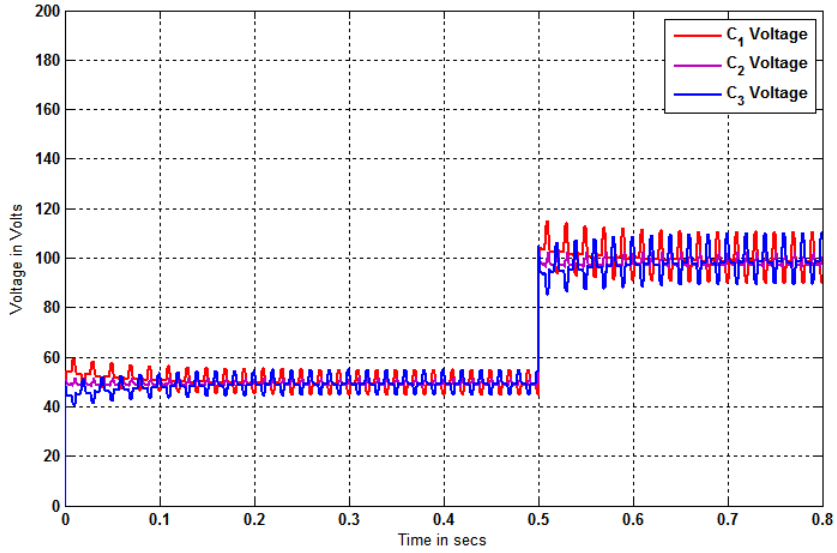

Figure 18. Capacitor voltage at the bottom inverter with balancing.

6. Hardware Validation

The proposed MLI was designed for a power of 2000 W with two asymmetrical DC input voltages of 47 V for the top inverter and 94 V × 3 for the bottom inverter, and the cascaded output voltage was obtained with equal discrete steps. Figure 19 depicts the block diagram of the hardware setup of the proposed converter. Figure 20 displays an image of the hardware configuration for the proposed d inverter with 15 levels constructed in the laboratory. The top and bottom inverters employed IGBTs from the MKI 80-06T6K series. A FIO50-12BD bidirectional secondary switch was employed in the bottom inverter. A SPARTAN 3A FPGA kit was used to create the gate-driving signal.

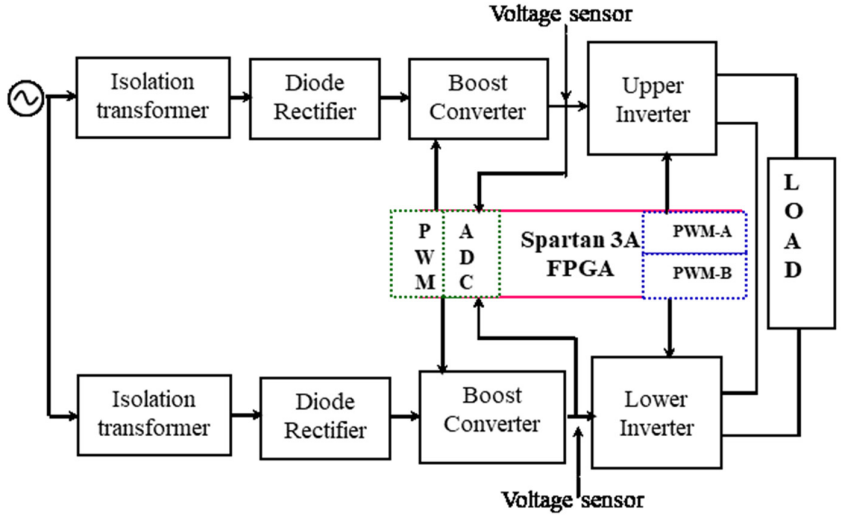

Figure 19. Hardware block setup of the proposed inverter.

Figures 21 and 22 depict the experimental findings of a 15-level inverter for upper inverters (PS1, PS3, PS2, and PS4). The switching pulses were produced for the high frequency of the top inverters while operating using the CVB technique. The switching frequency was maintained as 9.996 KHz for the upper switches (1 Div = 2 V). Figures 23 and 24 depict the experimental results of the PWM waveform for the bottom inverters (PS5, PS7, PS6, and PS8). The switching voltages for the lower inverters were 5 V with (1 Div = 2 V). It showed that it maintained constant voltage while applying the lower switches with the help of CBV. The secondary switches' PWM waveforms are illustrated in Figure 25. It

operated at a low frequency of 101.381 Hz (1 Div = 2 V). It showed that while applying the CVB algorithm, the auxiliary switches operated at a high frequency, and the remaining switches operated at a low frequency. The output voltage of the proposed inverter, while controlled by the CVB methodology, is shown in Figure 26. In addition to the load current waveform, it also displayed the high- and low-frequency inverter waveforms. It was seen that the lower-frequency inverter output momentarily switched to a high frequency [29–31]. Figure 27 shows the hardware results of the capacitance voltages when the load was rapidly raised from 5 KW to 10 KW. It was clear that regardless of the case of an immediate load shift, the capacitor voltage only slightly deviated from its initial value before returning to it.

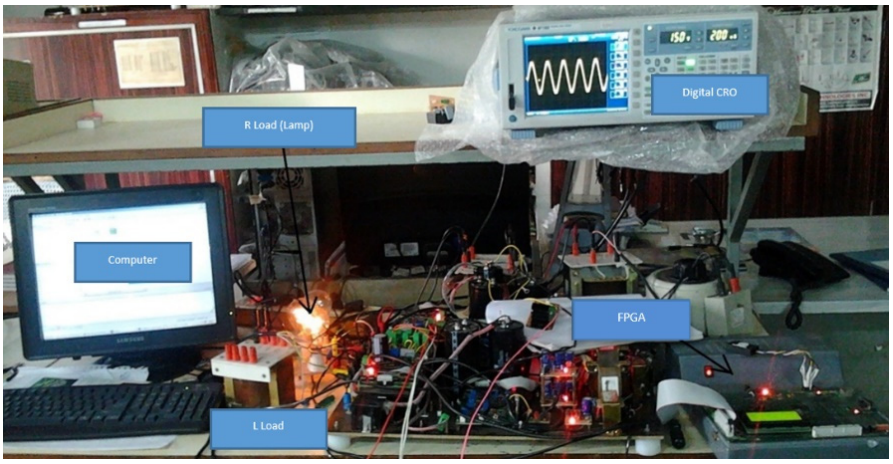

Figure 20. Hardware prototype model of the proposed inverter.

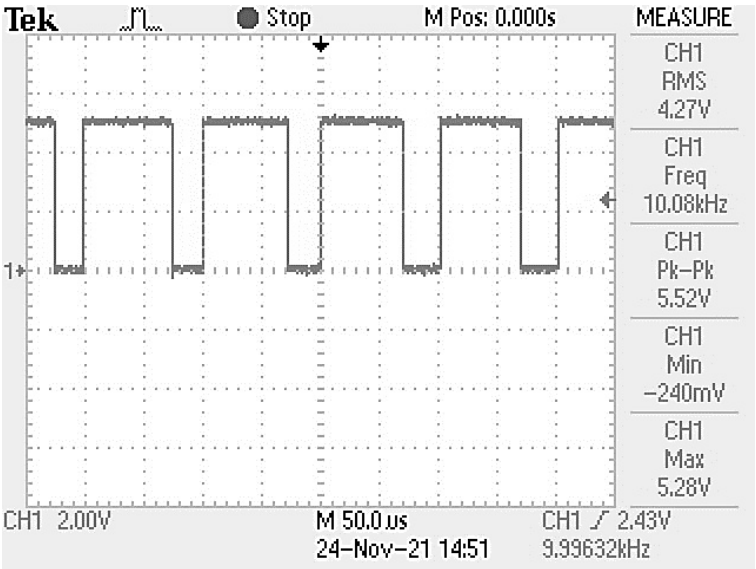

Figure 21. High-frequency top inverter PWM for PS_1 and PS_3.

The FFT analyses of the output voltage for the 11- and 15-level inverters are shown in Figures 28 and 29. The total harmonic distortions (THDs) of 11.36% and 8.02% were obtained for a fundamental frequency of 50 Hz. Without utilizing substantial voltage filters at the output, the load voltage was reached with a symmetrical voltage step equal to 100 V. The load current waveform with its harmonic spectra was reduced for a proposed MLI with a load of 5 kW and 0.8 LPF.

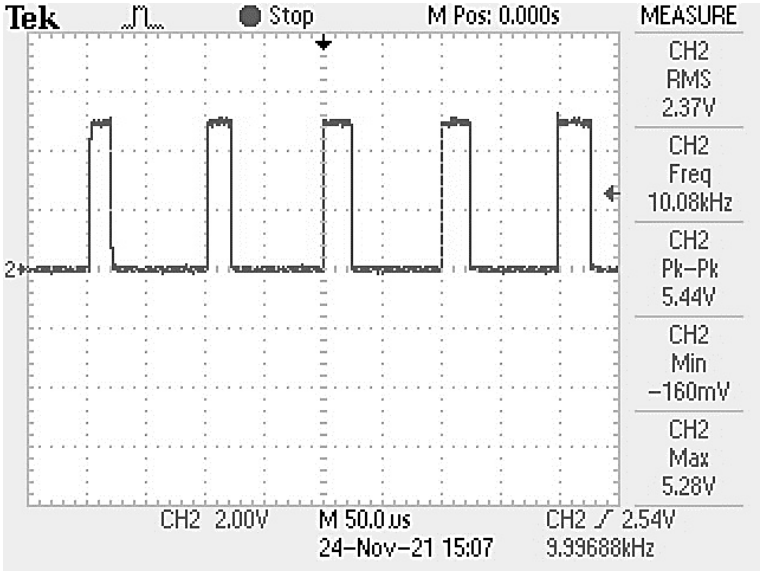

Figure 22. High-frequency top inverter PWM for PS_2 and PS_4.

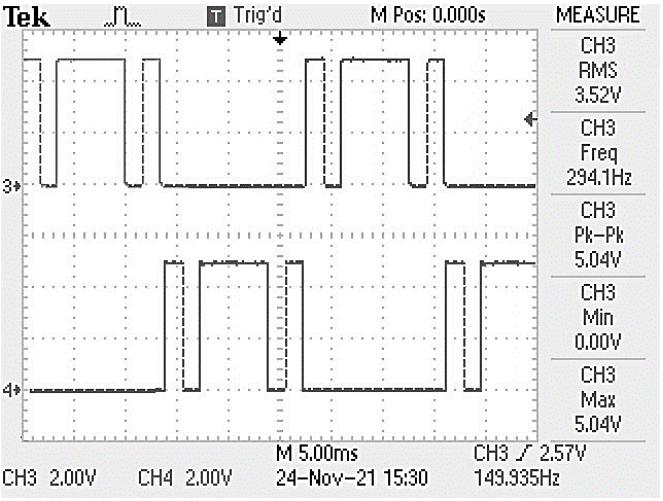

Figure 23. Low-frequency bottom inverter PWM for PS_5 and PS_7.

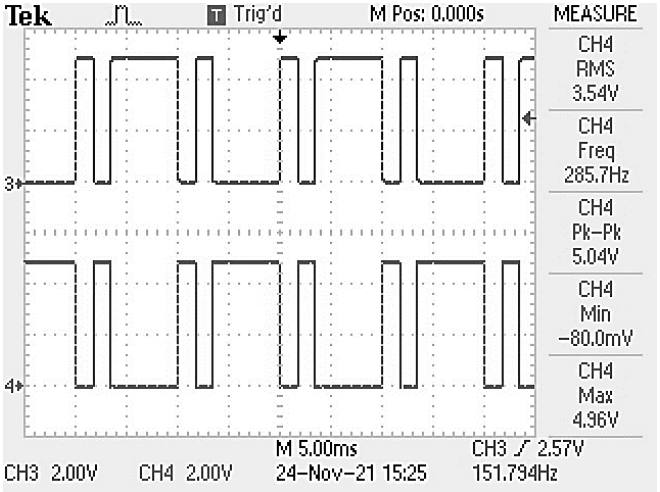

Figure 24. Low-frequency bottom inverter PWM for PS_6 and PS_8.

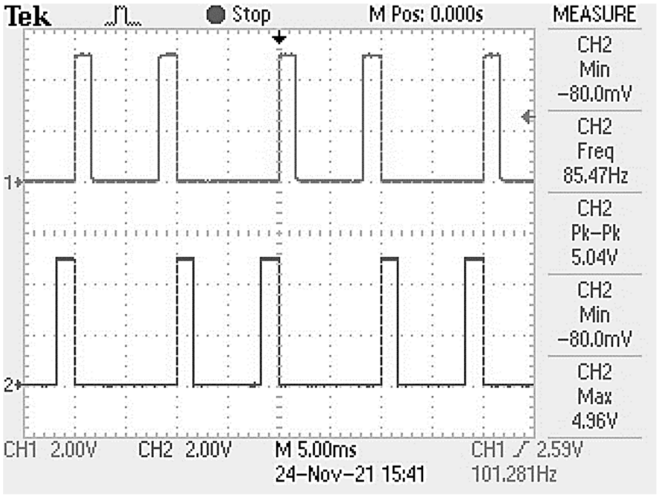

Figure 25. Bottom inverter PWM for SS_1 and SS_2.

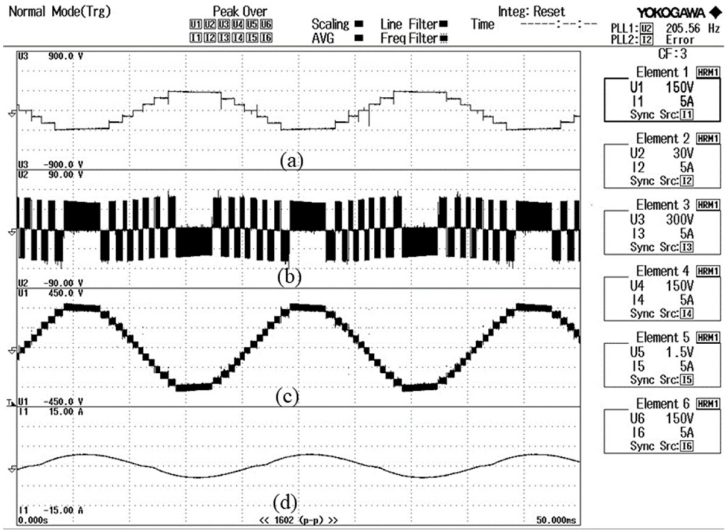

Figure 26. (**a**) Output voltage at the bottom inverter. (**b**) Voltage at the top inverter. (**c**) Output voltage across the load. (**d**) Load current hardware waveform.

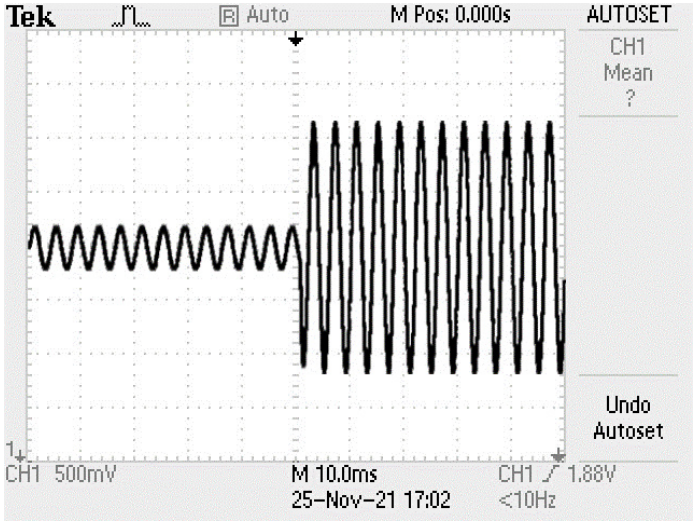

Figure 27. Output current with load variation.

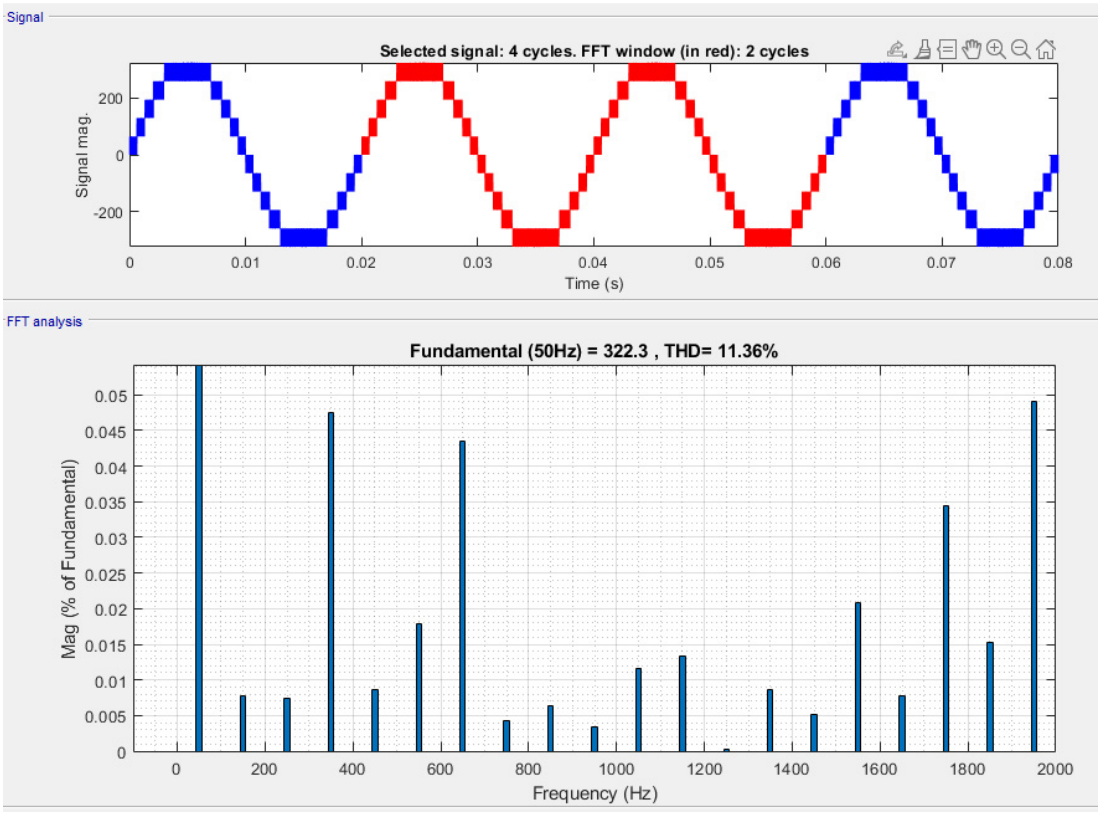

Figure 28. FFT analysis for 11-level inverter.

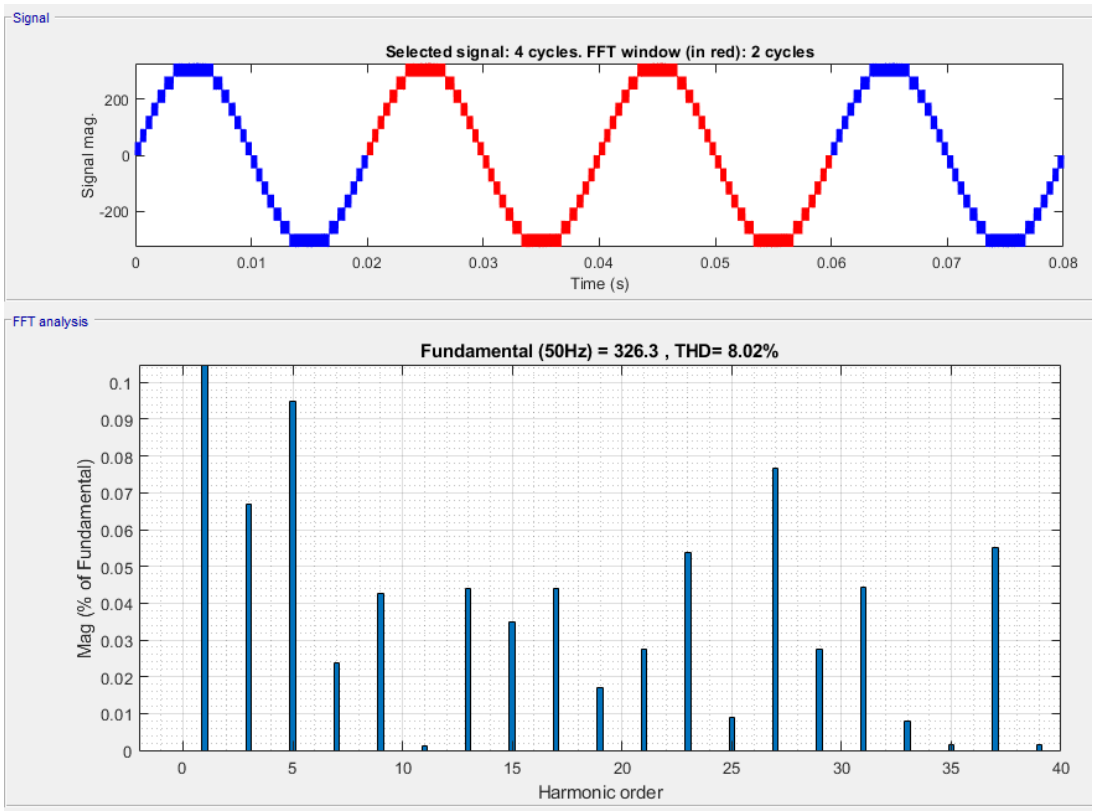

Figure 29. FFT analysis for 15-level inverter.

Table 5 details the current THD and the number of switches required for the 11- and 15-level inverters. The current THD values were 0.88 and 2.41 for 15 and 11 MLI, respectively. Table 6 demonstrates that the proposed topology outperformed the alternative topologies regarding switching devices and THD. In the MLI topologies, as the level increased, the THD reduced, and the decreased THD offered higher performance and power quality.

Table 5. Voltage THD for 11- and 15-level inverters.

Levels	No. of Primary Switches in the Top Inverter	No. of Primary Switches in the Bottom Inverter	No. of Secondary Switches in the Bottom	Current THD in %
15	4	4	2	0.88
11	4	4	1	2.41

Table 6. THD comparison of various 15-level MLIs with the proposed inverter.

Previous Work	Levels	Total No. of Switches Used	Total DC Sources	Current THD in %
[9]	15	10	3	2.32
[10]	15	10	3	1.83
[17]	15	10	3	1.08
Proposed	15	10	2	0.88

7. Conclusions

MLI provides improved output waveforms with a low THD. This study proposed a novel PWM technique for cascaded MLI with the few discrete DC sources and power electronics components possible. The capacitor voltages were also balanced using cutting-edge voltage balancing technology. The 15-level inverter converted a DC input voltage into a sinusoidal waveform with a lower THD of 8.02% compared with an 11-level MLI. The proposed inverter was simulated using MATLAB/Simulink, and experimental results were obtained, which were consistent with the simulation. The gate signals for the simulated inverter were generated using a SPARTAN 3A FPGA board, and these pulses were used to obtain the 15-level output of the inverter. The method balanced the capacitor voltages; hence, the generated inverter did not need extra multi-outlet DC–DC converters. The proposed inverter has various benefits apart from fewer components; it can be smaller and cost less and can have fewer switching losses and higher efficiency. As a result, applications requiring high and medium power can be employed with the proposed inverter. In future, this work can be extended to apply power balancing and machine learning approaches for controlling and diagnosing various faults in MLI.

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