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# Design and Optimization of Germanium-Based Gate-Metal-Core Vertical Nanowire Tunnel FET

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**Abstract:** In this paper, a germanium-based gate-metal-core vertical nanowire tunnel field effect transistor (VNWTFET) has been designed and optimized using the technology computer-aided design (TCAD) simulation. In the proposed structure, by locating the gate-metal as a core of the nanowire, a more extensive band-to-band tunneling (BTBT) area can be achieved compared with the conventional core–shell VNWTFETs. The channel thickness ($T_{ch}$), the gate-metal height ($H_g$), and the channel height ($H_{ch}$) were considered as the design parameters for the optimization of device performances. The designed gate-metal-core VNWTFET exhibits outstanding performance, with an on-state current ($I_{on}$) of 80.9 μA/μm, off-state current ($I_{off}$) of $1.09 \times 10^{-12}$ A/μm, threshold voltage ($V_t$) of 0.21 V, and subthreshold swing (SS) of 42.8 mV/dec. Therefore, the proposed device was demonstrated to be a promising logic device for low-power applications.

**Keywords:** tunnel field-effect transistor (TFET); low power; vertical nanowire; core–shell; germanium; technology computer-aided design (TCAD)

## 1. Introduction

The power consumption of future transistors has become one of the most important problems in the semiconductor industry. As the device dimensions, such as the minimum feature size, are scaled down, the importance of the off-state power as well as the active power becomes significant. Particularly, low standby power and low supply voltage ($V_{DD}$) operation are necessary in various electronics applications, such as mobile devices, wearable devices, and internet-of-things (IoT) systems [1–3]. Considering these aspects, the tunnel field-effect transistor (TFET) is one of the most promising logic devices. TFETs have advantages such as low off-state current ($I_{off}$), low subthreshold swing (SS), and low power consumption compared with the conventional metal-oxide-semiconductor field-effect transistors (MOSFETs). In particular, TFETs can have an SS lower than 60 mV/dec, which cannot be achieved by the conventional MOSFETs at room temperature because of their operation mechanism [4–7]. However, the conventional silicon-based TFETs exhibit several critical problems, in particular, low on-state current ($I_{on}$). Due to the large bandgap ($E_g$) of Si, the amount of electron band-to-band tunneling (BTBT) is insufficient, thus resulting in a small $I_{on}$ [8–11]. Therefore, various studies have been conducted to improve these problems in material or structural approaches. TFETs using small $E_g$ materials, such as Ge, at the source region exhibit an improvement in the amount of source-to-channel BTBT [12]. Furthermore, III–V heterojunction TFETs have been investigated for enhancing the electrical properties [13–15]. In addition to those experiments, many attempts have been performed in structural

approaches to overcome the drawbacks, such as line TFET, U-gate TFET, T-shaped TFET, L-shaped TFET, and vertical nanowire TFET (VNWTFET) [15–24]. However, it is still necessary to study TFETs having superior performances and a small size.

In this work, a Ge-based gate-metal-core VNWTFET has been optimally designed and analyzed using the technology computer-aided design (TCAD) simulations. By using the gate-metal-core structure, the proposed device has a wider BTBT junction and, thus, higher current drivability can be obtained at the same size as that of the conventional VNWTFETs. Direct current (DC) characteristics such as $I_{on}$, $I_{off}$, the on–off current ratio ($I_{on}/I_{off}$), threshold voltage ($V_t$), and SS are investigated to evaluate the device performance. Moreover, several device parameters were modulated to obtain the optimized design values.

## 2. Device Structure and Description

Figure 1 shows the cross-sectional view of the proposed Ge-based gate-metal-core VNWTFET with a gate radius ($R_g$) of 10 nm and a gate dielectric thickness ($T_{ox}$) of 2 nm. The gate dielectric material is hafnium oxide ($HfO_2$), which enhances the current performances because of a higher gate controllability. The lower $E_g$ and lower electron effective mass ($m_e^*$) of Ge can increase the BTBT rate [12]. The work function of the gate metal is 4.27 eV. The doping concentrations of the source, channel, and drain are *p*-type $1 \times 10^{20}$ cm$^{-3}$, *p*-type $1 \times 10^{16}$ cm$^{-3}$, and *n*-type $5 \times 10^{18}$ cm$^{-3}$, respectively. $I_{on}$ is defined as the drain current ($I_{DS}$) at the gate voltage ($V_{GS}$) = the drain voltage ($V_{DS}$) = 0.55 V, for low-power applications. Further, the threshold voltage ($V_t$) is extracted using a constant-current method [25].

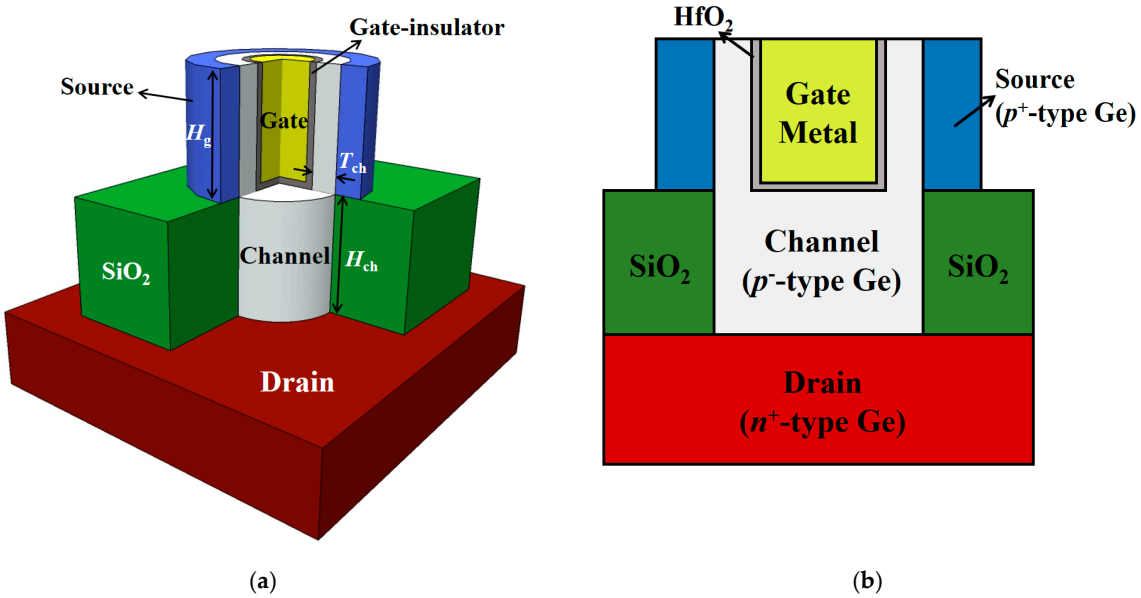



**Figure 1.** (**a**) Schematic view and (**b**) cross-sectional view of the proposed Ge-based gate-metal-core vertical nanowire tunnel field effect transistor (VNWTFET), respectively.

Figure 2 shows the mechanism of the current flow in the proposed device. As indicated in Figure 2a, the electrons are tunneled mainly from the source to the channel regions in the lateral path and the tunneled electrons drift toward the drain region by $V_{DS}$. When the positive $V_{GS}$ is applied, the energy bands in the channel region are lowered and BTBT occurs at the channel–source interfaces as shown in Figure 2b. Therefore, the channel thickness ($T_{ch}$) and the gate-metal height ($H_g$) were considered as design variables for optimization processes because $T_{ch}$ and $H_g$ determine the tunneling probability and current drivability. Furthermore, the proposed gate-metal-core structure has the advantage that it proposes a wider source–channel junction area ($A = 2\pi \times (R_g + T_{ox} + T_{ch}) \times H_g$) than the conventional core–shell structure ($A = 2\pi \times T_{ch} \times H_g$) in the same dimensions. Additionally,

in the case of TFETs, a short source-to-drain distance causes the leakage current at the off-state and the ambipolar behavior when the negative $V_{GS}$ is applied. Thus, the channel height ($H_{ch}$) was also considered as a design parameter. The silicon dioxide ($SiO_2$) is placed between the source and drain regions to suppress the leakage current.

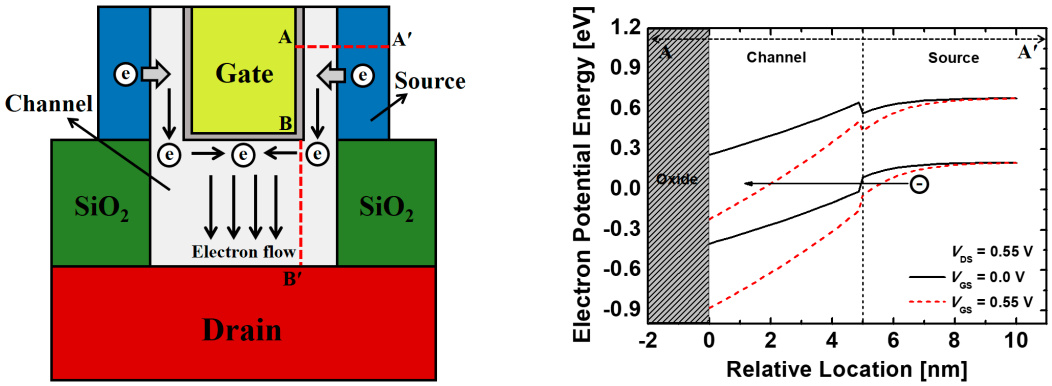



**Figure 2.** (**a**) The electron flow and (**b**) energy band diagrams of the proposed Ge-based gate-metal-core VNWTFETs. Energy band diagrams are extracted across the A–A′ line in Figure 2a.

The device design and analysis are performed with the Sentaurus TCAD simulation. During the simulation process, various physical models were included for the higher accuracy. A nonlocal BTBT model was applied because the drive current of the proposed device is totally affected by the amount of tunneled electrons. The generation rate ($R_{net}$) by the nonlocal BTBT mechanism can be obtained by the follow equation:

$$R_{net} = A\left(\frac{F}{F_0}\right)^P \exp\left(-\frac{B}{F}\right) \tag{1}$$

where $F_0$ = 1 V/cm, $P$ = 2.5 for the phonon-assisted tunneling process. At $T$ = 300 K, the prefactor, $A$, and the exponential factor, $B$, for the phonon-assisted tunneling process can be expressed by the follow equations:

$$A = \frac{g(m_c m_v)^{3/2}\left(1 + 2N_{op}\right)D^2{}_{op}(qF_0)^{5/2}}{2^{21/4}\mathrm{h}^{5/2}m_r^{5/4}\rho\varepsilon_{op}E_g^{7/4}} \tag{2}$$

$$B = \frac{2^{7/2}\pi m_r^{1/2}E_g^{3/2}}{3q\mathrm{h}} \tag{3}$$

where $g$ is a degeneracy factor, h is Plank's constant, and $D_{op}$, $\varepsilon_{op}$, and $N_{op}$ are the deformation potential, energy, and number of optical phonons, respectively. $\rho$ is the mass density. $m_C$ and $m_V$ are the effective mass in the conduction band and the valance band, respectively, with the relationship of $\frac{1}{m_r} = \frac{1}{m_V} + \frac{1}{m_C}$. According to the Equations (1)–(3), the proposed Ge-based TFET can achieve the higher $R_{net}$ due to the low $m_e^*$ and the low $E_g$. The Fermi–Dirac statistical model was applied because the electrons in thermal equilibrium with a semiconductor lattice obey Fermi–Dirac statistics. In addition, the Shockley–Read–Hall (SRH) recombination model, auger recombination model, and trap-assisted-tunneling (TAT) model were involved because the recombination/generation, which influences the leakage current in the device, is greatly affected by the SRH and TAT mechanism. Moreover, the bandgap narrowing model, doping dependent mobility model, and quantum confinement effect were considered to estimate the device performances more accurately [26].

## 3. Results and Discussion

Figure 3a shows the $I_{DS}$–$V_{GS}$ transfer characteristics of the proposed gate-metal-core VNWTFETs that vary with different $T_{ch}$. As $T_{ch}$ gets thinner, $I_{on}$ increases since the effective tunneling barrier width decreases. Figure 3b depicts the energy band diagrams of the proposed devices with different $T_{ch}$. The electric field across the channel region also gets stronger as $T_{ch}$ decreases, resulting in the enhancement of the gate controllability. Thus, the thinner $T_{ch}$, having an energy band with a sharp slope, results in an increase of the electron tunneling rate. Moreover, $I_{off}$ also increases as $T_{ch}$ becomes thinner. When $T_{ch}$ is 6 nm, however, $I_{off}$ decreases because of the increment of the resistance of the channel ($R_{ch}$), and then $I_{off}$ increases again as $T_{ch}$ further decreases. Figure 4 indicates the $I_{on}$ and $SS$ characteristics of the proposed devices with the different $T_{ch}$. As described earlier, it is shown that $I_{on}$ increases as $T_{ch}$ reduces. Unlike $I_{on}$, however, $SS$ improved until $T_{ch}$ becomes 5 nm, having the minimum value of 57.5 mV/dec, and thereafter increases because of the increment of $I_{off}$. On the other hand, the ambipolar behavior was scarcely affected by $T_{ch}$, since $H_{ch}$, which contributes to the leakage current when the negative $V_{GS}$ being applied is constant. Since $SS$ is as crucial as $I_{on}$ in the performance of the logic devices, it is desirable that $T_{ch}$ is adjusted to be 5 nm. Consequently, $I_{on} = 4.46 \times 10^{-5}$ A/μm, $I_{off} = 1.35 \times 10^{-11}$ A/μm, $V_t = 0.24$ V, $I_{on}/I_{off} = 3.3 \times 10^6$, and $SS = 57.5$ mV/dec are obtained at $T_{ch} = 5$ nm.

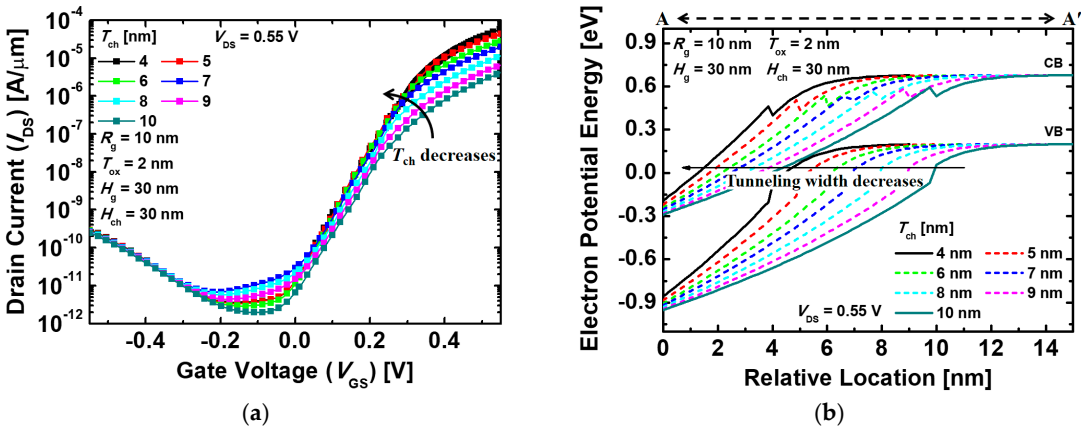



**Figure 3.** (**a**) $I_{DS}$–$V_{GS}$ (drain current–gate voltage) transfer characteristics and (**b**) energy band diagrams of the proposed devices with different channel thicknesses ($T_{ch}$). The energy band diagrams are extracted across the A–A′ line in Figure 2a.

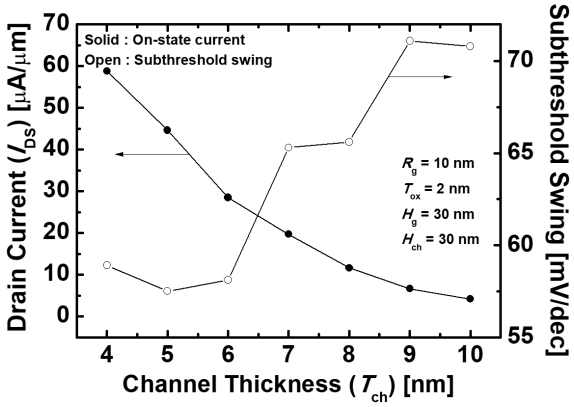
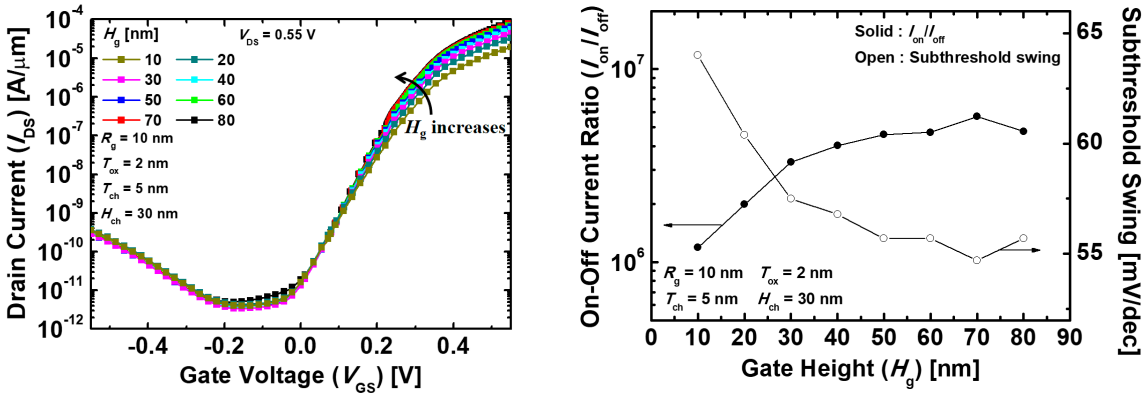



**Figure 4.** $I_{on}$ and subthreshold swing (SS) characteristics of the proposed Ge-based gate-metal-core VNWTFETs with different $T_{ch}$.

Figure 5a shows the $I_{DS}$–$V_{GS}$ transfer characteristics of the proposed devices according to variation in $H_g$. Each curve was extracted from the devices with the different $H_g$ varying from 10 to 80 nm at

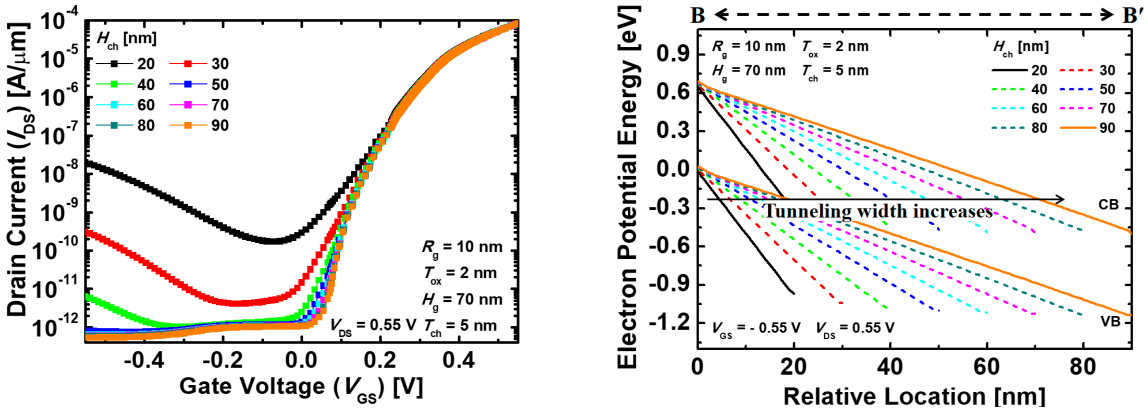
$T_{ch}$ = 5 nm. The higher $H_g$ widens the tunneling area, resulting in the enhancement of $I_{on}$ because the $I_{DS}$ of TFETs is totally affected by the amount of the tunneled electrons. Meanwhile, $I_{off}$ also tends to increase slightly with the higher $H_g$ for the same reason mentioned above. However, when $H_g$ = 30 nm and $H_g$ = 70 nm, $I_{off}$ decreased because the increment of $R_{ch}$, which resulted from the longer current path, dominates over the increase of the amount of the electron tunneling at the off-state. Furthermore, the increase of $R_{ch}$ deteriorates the rate of the $I_{on}$ increment, thus, $I_{on}$ is gradually saturated. For these reasons, $I_{on}/I_{off}$ and SS have the largest value and the lowest value at $H_g$ = 70 nm, respectively, as indicated in Figure 5b. Therefore, optimized values were obtained with $I_{on} = 8.22 \times 10^{-5}$ A/μm, $I_{off} = 1.45 \times 10^{-11}$ A/μm, $V_t$ = 0.21 V, $I_{on}/I_{off} = 5.67 \times 10^6$, and SS = 54.7 mV/dec at $T_{ch}$ = 5 nm and $H_g$ = 70 nm.




(**a**) (**b**)

**Figure 5.** (**a**) $I_{DS}$–$V_{GS}$ transfer characteristics and (**b**) $I_{on}/I_{off}$ (on-state current/off-state current) and SS of the proposed Ge-based gate-metal-core VNWTFETs with different gate-metal heights ($H_g$).

Figure 6a shows the $I_{DS}$–$V_{GS}$ transfer characteristics of the proposed devices that vary with $H_{ch}$. In the proposed device, the ambipolar behavior, when the negative $V_{GS}$ is applied, is mainly affected by the amount of the electron tunneling from the source and channel region to the drain region. Figure 6b depicts the energy band diagrams of the proposed devices that vary with $H_{ch}$ at $V_{GS}$ = −0.55 V and $V_{DS}$ = 0.55 V. With the lower $H_{ch}$, the energy band of the channel is lowered by $V_{DS}$, as in the conventional short channel TFETs [27]. Therefore, the longer $H_{ch}$ where $V_{DS}$ has less effect on the channel has the thicker tunneling barrier width at the channel–drain junction and, thus, suppresses the electron tunneling from the channel to the drain. In addition to the foregoing, as $H_{ch}$ increases, $R_{ch}$ increases because the current path also becomes longer. As a result, $I_{off}$ decreases gradually with the $H_{ch}$ increasing. The increase in $R_{ch}$ also deteriorates $I_{on}$ for the same reason. Figure 7 indicates $I_{on}/I_{off}$ and SS characteristics of the proposed devices with the different $H_{ch}$ varying from 20 to 90 nm. $I_{on}/I_{off}$ is gradually improved as $H_{ch}$ increases, and is then almost saturated when $H_{ch}$ = 80 nm. Moreover, SS has minimum values at $H_{ch}$ = 80 nm and then increases at $H_{ch}$ = 90 nm. As mentioned above, because of the effect of $R_{ch}$, $I_{on}$ and $I_{off}$ decrease constantly with increasing $H_{ch}$, and the decrease in $I_{on}$ dominates over $I_{off}$ when $H_{ch}$ = 80 nm. Finally, the optimized device is achieved with $I_{on} = 8.09 \times 10^{-5}$ A/μm, $I_{off} = 1.09 \times 10^{-12}$ A/μm, $V_t$ = 0.21 V, $I_{on}/I_{off} = 7.45 \times 10^7$, and SS = 42.8 mV/dec at $T_{ch}$ = 5 nm, $H_g$ = 70 nm, and $H_{ch}$ = 80 nm.




(**a**) (**b**)

**Figure 6.** (**a**) $I_{DS}$–$V_{GS}$ transfer characteristics and (**b**) energy band diagrams of the proposed Ge-based gate-metal-core VNWTFETs with different channel heights ($H_{ch}$). The energy band diagrams are extracted across the B–B′ line in Figure 2a at $V_{GS}$ = −0.55 V and $V_{DS}$ = 0.55 V (drain voltage).

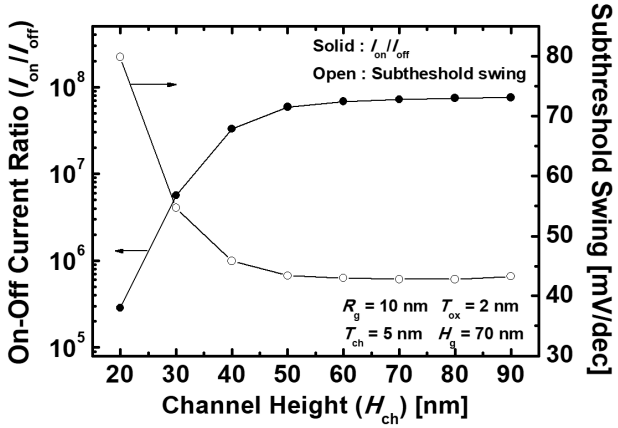



**Figure 7.** $I_{on}$ and SS characteristics of the proposed Ge-based gate-metal-core VNWTFETs with different $H_{ch}$.

Figure 8 indicates the output characteristics of the proposed devices with different $V_{GS}$. When a small $V_{GS}$ of 0.3 V or less is applied, $I_{DS}$ is almost constant and has a low value. $I_{DS}$ has a low value even though $V_{DS}$ increases because the amount of the electrons tunneled from the source to the channel region is small for a low $V_{GS}$. When $V_{GS}$ is greater than 0.4 V, the tunneled electrons in the channel region drift toward the drain region by the positive $V_{DS}$. $I_{DS}$ increases as a function of $V_{DS}$ for small $V_{DS}$, then gets saturated and becomes less dependent on $V_{DS}$ when $V_{DS}$ is approximately 0.5 V, showing the proper output characteristics for circuit applications.

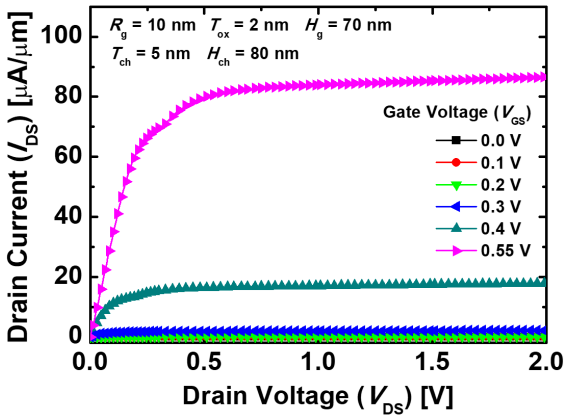



**Figure 8.** Output characteristics of the proposed Ge-based gate-metal-core VNWTFETs with different $V_{GS}$.

The comparison of the proposed device with the different works in terms of $I_{on}$, $V_t$, $V_{DD}$, and SS is presented in Table 1. This proposed device has the highest $I_{on}$ value with the low $V_t$ and the low $V_{DD}$ value. Thus, the proposed Ge-based gate-metal-core VNWTFET is a suitable candidate for the logic devices with the low power consumption.

**Table 1.** Comparison with the different works.

| Parameter | This Work | SiGe-S-NW-TFET [28] | Si-Based Nanotube TFET [29] | Si/SiGe HTG-TFET [30] | Ge-Source vTFET [31] |
|---|---|---|---|---|---|
| $I_{on}$ (μA/μm) | 80.9 (at $V_{GS}$ = 0.55 V) | 11.66 (at $V_{GS}$ = 1.0 V) | 5.0 (at $V_{GS}$ = 1.5 V) | 7.02 (at $V_{GS}$ = 0.5 V) | 27.6 (at $V_{GS}$ = 0.5 V) |
| $V_t$ (V) | 0.21 | 0.37 | 0.9 | 0.28 | 0.20 |
| $V_{DD}$ (V) | 0.55 | 0.8 | 1.2 | 0.5 | 0.5 |
| SS (mV/dec) | 42.8 | 23.75 | 58.3 | 44.64 | 21.2 |

## 4. Conclusions

In this work, a Ge-based gate-metal-core VNWTFET was optimally designed and analyzed based on TCAD simulations. With wider BTBT junctions, a higher current drivability can be realized compared to the conventional TFETs. The proposed device demonstrated superior DC performances with $I_{on} = 8.09 \times 10^{-5}$ A/μm, $I_{off} = 1.09 \times 10^{-12}$ A/μm, $V_t = 0.21$ V, $I_{on}/I_{off} = 7.45 \times 10^7$, and SS = 42.8 mV/dec at $H_g = 70$ nm, $T_{ch} = 5$ nm, and $H_{ch} = 80$ nm. It is ensured that the proposed device would be a promising logic device for the low-power applications.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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