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Investigation on Ambipolar Current Suppression Using a Stacked Gate in an L-shaped Tunnel Field-Effect Transistor

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Abstract: L-shaped tunnel field-effect transistor (TFET) provides higher on-current than a conventional TFET through band-to-band tunneling in the vertical direction of the channel. However, L-shaped TFET is disadvantageous for low-power applications because of increased off-current due to the large ambipolar current. In this paper, a stacked gate L-shaped TFET is proposed for suppression of ambipolar current. Stacked gates can be easily implemented using the structural features of L-shaped TFET, and on- and off-current can be controlled separately by using different gates located near the source and the drain, respectively. As a result, the suppression of ambipolarity is observed with respect to work function difference between two gates by simulation of the band-to-band tunneling generation. Furthermore, the proposed device suppresses ambipolar current better than existing ambipolar current suppression methods. In particular, low drain resistance is achieved as there is no need to reduce drain doping, which leads to a 7% enhanced on-current. Finally, we present the fabrication method for a stacked gate L-shaped TFET.

Keywords: L-shaped tunnel field-effect transistor; stacked gate; dual work function; ambipolar current

1. Introduction

A tunnel field-effect transistor (TFET) has attracted attention as a candidate for low-power applications because of its low subthreshold swing and low off-current compared with the metal-oxide-semiconductor field-effect transistor (MOSFET) [1–5]. Since a working principle of TFET relies on band-to-band tunneling (BTBT), TFET can achieve under 60 mV/decade subthreshold swing which acts as a limit on MOSFET [5–7]. However, TFET has a limitation in its on-current, which is lower than that of the conventional MOSFET because of low BTBT rates [8]. To solve this problem, an L-shaped TFET using vertical BTBT has been proposed [9]. Nevertheless, it has a disadvantage of ensuing large ambipolar current due to the tunneling layer deposited on the gate-drain overlap region during the selective epitaxial-layer growth (SEG) process [10]. Since ambipolar current contributes to the increase of the off-current, finding a method to reduce it is an important issue. Reduced drain doping and gate-drain underlap have been suggested as strategies for eliminating ambipolar current [11–14]. However, the method reducing drain doping concentration has drawbacks in terms of decreased on-current because of the increased drain resistance and in terms of increased Miller capacitance due

to increased gate-drain coupling, which leads to the degradation of resistor–capacitor (RC) switching characteristics [12]. The gate-drain underlap also has a drawback which limits the scalability.

Therefore, in this paper, we propose a method of suppressing ambipolar current by simply stacking the gates utilizing the structural features of L-shaped TFET. First, the structure of the proposed device and simulation method are described. Next, the electrical characteristics of the device are analyzed, which is followed by comparisons to other methods of suppressing ambipolar current. Finally, the fabrication method is presented for the stacked gate L-shaped TFET.

2. Device Structures and Simulation Methods

Figure 1a–d show the schematic designs of the single gate, stacked gate L-shaped TFET and the other devices with gate-drain underlap applied to each of the two devices. All devices are based on silicon and share the same doping concentration except low drain doping device (1×10^{19} cm^{-3} on drain). Abrupt doping profile can be formed because of in-situ doping during epitaxy, especially at the source [15]. Work function of the top gate (ϕ_{G2}) is fixed at 4.5 eV and its height (H_{G2}) is 88 nm. The bottom gate work function (ϕ_{G1}) varies from 4.0 to 4.5 eV and its height (H_{G1}) is 10 nm. The source height is adjusted to 65 nm, which allows the SEG tunneling layer between the source and the gate to be controlled by the top gate while the bottom channel is controlled by the bottom gate. The vertical tunneling thickness (L_t) is 4 nm and the underlap length (L_{un}) is 9 nm. All design parameters are summarized in Table 1. In order to verify the suppression of ambipolar current due to the stacked gates structure, electrical characteristics of each device are investigated through Synopsys Sentaurus™ Technology Computer-Aided Design (TCAD) two-dimensional (2D) device simulation. The nonlocal BTBT model is applied for investigation of ambipolar current in L-shaped TFET since this model takes tunneling effect into consideration based on energy band profile. Two tunneling model coefficients $A_{Si} = 4.0 \times 10^{14}$ cm^{-1}s^{-1}, $B_{Si} = 9.9 \times 10^{6}$ V/cm, $A_{SiGe} = 3.1 \times 10^{16}$ cm^{-1}s^{-1} and $B_{SiGe} = 7.1 \times 10^{5}$ V/cm from [16] are used in this work.

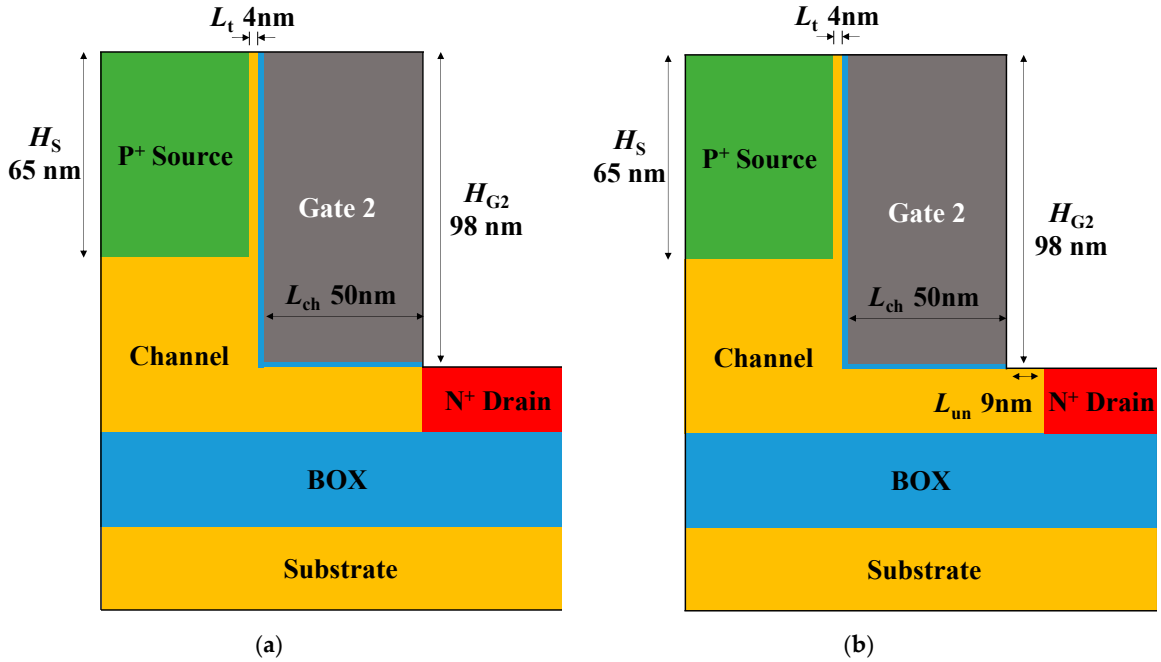


Figure 1. *Cont.*

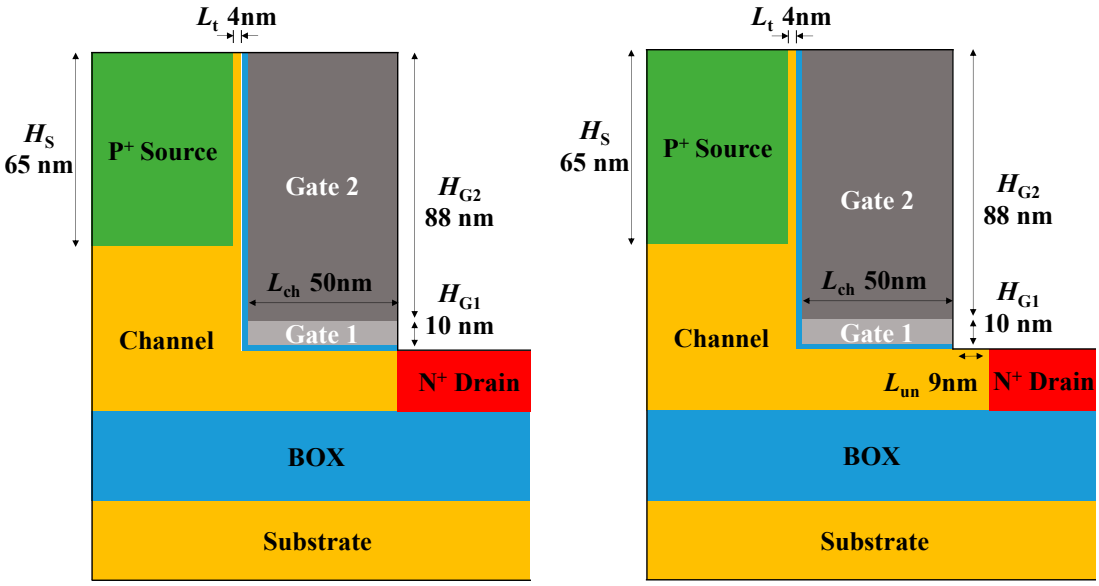


Figure 1. Schematic designs of (**a**) (conventional) single gate L-shaped tunnel field-effect transistor (TFET), (**b**) single gate L-shaped TFET with underlap, (**c**) stacked gate L-shaped TFET and (**d**) stacked gate L-shaped TFET with underlap. In order to compare the suppression of the ambipolar current for each method, the simulations were conducted according to the schematics above.

Table 1. Simulation parameters used for this work.

Parameters	Definitions	Value
N_S	Source doping concentration	Boron, 1×10^{20} cm^{-3}
N_B	Channel doping concentration	Boron, 1×10^{16} cm^{-3}
N_D	Drain doping concentration	Arsenic, 1×10^{19} cm^{-3}, 1×10^{20} cm^{-3}
H_S	Source height	65 nm
H_{G1}	Gate1 height	88 nm
H_{G2}	Gate2 height	10 nm
L_t	Vertical tunneling thickness	4 nm
L_{ch}	Lateral channel length	50 nm
L_{un}	Gate-drain underlap length	9 nm
T_B	Body thickness	20 nm
T_{OX}	Gate oxide thickness	2 nm
V_{DS}	Drain voltage	0.7 V
ϕ_{G1}	Gate1 work function	4.0–4.5 eV
ϕ_{G2}	Gate2 work function	4.5 eV

3. Results

3.1. Ambipolar Suppression of Stacked Gate L-Shaped TFET

As shown in Figure 2a, the ambipolar current is significantly decreased in stacked gate L-shaped TFET because ϕ_{G1} is lower than ϕ_{G2}, which leads to larger channel potential at the drain side. Meanwhile, on-current remains constant because ϕ_{G2} is the same as that of the single gate L-shaped TFET so that the same amount of electrostatic potential is applied to the SEG tunneling layer. Consequently, the on-state region remains unchanged while the off-state region expands [(ii) to (iv)] and the ambipolar state region contracts [(i) to (iii)]. The on-state region, off-state region and ambipolar state region are defined with the constant current method. Figure 2b shows that the tunneling barrier width between the channel and the drain becomes thicker in the stacked gate L-shaped TFET due to

the stronger potential applied to the channel. As a result, the BTBT rate of stacked gate L-shaped TFET significantly decreases in the ambipolar state (Figure 3). In addition, considering the relationship of the potential applied to the channel according to the work function of the gate, the ambipolar state region in the transfer curve will be shifted to the left by decreasing ϕ_{G1}, which will be covered in a later subsection.

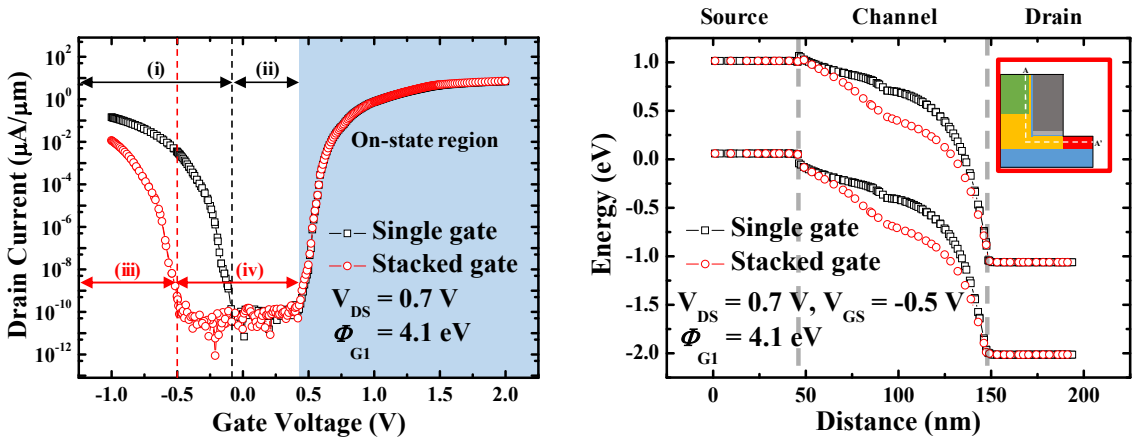


Figure 2. (**a**) Transfer curves of single gate L-shaped TFET and stacked gate L-shaped TFET with 0.7 V-drain voltage (V_{DS}). Off-state and ambipolar state region of each device is distinguished by (i)–(iv). Ambipolar state region of the single gate (i), the off-state region of the single gate (ii), ambipolar state region of the stacked gate (iii) and the off-state region of the stacked gate (iv). It is shown that the ambipolar current is suppressed and the ambipolar state region contracts in the stacked gate L-shaped TFET; (**b**) Energy band diagram at gate voltage (V_{GS}) = −0.5 V for single gate L-shaped TFET and stacked gate L-shaped TFET. They are obtained from source-to-drain along the cutline which is indicated in the inset (A-A′). It is presented that the tunneling barrier between channel-to-drain becomes thicker in the stacked gate L-shaped TFET.

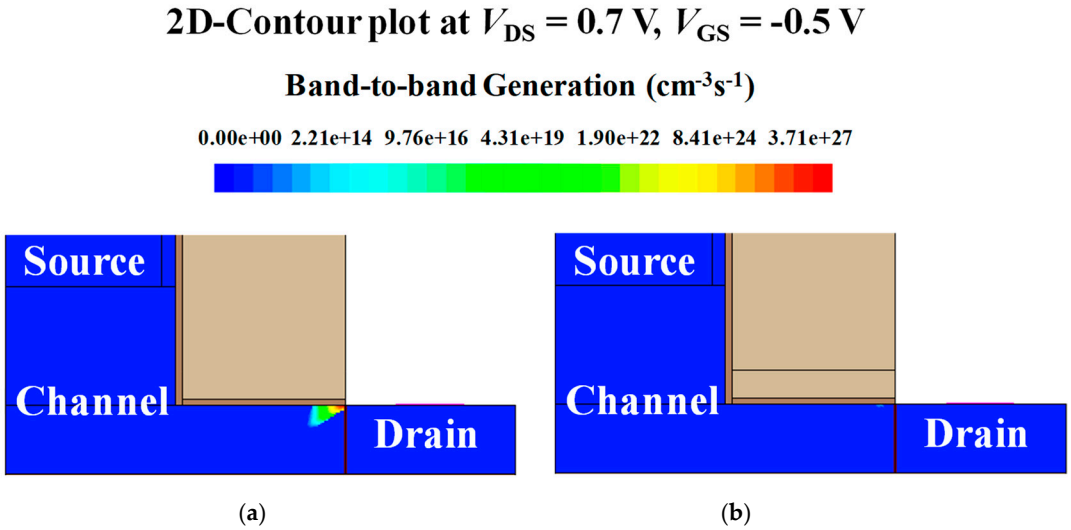


Figure 3. 2-D contour plot of band-to-band tunneling (BTBT) generation for (**a**) single gate and (**b**) stacked gate L-shaped TFET. Ambipolar current suppression is observed from the decreased BTBT rates in the stacked gate L-shaped TFET.

As illustrated in Figure 4, the ambipolar current of stacked gate L-shaped TFET with underlap is the most suppressed. Non-stacked devices have similar off-state region sizes, while stacked devices have an expanded off-state region and reduced ambipolar state region. Comparing with the single

gate L-shaped TFET (without underlap), the stacked gate L-shaped TFET (without underlap) shows ambipolar current (drain current at V_{GS} = −1 V) and ambipolar region to be reduced and contracted by 12 times and by 0.5 V, respectively. This advantage further reduces off-current and makes it less sensitive to process variations.

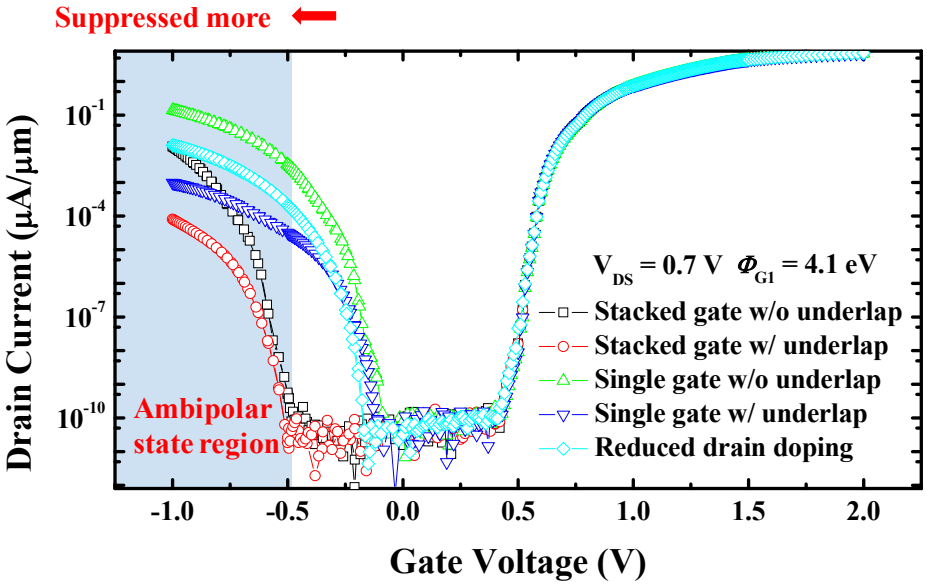


Figure 4. Transfer characteristics for stacked gate L-shaped TFET, stacked gate L-shaped TFET with underlap, low drain doping L-shaped TFET, (conventional) single gate L-shaped TFET, and single gate L-shaped TFET with underlap at V_{DS} = 0.7 V. It is illustrated that the ambipolar state region significantly contracts in the stacked gate L-shaped TFET.

3.2. Gate1 Work Function (ϕ_{G1}) Split

Figure 5 shows the transfer curves of stacked gate L-shaped TFET with various ϕ_{G1}. As the ϕ_{G1} decreases, the ambipolar state region contracts and the off-state region expands because the energy band of the channel drops downward (Figure 6). It leads to thickening of the tunneling barrier width between channel and drain, reducing BTBT rates, as shown in Figure 7.

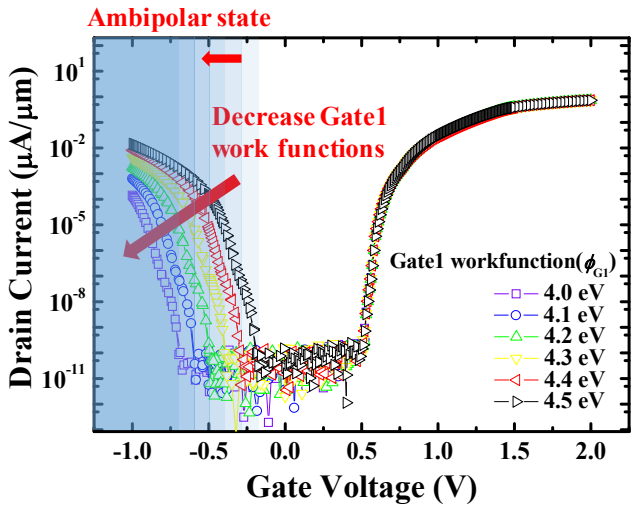


Figure 5. Transfer curves of stacked gate L-shaped TFET with various ϕ_{G1} (at V_{DS} = 0.7 V). As ϕ_{G1} decreases, ambipolar current is suppressed more and also ambipolar state region contracts. It can be interpreted as if only the left part of the transfer curve (V_{GS} < 0) is shifted to the left.

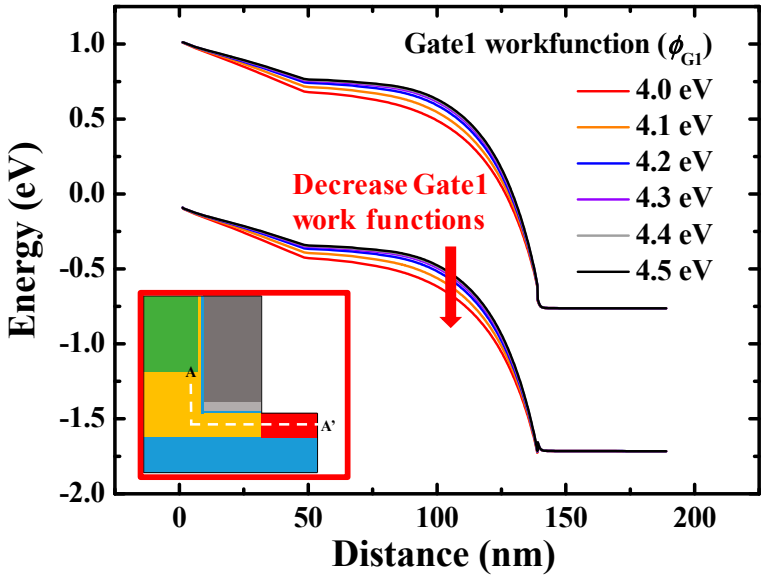


Figure 6. Energy band diagrams with various ϕ_{G1} (at V_{DS} = 0.7 V). They are obtained from channel-to-drain along the cutline which is indicated in the inset (A-A'). As ϕ_{G1} decreases, the tunneling barrier between the channel and the drain becomes thicker.

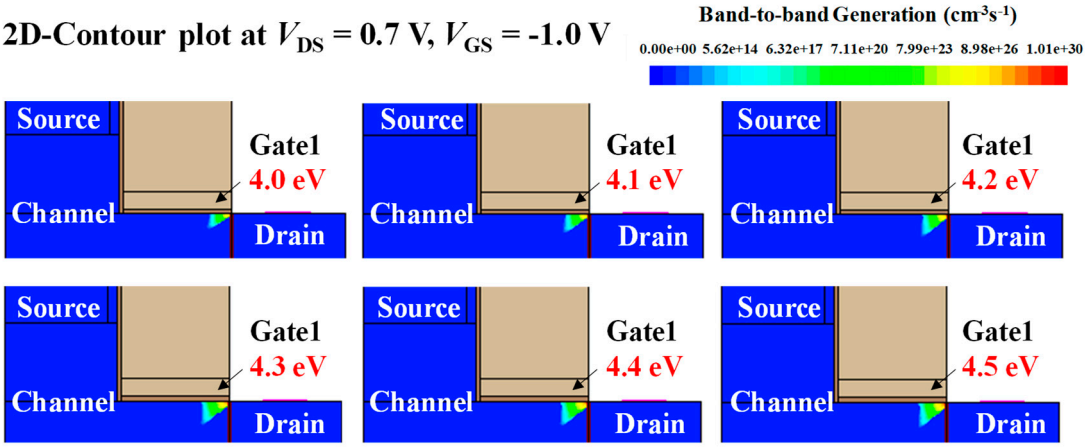
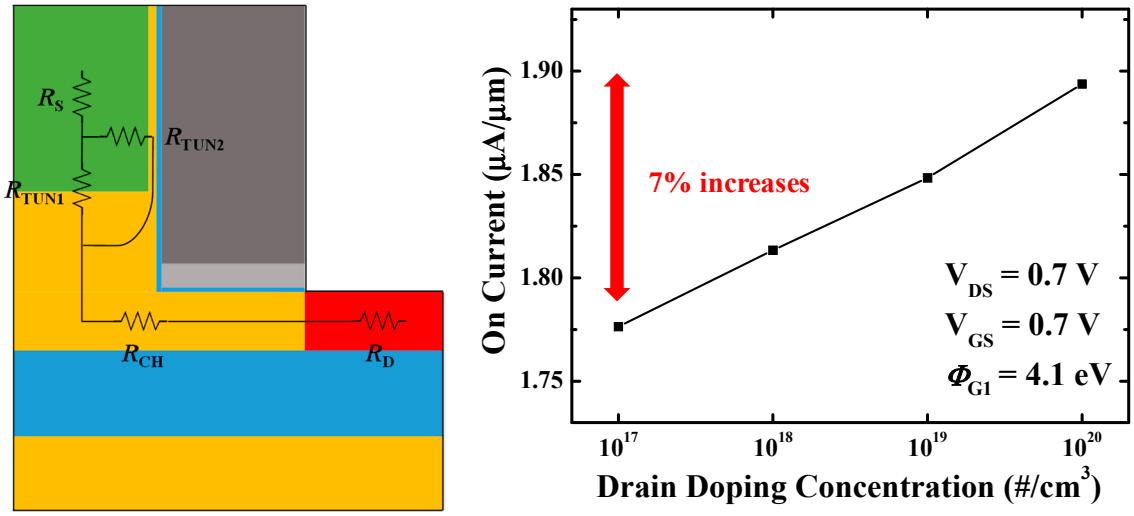


Figure 7. 2-D contour plot of BTBT generation for various ϕ_{G1}. As ϕ_{G1} decreases, BTBT rate decreases.

3.3. Resistance/on-Current

Increase in on-current is beneficial in terms of RC characteristic due to a reduction in the resistance. Figure 8a displays the resistance network in stacked gate L-shaped TFET when the device is in the on-state. Considering that the BTBT generation that contributes to the on-current occurs in two places near the source, the resistance network can be described as above. Since there is no need to lower the drain doping to suppress the ambipolar current, the drain resistance does not increase and it leads to higher on-current than the conventional method. Moreover, increasing the BTBT rate, for example by changing the source from Si to SiGe, reduces the tunneling resistance (R_{TUN1}, R_{TUN2}) and makes the effect of drain resistance more critical. Figure 8b exhibits the on-current with the drain doping concentration in stacked gate L-shaped TFET using SiGe on the source. As a result, up to 7% of an on-current gain can be achieved with an L-shaped TFET.

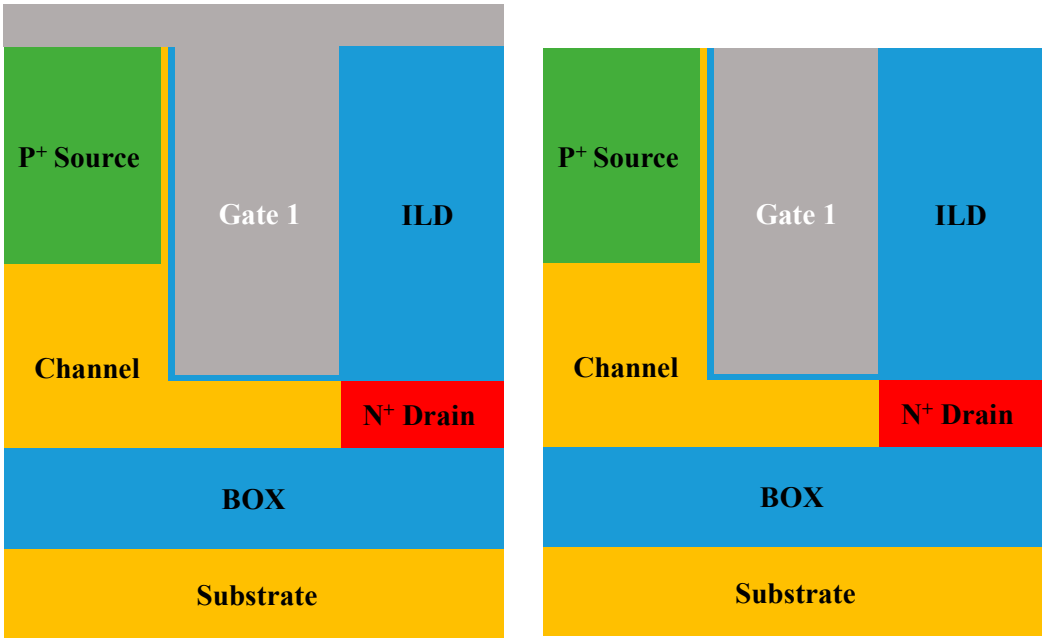


(**a**) (**b**)

Figure 8. (**a**) Resistance network when the device is in the on-state. R_{TUN1} and R_{TUN2} are the tunneling resistances; (**b**) on-current with the drain doping concentration. After changed the source material to SiGe, 7% on-current increases with the drain doping concentration.

3.4. Process Flow

The stacked gate L-shaped TFET can be easily fabricated by the repetition of deposition and etch-back processes, unlike the planar structure in which the lithography process is necessary to form the stacked gate. Figure 9 illustrates the key process steps for stacked gate L-shaped TFET. The other processes before the stacked gate are described in [15]. After the gate dielectric deposition, Gate 2 atomic layer deposition (ALD) process (Figure 9a) is followed by chemical mechanical polishing (CMP) (Figure 9b). Then the etch-back process is done to recess Gate2 under the source (Figure 9c). Finally, Gate1 is repeatedly deposited and CMP is done (Figure 9d). The process flow for the gate stack is explained in [17].



(**a**) (**b**)

Figure 9. *Cont.*

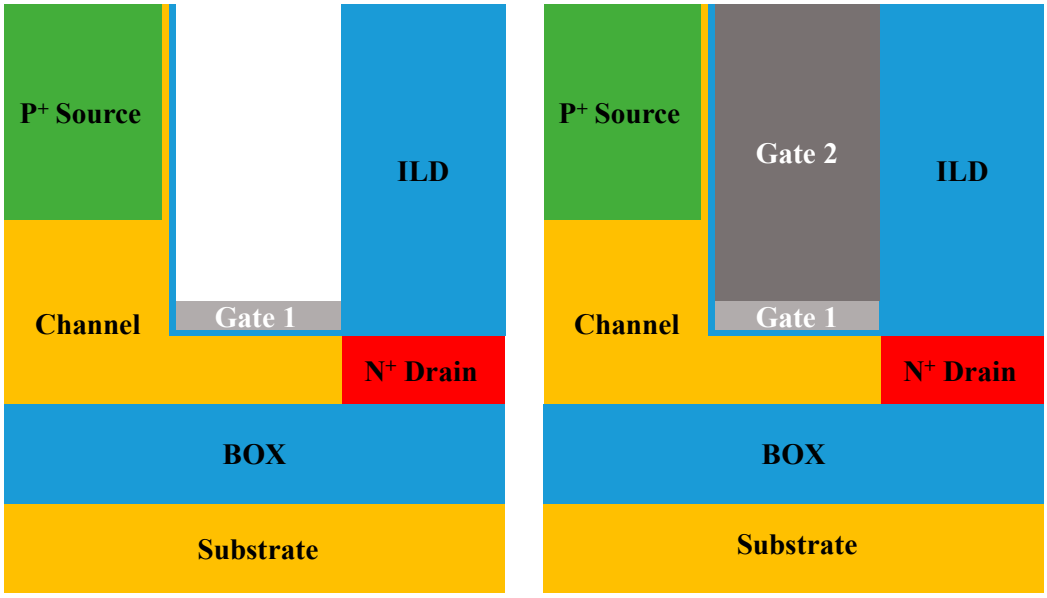


Figure 9. Key process steps for stacked gate L-shaped TFET. (**a**) Gate 2 is deposited by atomic layer deposition (ALD); (**b**) Gate 2 chemical mechanical polishing (CMP); (**c**) etch-back process; (**d**) Gate1 ALD & CMP.

4. Summary

In this study, we have successfully suppressed the ambipolar current of L-shaped TFET. The results prove that the ambipolar current can be efficiently suppressed by stacking the gates and using a low ϕ_{G2}. Compared with the other strategies for suppressing ambipolar behavior, the stacked gate method shows the best performance in terms of ambipolar current, on-current and self-aligned process feasibility. Consequently, the proposed device will be a better candidate for the future generation of ultra-low-power circuits.

Author Contributions: Conceptualization, J.Y. and S.K. (Sihyun Kim); Device simulation, J.Y. and C.K.; methodology, J.Y. and S.K. (Sihyun Kim); formal analysis, J.Y.; Writing—Original Draft preparation, J.Y.; Writing—Review and Editing, J.Y., K.L., D.R., C.K., J.-H.L., S.K. (Sangwan Kim), and B.-G.P.; supervision, S.K. (Sangwan Kim) and B.-G.P.

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Conflicts of Interest: The authors declare no conflict of interest.

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