micromachines

MDPI

Article

Electrical Performance and Bias-Stress Stability of Amorphous InGaZnO Thin-Film Transistors with Buried-Channel Layers

Ying Zhang, Haiting Xie and Chengyuan Dong *

Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai 200240, China; Zhangying0036@sjtu.edu.cn (Y.Z.); haitingx@163.com (H.X.)

* Correspondence: cydong@sjtu.edu.cn; Tel.: +86-021-3420-8271

Received: 17 October 2019; Accepted: 11 November 2019; Published: 14 November 2019

Abstract: To improve the electrical performance and bias-stress stability of amorphous InGaZnO thin-film transistors (a-IGZO TFTs), we fabricated and characterized buried-channel devices with multiple-stacked channel layers, i.e., a nitrogen-doped a-IGZO film (front-channel layer), a conventional a-IGZO film (buried-channel layer), and a nitrogen-doped a-IGZO film (back-channel layer). The larger field-effect mobility (5.8 $cm^2V^{-1}s^{-1}$), the smaller subthreshold swing value (0.8 V/dec, and the better stability (smaller threshold voltage shifts during bias-stress and light illumination tests) were obtained for the buried-channel device relative to the conventional a-IGZO TFT. The specially designed channel-layer structure resulted in multiple conduction channels and hence large field-effect mobility. The in situ nitrogen-doping caused reductions in both the front-channel interface trap density and the density of deep states in the bulk channel layers, leading to a small subthreshold swing value. The better stability properties may be related to both the reduced trap states by nitrogen-doping and the passivation effect of the nitrogen-doped a-IGZO films at the device back channels.

Keywords: amorphous InGaZnO; thin-film transistor; nitrogen-doping; buried-channel; stability

1. Introduction

Amorphous silicon thin-film transistors (a-Si TFTs) are the mainstream of active-matrix devices for flat panel displays (FPDs); additionally, polycrystalline (p-Si) TFTs are used to address some high-standard FPD products. In recent years, amorphous InGaZnO (a-IGZO) has been extensively studied as a potential material for the channel layers of TFT devices. In fact, a-IGZO TFTs are considered to replace silicon TFTs owing to their high mobility, low-temperature deposition, good large-area uniformity, and simple processing methods [1–3].

However, the electrical performance and stability properties of a-IGZO TFTs still need further improvements for their applications in FPDs and other fields [4,5]. Recently, some researchers—including our group—reported that nitrogen-doping (N-doping) effectively improved the electrical properties (e.g., subthreshold swing (SS) and bias-stress stability) of a-IGZO TFTs by decreasing the number of deep states and oxygen vacancies (Vo) in the device channel layers and reducing the channel/dielectric interface trap density with N atoms incorporated into the a-IGZO film [6–8]. However, the field-effect mobility (μ_{FE}) of the nitrogen-doped a-IGZO (a-IGZO:N) TFT devices also decreases due to the suppression of the oxygen vacancy (Vo) level in their channel layers, the main source of free electrons in oxide semiconductors [9,10]. Therefore, N-doping is an effective method for improving the electrical properties of a-IGZO TFTs, but its shortcomings still need to be overcome.

In this study, buried-channel a-IGZO:N TFTs, i.e., devices with multiple-stacked channel layers, were fabricated and evaluated. These devices showed better performance and stability than the

conventional devices. Specifically, the channel layer of the buried-channel device consisted of an a-IGZO:N layer (front-channel layer), an a-IGZO layer (buried-channel layer), and an a-IGZO:N layer (back-channel layer). We believe this device structure is a feasible approach to improving the electrical properties of a-IGZO TFTs.

2. Materials and Methods

Inverted staggered a-IGZO TFTs were prepared on p+ heavily doped silicon wafers with 100 nm thick thermal oxide (SiO_2). The silicon wafers and thermal SiO_2 were used as the gate electrodes and gate insulators of the TFT devices, respectively. For comparison, three types of TFT devices with different channel layers were fabricated, as shown in Figure 1. A 30 nm thick single channel layer was formed with conventional a-IGZO for Device A and with a-IGZO:N for Device B, respectively. Then, Device C with the buried-channel layer structure (10 nm thick a-IGZO:N (front-channel layer) + 10 nm thick a-IGZO (buried-channel layer) + 10 nm thick a-IGZO:N (back-channel layer)) was designed and prepared.

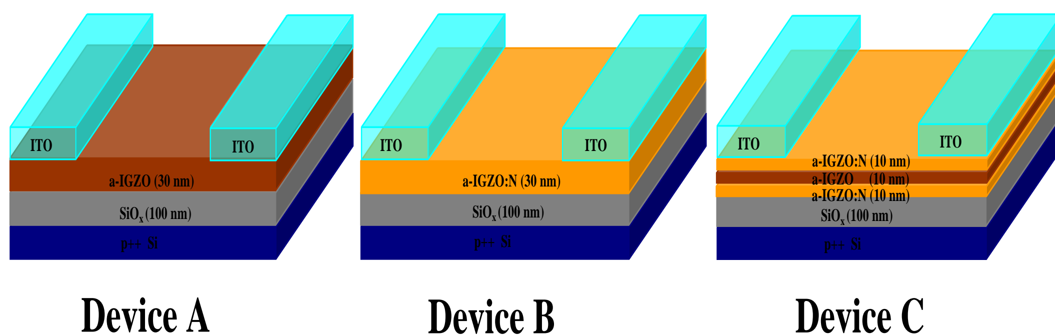

Figure 1. Schematic cross sections of the amorphous InGaZnO thin-film transistors (a-IGZO TFTs) prepared in this study.

The channel layers and the source/drain (S/D) electrodes were deposited with the RF-magnetron sputtering technique. The sputtering chamber was evacuated to a base pressure ($<3 \times 10^{-6}$ Torr) before the film depositions. The gas pressure was fixed at 3×10^{-3} Torr during the sputtering process. The channel layers were prepared at room temperature (RT) using an IGZO target (In_2O_3:Ga_2O_3:ZnO = 1:1:1 mol%); the RF power and the Ar flow rate were 60 W and 10 sccm, respectively. As for the depositions of the a-IGZO:N films, the nitrogen gas (N_2) was fed into the sputtering chamber at the flow rate of 1.2 sccm, and the Ar flow rate was fixed at 10 sccm. Then, the 100 nm thick indium-tin-oxide (ITO) layers were prepared as S/D electrodes in the same sputtering chamber. For simplicity, no passivation layers were prepared in this study. Both the channel layers and S/D electrodes were patterned by the shadow masks during sputtering; the channel width (W) and length (L) of the a-IGZO TFTs were fixed at 1000 and 250 μm, respectively. Finally, the TFT devices were annealed in N_2 atmosphere at 380 °C for 1 h.

The electrical measurements for the a-IGZO TFTs were performed at RT using an electrical analyzer (Keithley 4200, Keithley, Cleveland, OH, USA). For the transfer curve tests, the drain-source voltage (V_{DS}) was fixed at 10 V, and the gate-source voltage (V_{GS}) ranged from −20 to 40 V.

3. Results and Discussion

Figure 2 and Table 1 show the transfer curves and the corresponding extracted electrical parameters of the TFT devices, respectively. Here the μ_{FE} was obtained graphically from the square root of drain current ($I_{DS}{}^{1/2}$) versus the gate voltage (V_{GS}) in the saturation region using the intercept and maximum slope [11]. The threshold voltage (V_{TH}) was extracted from the gate voltage value where $I_{DS}/(W/L)$ = 1 nA. The subthreshold swing (SS) was defined as the half value of the difference between the gate voltages corresponding to the drain currents of 10^{-10} A and 10^{-8} A. The on–off current ratio (I_{ON}/I_{OFF})

was obtained from the ratio of the maximum and minimum drain current values within the V_{GS} range of −20 to ~40 V.

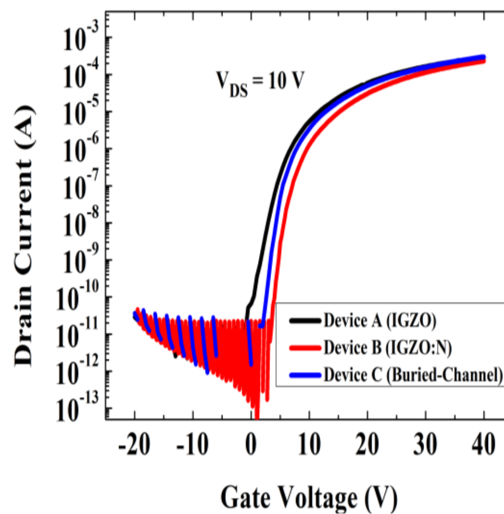

Figure 2. Transfer curves of the prepared TFTs (Devices A, B, and C).

Table 1. Extracted electrical parameters of the amorphous InGaZnO thin film transistors (a-IGZO TFTs).

Device	A	B	C
μ_{FE} ($cm^2V^{-1}s^{-1}$)	5.8	4.7	5.8
SS (V/dec)	1.3	0.8	0.8
V_{TH} (V)	2.0	5.0	3.5
I_{ON}/I_{OFF}	2.2×10^8	3.4×10^8	5.6×10^8

As switching devices in FPDs, TFTs are expected to have high field-effect mobility and low subthreshold swing, which can lead to better switching speed and smaller power consumption. As shown in Figure 2 and Table 1, the a-IGZO:N TFT (Device B) showed an improved SS value (0.8 V/dec) but degraded μ_{FE} (4.7 $cm^2V^{-1}s^{-1}$) compared with those of the conventional IGZO TFT (Device A, SS = 1.3 V/dec and μ_{FE} = 5.8 $cm^2V^{-1}s^{-1}$). In fact, this result was consistent with the other reported a-IGZO:N TFTs [7,9]. Besides, from Figure 2 one may clearly observe that the N-doping process could cause a positive V_{TH} shift for a-IGZO TFTs. As shown in Table 1, the V_{TH} increased from 2.0 V (Device A) to 5.0 V (Device B) with the nitrogen doped into the channel layers of the a-IGZO TFT. This result also agreed well with the findings of a recent study of a-IGZO:N TFTs [12]. Most importantly, the buried-channel TFT (Device C) showed the best electrical performance in this study. As shown in Table 1, Device C exhibited the smallest SS value (0.8 V/dec) as well as the largest μ_{FE} (5.8 $cm^2V^{-1}s^{-1}$) among all three devices. In addition, the V_{TH} of the buried-channel device (3.5 V) lay between those of the conventional a-IGZO TFT (Device A) and the a-IGZO:N TFT (Device B). It should be noted here that all the tested devices exhibited reasonably good I_{ON}/I_{OFF} values (>10^8), as shown in Figure 2 and Table 1.

Figure 3 shows the transfer curves of the a-IGZO TFTs under positive bias stress (PBS) tests. For measurements, the gate electrodes were applied by +30 V with the drain and source grounded; after a period, the transfer curves were instantly measured (V_{DS} = 10 V). As shown in Figure 3, the transfer curves of the three devices shifted positively to different extents as the stressing time elapsed. As shown in Figure 3a, the positive V_{TH} shift of the conventional a-IGZO TFT (Device A) was as large as +4.5 V under 2500 s of PBS testing. In contrast, the a-IGZO:N TFT (Device B) showed a much smaller V_{TH} shift (+3 V) than that of the conventional a-IGZO TFT, as shown in Figure 3b. As for the buried-channel device (Device C), the maximum V_{TH} shift value (+3.5 V, as shown in Figure 3c) lay between those of Devices A and B. In fact, the PBS stability of Device C was quite close to that of

Device B, as shown in Figure 3. In other words, during PBS tests, the buried-channel TFT (Device C) showed more stable properties than the conventional a-IGZO TFT (Device A).

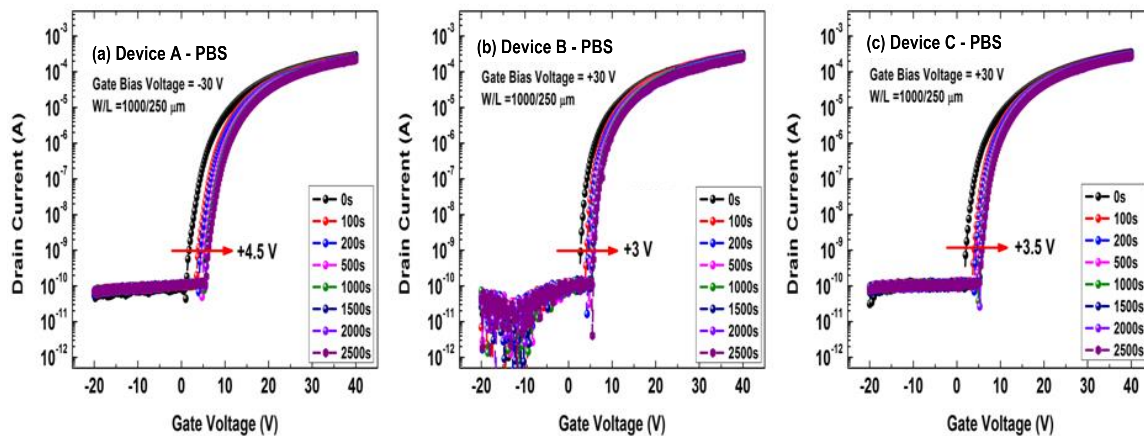

Figure 3. Positive bias stress (PBS) testing results of the a-IGZO TFTs: (**a**) the conventional a-IGZO TFT (Device A), (**b**) the a-IGZO:N TFT (Device B), and (**c**) the buried-channel TFT (Device C). The stressing conditions were V_{GS} = +30 V and V_{DS} = 0 V.

Figure 4 shows the transfer curves of the a-IGZO TFT devices under the negative bias stress (NBS) tests, where the stressing conditions were as follows: V_{GS} = −30 V and V_{DS} = 0 V. The NBS measurement operation was the same as that of PBS. One may observe from Figure 4 that the transfer curves of the three devices exhibited different negative shifts during NBS tests. As shown in Figure 4a,b, the maximum V_{TH} shift of the conventional a-IGZO TFT (−3.3 V) was much larger than that of the a-IGZO:N TFT (−1 V). Importantly, Device C showed a similar V_{TH} shift (−1.7 V after 2500 s of NBS testing) to that of Device B, implying that the buried-channel device (Device C) also exhibited better stability than the conventional a-IGZO TFT (Device A) during NBS tests.

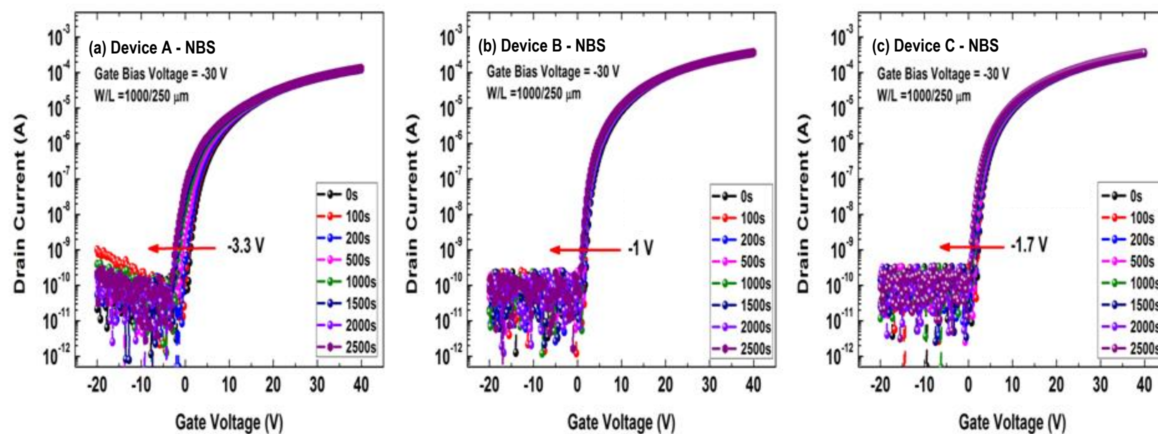

Figure 4. Negative bias stress (NBS) testing results of the a-IGZO TFTs: (**a**) the conventional a-IGZO TFT (Device A), (**b**) the a-IGZO:N TFT (Device B), and (**c**) the buried-channel TFT (Device C). The stressing conditions were V_{GS} = −30 V and V_{DS} = 0 V.

Figure 5 shows the transfer curves of the a-IGZO TFT devices under negative bias stress with ultraviolet (UV) light illumination (NBIS) tests. The stressing voltage was V_{GS} = −20 V; the wavelength and power intensity of the UV light were 380 nm and 0.1 mW/cm^2, respectively. Both the light illumination and gate stressing were applied for a period, and then the transfer curves were immediately measured (V_{DS} = 10 V). According to Figure 5, one may notice that all three devices exhibited serious negative shifts during NBIS tests. As shown in Figure 5a, the maximum V_{TH} shift of the conventional a-IGZO TFT (Device A) was up to −7 V, which was the worst among all the tested samples. However,

this negative V_{TH} shift could be effectively reduced to −3 V using the buried-channel structure (as shown in Figure 5c) or to −2 V by adopting the N-doping technology (as shown in Figure 5b). Apparently, the NBIS stability of Device C was more similar to that of Device B than that of Device A. In other words, the experimental results proved that the buried-channel device (Device C) could lead to a significant improvement in NBIS stability compared with the conventional a-IGZO TFT (Device A).

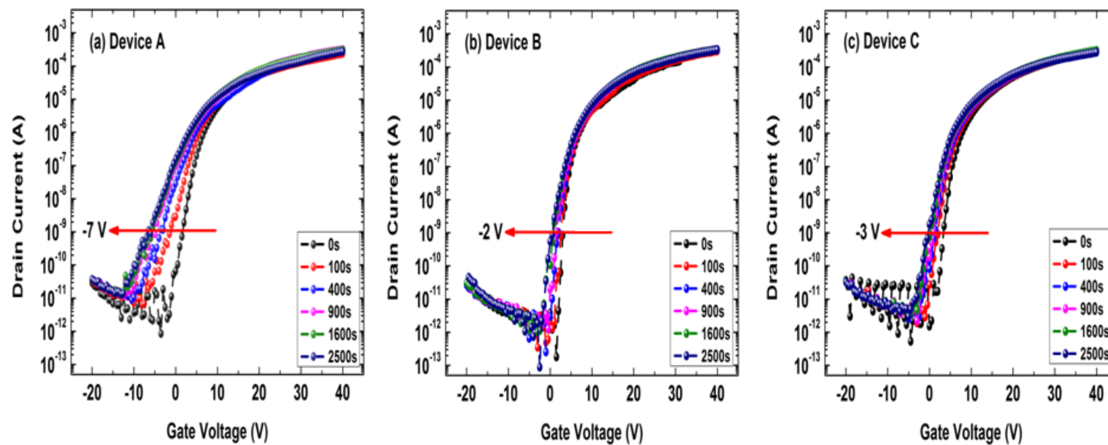

Figure 5. Negative bias stress with ultraviolet (UV) light illumination (NBIS) testing results of the a-IGZO TFTs: (**a**) the conventional a-IGZO TFT (Device A), (**b**) the a-IGZO:N TFT (Device B), and (**c**) the buried-channel TFT (Device C). The stressing voltage was V_{GS} = −20 V; the wavelength and power intensity of the UV light used in this test were 380 nm and 0.1 mW/cm^2, respectively.

It has been reported by our group and other researchers that the field-effect mobilities of oxide semiconductor TFTs were evidently improved by employing the double-stacked channel layers (DSCL) with a high defect-density channel layer and a low defect-density channel layer [13–15]. In this study, we further designed and prepared the buried-channel a-IGZO:N TFTs using the multiple-stacked channel layers composed of a 10 nm thick a-IGZO:N layer (front-channel layer), a 10 nm thick a-IGZO layer (buried-channel layer), and a 10 nm thick a-IGZO:N layer (back-channel layer). This design exhibited the best electrical performance (e.g., the smallest SS value, the largest μ_{FE}, and the optimum V_{TH}), as shown in Table 1. Furthermore, the buried-channel device exhibited similar stable properties to those of the a-IGZO:N TFT during PBS, NBS, and NBIS tests, which were much better than those of the conventional a-IGZO TFT. The related physical mechanisms could be ascertained by analyzing the channel-layer structure of these devices.

Figure 6 shows the energy band diagrams for Devices A, B, and C. As reported previously [7,9], N-doping caused a mobility reduction due to the significant suppression of the Vo level in the bulk channel layer. Former studies [15–17] indicated that N-doping reduced the Vo and defect density in the a-IGZO films. Hence, there was more Vo acting as the origin of free carriers in the conventional a-IGZO layer compared with that in the a-IGZO:N film. Therefore, one could assume that fewer free electrons took part in conductivity for Device B compared with the case for Device A (as shown in Figure 6a,b). This resulted in a lower mobility for Device B.

But, why did the buried-channel device not show degraded mobility as the a-IGZO:N TFT did? We attributed this fact to the particular energy band structure of the buried-channel device, as shown in Figure 6c. The electrons tended to inject from the conventional a-IGZO layer towards both the bottom a-IGZO:N layer and the top a-IGZO:N layer owing to the electron concentration difference between the conventional a-IGZO layer and the a-IGZO:N layer. Due to the positive polarity of the a-IGZO layer, the electrons accumulated in both the bottom a-IGZO:N/a-IGZO interface and the top a-IGZO/a-IGZO:N interface. During the operation of the buried-channel TFT device, these accumulated electrons also took part in conductivity, forming a first sub-channel at the bottom a-IGZO:N/a-IGZO interface and a second sub-channel at the top a-IGZO/a-IGZO:N interface. In other words, the conduction current

in the buried-channel TFT was not only dominated by the main channel (channel layer/dielectric layer interface), but also the two additional sub-channels (bottom a-IGZO:N/a-IGZO interface and top a-IGZO/a-IGZO:N interface). The total carrier concentration from these three conduction channels in the buried-channel device might be comparable only with that from the front channel in the conventional a-IGZO TFT, as shown in Figure 6a,c, leading to the μ_{FE} values of the buried-channel device (Device C) that were nearly equal to those of the conventional a-IGZO TFT (Device A). In fact, these qualitative analyses might also be confirmed by numerical simulations, which are commonly used in explaining and discussing electrical properties of semiconductor devices [18,19]. The related study is still ongoing.

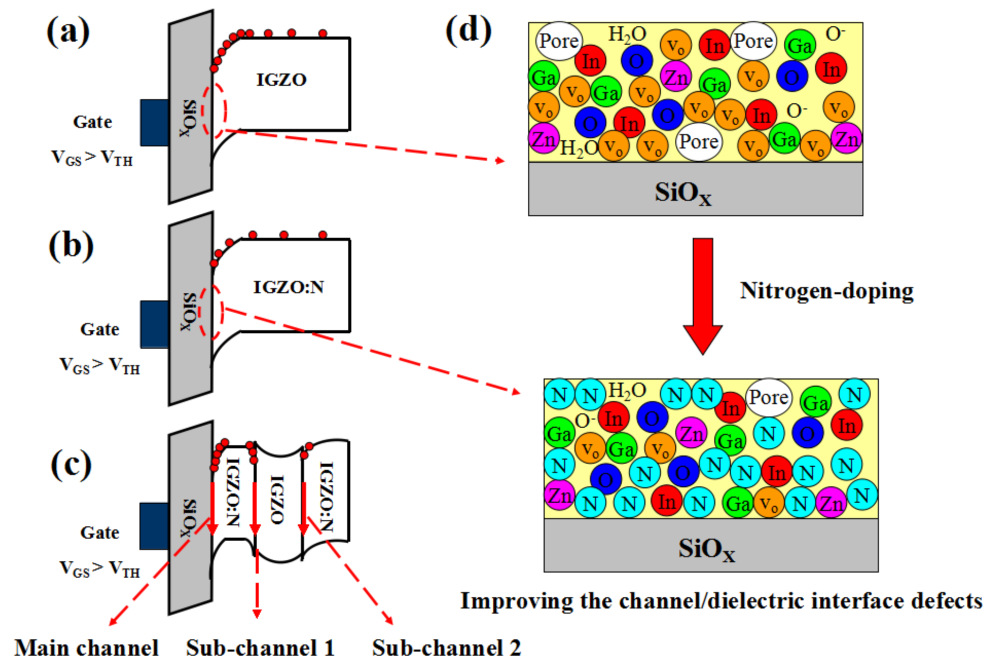

Figure 6. Energy band diagrams for (**a**) the conventional a-IGZO TFT (Device A), (**b**) the a-IGZO:N TFT (Device B), and (**c**) the buried-channel a-IGZO TFT (Device C). (**d**) The schematic illustration of the improvement effect for the N-doping process on the trap states in the bulk-layers and interfaces.

As mentioned before, N-doping effectively decreased the interface trap density as well as the deep defect density in the channel layer by incorporating the N atoms into the a-IGZO film (as shown in Figure 6d). Since the SS values of TFTs are closely related to the channel/dielectric trap density and the number of deep states in the channel layers [7,9,20], it is quite reasonable that the a-IGZO:N TFT had smaller SS values than the conventional a-IGZO TFT. As shown in Figure 6b,c, both the front-channel interface and the nearby channel layer of the buried-channel device were the same as those of the a-IGZO:N TFT, which naturally led to the same SS values for both cases.

The evident stability improvements (during PBS, NBS, and NBIS tests) of the a-IGZO:N TFT with respect to the conventional a-IGZO TFTs were assumed to result from the following reasons. First, the incorporation of N atoms into the a-IGZO film led to the suppression of trap states in the bulk channel layer as well as those in the front-channel interface (as shown in Figure 6d). Second, the nitrogen atoms doped at the back channel might act as a passivation layer, which could effectively protect the device from the influence of ambient gas (such as O_2, moisture, etc.). Third, the back-channel a-IGZO:N layer might shield the channel from UV light influence to a certain extent. As for the buried-channel device, the aforementioned stability-improving effects were also valid. However, the existence of the buried-channel layer (a-IGZO) more or less increased the trap states in the bulk channel layers compared with the a-IGZO:N TFT (Device B). Therefore, the stability properties (PBS,

NBS, and NBIS) of the buried-channel device (Device C) were a little worse than those of the a-IGZO:N TFT (Device B), but still much better than those of the conventional a-IGZO TFT (Device A).

So far, we can make some overall comments on the buried-channel TFT devices. Compared with the conventional a-IGZO TFT, the buried-channel device exhibited better electrical performance (smaller SS value and non-degraded μ_{FE}) and more stable properties (much smaller V_{TH} shifts during PBS, NBS, and NBIS tests). Compared with the a-IGZO:N TFT, the buried-channel device showed a little worse stability under PBS, NBS, and NBIS tests, but better electrical properties (larger μ_{FE} and the same SS value). Notably, the buried-channel structure could be easily achieved by one-pump-down depositions in the sputtering machines. Therefore, we believe the use of buried-channel devices is a feasible approach for improving the electrical performance and stability properties of amorphous oxide thin-film transistors.

4. Conclusions

Buried-channel TFTs with multiple-stacked channel layers including an a-IGZO:N film (front-channel layer), an a-IGZO film (buried-channel layer), and an a-IGZO:N film (back-channel layer) were fabricated and measured in this work. Compared with those of the conventional a-IGZO TFT, the better electrical performance (e.g., smaller SS value, larger μ_{FE}, and optimum V_{TH}) as well as the improved stability properties (e.g., smaller V_{TH} shifts during PBS, NBS, and NBIS tests) were obtained for the buried-channel device. The a-IGZO:N film used as the front-channel layer in the buried-channel structure could reduce both the interface trap density and the bulk-layer deep state density, leading to a smaller SS value (0.8 V/dec) in comparison with the conventional a-IGZO TFT device (SS = 1.3 V/dec). The non-degraded μ_{FE} (5.8 $cm^2V^{-1}s^{-1}$) for the buried-channel TFT might be attributed to its three conduction channels, including the main channel at the interface between the channel layer and the dielectric layer, the first sub-channel formed at the bottom a-IGZO:N/a-IGZO interface, and the second sub-channel formed at the top a-IGZO/a-IGZO:N interface. In addition, the improved bias-stress and NBIS stability of the buried-channel TFT compared with those of the conventional a-IGZO TFT might be mainly due to the suppression of the trap states in the bulk channel layers, the reduction in the defects at the front-channel interface, and the passivation effect created by using the a-IGZO:N film as the back-channel layer.

Author Contributions: Y.Z. and H.X. fabricated and measured all the a-IGZO TFTs. Y.Z. and C.D. designed the experiments and contributed to the theoretical explanations. The manuscript was written and revised by all the authors.

Funding: This work was supported by Natural Science Foundation of China (Grant No. 61474075).

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Nomura, K.; Ohta, H.; Takagi, A.; Kamiya, T.; Hirano, M.; Hosono, H. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature* **2004**, *432*, 488–492. [CrossRef] [PubMed]
2. Zhou, Y.; Dong, C. Influence of passivation layers on positive gate bias-stress stability of amorphous InGaZnO thin-film transistors. *Micromachines* **2018**, *9*, 603. [CrossRef] [PubMed]
3. Ide, K.; Ishikawa, K.; Tang, H.; Katase, T.; Hiramatsu, H.; Kumomi, H.; Hosono, H.; Kamiya, T. Effects of base pressure on growth and optoelectronic properties of amorphous In-Ga-Zn-O: Ultralow optimum oxygen supply and bandgap widening. *Phys. Status Solidi A* **2019**, *216*. [CrossRef]
4. Choi, S.; Kim, J.Y.; Kang, H.; Ko, D.; Rhee, J.; Choi, S.J.; Kim, D.M.; Kim, D.H. Effect of oxygen content on current stress-induced instability in bottom-gate amorphous InGaZnO thin-film transistors. *Materials* **2019**, *12*, 3149. [CrossRef] [PubMed]
5. Dong, C.; Xu, J.; Zhou, Y.; Zhang, Y.; Xie, H. Light illumination stability of amorphous InGaZnO thin film transistors in oxygen and moisture ambience. *Solid State Electron.* **2019**, *153*, 74–78. [CrossRef]

6. Liu, P.T.; Chou, Y.T.; Teng, L.F.; Li, F.H.; Shieh, H.P. Nitrogenated amorphous InGaZnO thin film transistor. *Appl. Phys. Lett.* **2011**, *98*. [CrossRef]
7. Raja, J.; Jang, K.; Balaji, N.; Yi, J. Suppression of temperature instability in InGaZnO thin-film transistors by in situ nitrogen doping. *Semicond. Sci. Technol.* **2013**, *28*, 115010. [CrossRef]
8. Xie, H.; Zhou, Y.; Zhang, Y.; Dong, C. Chemical bonds in nitrogen-doped amorphous InGaZnO thin film transistors. *Results Phys.* **2018**, *11*, 1080–1086. [CrossRef]
9. Raja, J.; Jang, K.; Balaji, N.; Choi, W.; Trinh, T.T.; Yi, J. Negative gate-bias temperature stability of N-doped InGaZnO active-layer thin-film transistors. *Appl. Phys. Lett.* **2013**, *102*. [CrossRef]
10. Ryu, B.; Noh, H.K.; Choi, E.A.; Chang, K.J. O-vacancy as the origin of negative bias illumination stress instability in amorphous In–Ga–Zn–O thin film transistors. *Appl. Phys. Lett.* **2010**, *97*, 022108. [CrossRef]
11. Aikawa, S.; Darmawan, P.; Yanagisawa, K.; Nabatame, T.; Abe, Y.; Tsukagoshi, K. Thin-film transistors fabricated by low-temperature process based on Ga- and Zn-free amorphous oxide semiconductor. *Appl. Phys. Lett.* **2013**, *102*, 102101. [CrossRef]
12. Huang, X.; Wu, C.; Lu, H.; Ren, F.; Chen, D.; Zhang, R.; Zheng, Y. Enhanced bias stress stability of a-InGaZnO thin film transistors by inserting an ultra-thin interfacial InGaZnO:N layer. *Appl. Phys. Lett.* **2013**, *102*, 193505. [CrossRef]
13. Park, J.C.; Lee, H.N. Improvement of the performance and stability of oxide semiconductor thin-film transistors using double-stacked active layers. *IEEE Electron Dev. Lett.* **2012**, *33*, 818–820. [CrossRef]
14. Zhan, R.; Dong, C.; Yang, B.R.; Shieh, H.P. Modulation of interface and bulk states in amorphous InGaZnO thin film transistors with double stacked channel layers. *Jpn. J. Appl. Phys.* **2013**, *52*, 090205. [CrossRef]
15. Xie, H.; Wu, Q.; Xu, L.; Zhang, L.; Liu, G.; Dong, C. Nitrogen-doped amorphous oxide semiconductor thin film transistors with double-stacked channel layers. *Appl. Surf. Sci.* **2016**, *387*, 237–243. [CrossRef]
16. Nguyen, T.T.; Renault, O.; Aventurier, B.; Rodriguez, G.; Barnes, J.P.; Templier, F. Analysis of IGZO thin-film transistors by XPS and relation with electrical characteristics. *J. Disp. Technol.* **2013**, *9*, 770–774. [CrossRef]
17. Raja, J.; Jang, K.; Balaji, N.; Hussain, S.Q.; Velumani, S.; Chatterjee, S.; Kim, T.; Yi, J. Aging effects on the stability of nitrogen-doped and un-doped InGaZnO thin-film transistors. *Mater. Sci. Semicond. Process.* **2015**, *37*, 129–134. [CrossRef]
18. Bencherif, H.; Dehimi, L.; Pezzimenti, F.; Corte, F.G.D. Temperature and SiO_2/4H-SiC interface trap effects on the electrical characteristics of low breakdown voltage MOSFETs. *Appl. Phys. A* **2019**, *125*, 294. [CrossRef]
19. Megherbi, M.L.; Pezzimenti, F.; Dehimi, L.; Saadoune, M.A.; Corte, F.G.D. Analysis of trapping effects on the forward current-voltage characteristics of al-implanted 4H-SiC p-i-n Diodes. *IEEE Trans. Electron Dev.* **2018**, *65*, 3371–3378. [CrossRef]
20. Nomura, K.; Kamiya, T.; Hosono, H. Highly stable amorphous In-Ga-Zn-O thin-film transistors produced by eliminating deep subgap defects. *Appl. Phys. Lett.* **2011**, *99*, 053505. [CrossRef]

© 2019 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).