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A Novel GaN Metal-Insulator-Semiconductor High Electron Mobility Transistor Featuring Vertical Gate Structure

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Abstract: A novel structure scheme by transposing the gate channel orientation from a long horizontal one to a short vertical one is proposed and verified by technology computer-aided design (TCAD) simulations to achieve GaN-based normally-off high electron mobility transistors (HEMTs) with reduced on-resistance and improved threshold voltage. The proposed devices exhibit high threshold voltage of 3.1 V, high peak transconductance of 213 mS, and much lower on-resistance of 0.53 mΩ·cm² while displaying better off-state characteristics owing to more uniform electric field distribution around the recessed gate edge in comparison to the conventional lateral HEMTs. The proposed scheme provides a new technical approach to realize high-performance normally-off HEMTs.

Keywords: wide-bandgap semiconductor; high electron mobility transistors; vertical gate structure; normally-off operation; gallium nitride

1. Introduction

Wide-bandgap GaN-based high electron mobility transistors (HEMTs) are promising candidates in the applications of high-frequency and high-power electronics owing to their superior material properties such as large bandgap, high critical breakdown field, and high-density carriers in the form of two-dimensional electron gas (2DEG) with high mobility over 2000 cm²/V·s [1–5]. Nowadays, much progress has been achieved in GaN-based HEMTs with the development of the material quality and the innovation of the device structure [6,7]. However, there are still several important issues unaddressed, among which, the normally-off operation with a large threshold voltage (V_{th}) is a big concern when the chip products are pushed toward the market [8–10]. Several device architectures, such as p-GaN cap, barrier layer-recessed, fluorinated-gate, and cascode-connected metal-insulator-semiconductor high electron mobility transistors (MIS-HEMTs), have been reported to shift the threshold voltage to be positive [11–16]. Indeed, the device performances have been improved significantly in the past ten years. However, these normally-off HEMTs still suffer from either large on-resistance (R_{on}) or low V_{th} which increases the risk of device switching failure. Basically, the enhancement of V_{th} comes at the expense of increasing the R_{on} of the devices. A trade-off, hence, has to be made between them [17]. In recent years, several novel normally-off schemes such as tri-gate, Fin-gate, and trench etching in the SiO₂ buried layer have also been proposed and developed [18–20].

However, a truly effective device structure to gain both high V_{th} and low R_{on} simultaneously should be developed to resolve the mentioned issues effectively.

In this work, a novel scheme featuring a vertical short gate channel is proposed and demonstrated in AlGaIn/GaN MIS-HEMTs to realize the normally-off operation. The source electrode is located at the trenched GaN bulk region with gate dielectric layer covering the side wall. The proposed vertical gate HEMT (VG-HEMT) is able to get a higher V_{th} (>3 V) and at the same time a lower R_{on} due to the short vertical channel (200–500 nm in this work). To verify this design, a conventional HEMT was fabricated and its output characteristics were utilized to extract the physical parameters for the subsequent TCAD simulations for the VG-HEMT design which finally exhibits a much higher output current and transconductance (g_m) while displaying a better off-state electric field profile. The quantitative dependences of saturated current density and R_{on} on scattering factors in the trenched vertical gate channel were also investigated in detail in the work.

2. The Proposed Device and Physical Principle

Figure 1 shows the cross-sectional schematics of GaN-based HEMTs, where the same L_{GD} (distance between gate and drain) and gate length (including the gate overlap) have been employed. In the conventional lateral gate-recessed HEMTs (LG-HEMTs), as shown in Figure 1a, the length of the recessed gate is usually designed to be 1–3 μm , which is limited by the influence of the UV light diffraction in the lithography process. It is hard to get very high pattern resolution just using the common mask aligner. If the pattern resolution below 1 μm is required, a more precise and expensive lithography apparatus such as stepper has to be used. The technology processes, such as gate channel etching and metal lift-off, with resolution below 1 μm are more rigorous and challenging, and hence increase the cost. It is not easy to control the precision around few nanometers for fully etching just the thin AlGaIn barrier (~ 20 nm), and the resulting over-etch leads to a severe degradation of 2DEG channel mobility. Therefore, an unstable V_{th} and large R_{on} are still the typical issues unaddressed till now.

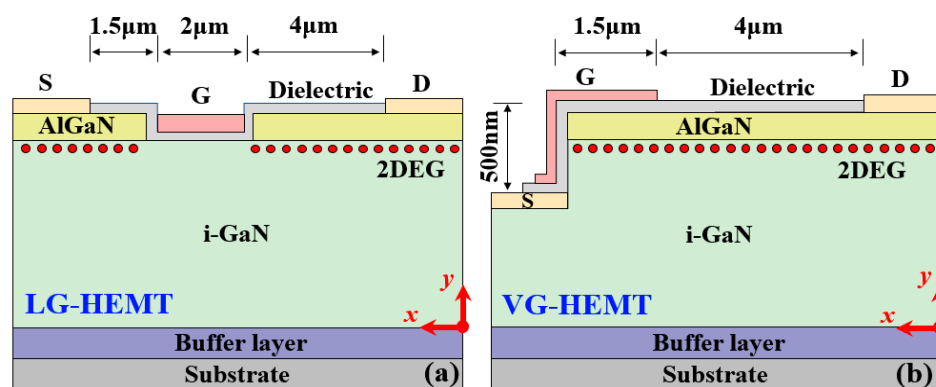


Figure 1. Cross-sectional schematics of (a) the lateral gate-recessed-high electron mobility transistors (LG-HEMT) and (b) the vertical gate HEMT (VG-HEMT).

In contrast to this, the conductive 2DEG channel is removed completely by fine etching in the VG-HEMTs and the source electrode is placed at the wafer body, as shown in Figure 1b. A decent source contact can be formed by Si ion implantation beneath the source region and post-annealing treatment [21]. To address the mismatch issue, the self-aligned technology will be employed in the future to precisely adjust the source metal edge to the edge of the recessed region. To make a better isolation between gate and source, a multiple dielectric stack or a relative thick dielectric film (e.g., 30 nm) will be employed. The vertical gate on the sidewall can modulate the electric field in the vertical channel for electron accumulation and hence control the device on/off switching. Considering the large G-to-S capacitance, the VG-HEMT devices will not be used in high-frequency or microwave applications. But, for the conventional switching applications at the frequency less than 1.0 MHz,

they should be able to handle. Moreover, more schemes such as increasing the dielectric thickness between the gate and source and reducing the overlap dimension of the gate electrode will be employed to reduce the capacitance. To improve the gate breakdown endurance, the bi-layer dielectric and slanted gate schemes are considered and the gate overdrive circuit will also be designed to protect the device. Compared with the long recessed-gate channel in the LG-HEMTs, the main benefits in the VG-HEMTs include a shorter gate channel originated from the low-mobility trenched region based on a simple lithography technique and greater tolerance on etching depth error. Therefore, the device is able to achieve both high V_{th} and low R_{on} .

3. Fabrication Work and Parameter Calibration for TCAD simulation

The heterostructure comprising 25 nm $Al_{0.2}Ga_{0.8}N$ barrier layer and 4 μm undoped GaN channel and buffer layers was grown on a 6-inch p-Si (111) substrate by metal-organic chemical vapor deposition (MOCVD) technique. The conventional GaN-based HEMTs were fabricated and characterized. The fabrication work started with the device isolation by employing Cl⁻-based plasma etching. Source and drain contacts were formed by depositing Ti/Al/Ni/Au stack using E-beam evaporation system followed by a rapid thermal annealing (RTA) at 875 °C for 30 s in N₂ atmosphere. The gate electrode was deposited by evaporating Ni/Au alloy. Then, 300 nm SiO₂ layer was deposited on the device surface at 300 °C by plasma enhanced chemical vapor deposition (PECVD) system for passivation purpose. Figure 2a indicates the structural schematic of the GaN HEMT. Figure 2b shows the microscopy image of the fabricated device and the I–V characteristics measured using Agilent B1505A system and benchmarked by the simulation data.

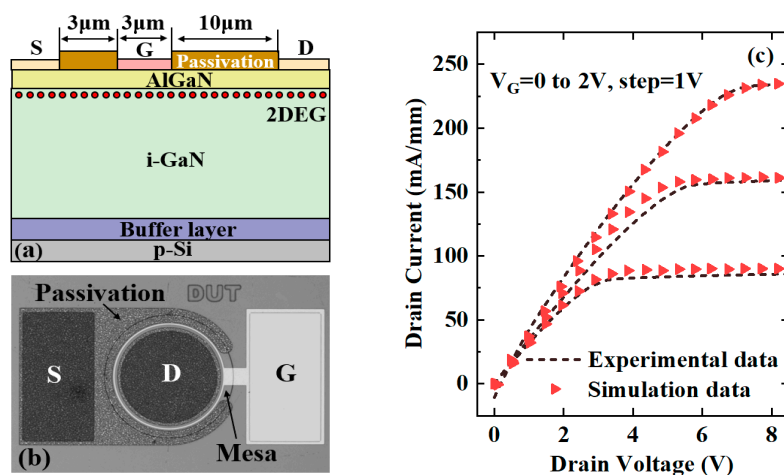


Figure 2. (a) Schematic and (b) microscopy image of the fabricated normally-on AlGaN/GaN HEMTs, and (c) comparisons of output I–V characteristics of the devices for physical parameter calibration.

In TCAD simulations, Auger recombination, Shockley–Read–Hall (SRH) recombination, and Van Overstraeten–De Man models were used to simulate the device behaviors. To investigate the dry etching effects on the carrier mobility of gate channel in the normally-off devices, several mobility models were selected. The Arora model was employed to determine the doping-dependent mobility in the low-field case, and the transferred electron model was used to describe the effect of a transfer of electrons into an energetically higher side valley with a much larger effective mass in the high-field case [22]. The mobility degradations caused by high field and interface scattering are given by Meinerzhagen–Engl model and Lombardi model, respectively [23,24]. The comparison of simulated output I–V characteristics with the measurement data is shown in Figure 2c. The displayed I–V curves match well and the average mismatch for the current density is within 5%. This confirms the validity of the parameters used in the simulations. The physical parameters used in simulation are listed in Table 1 [3]. Especially, in the VG-HEMT, it is also of great importance to know the the mobility

degradation at the etched sidewall. Thus, the effects of the etched roughness at the gate region on the device performances were investigated in detail in the next section.

Table 1. Physical parameters used in technology computer-aided design (TCAD) simulations after calibration [3].

Physical Parameters	Values
Electron effective mass in GaN	$0.22 \cdot m_e$
Electron affinity	3.4 eV
Relative dielectric constant in GaN	9.7
Background electron concentration in i-GaN layer	$5.0 \times 10^{15} \text{ cm}^{-3}$
Electron mobility in 2DEG channel	$1500 \text{ cm}^2/(\text{V}\cdot\text{s})$
2DEG sheet density	$8.0 \times 10^{12} \text{ cm}^{-2}$
Electron saturation velocity in GaN	$1.8 \times 10^7 \text{ cm/s}$

4. Results and Discussions

The output I–V characteristics of the normally-off LG-HEMT and VG-HEMT are illustrated in Figure 3. The V_{th} values are defined by extrapolating the linear section of the I_D – V_G curve to the voltage axis. The normally-off operation with a positive V_{th} is realized in both devices. The VG-HEMT exhibits a V_{th} of 3.1 V and a high peak g_m of 213 mS/mm compared with 3.6 V and 114 mS/mm in the LG-HEMT, respectively. The similar V_{th} values in both devices are found when the influence of the polar plane is ignored considering the fact that usually the gate surface polarization might be damaged severely after a long-time plasma etching in the gate recess process and the polarization charges at the lateral surface are generally compensated by the high-density surface states, such as donor-like traps.

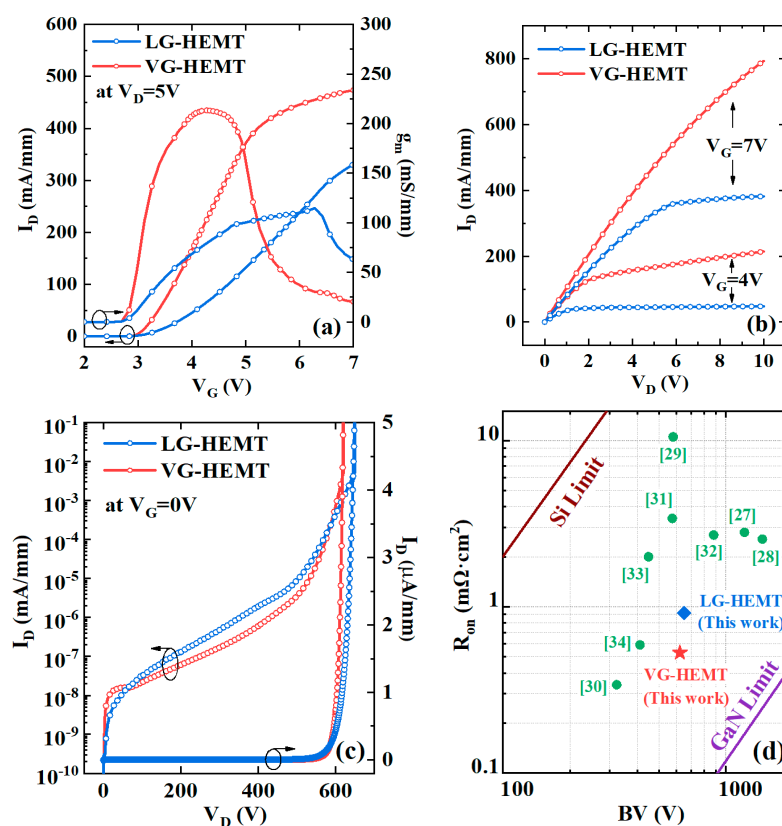


Figure 3. Comparisons of (a) transfer characteristics, (b) output I_D – V_D curves, and (c) off-state breakdown characteristics between the LG-HEMT and VG-HEMT devices, and (d) performance comparisons among the reported normally-off HEMTs including the VG-HEMT in this work (the red star).

Theoretically, the V_{th} model for the MIS-HEMT can be expressed in Equation (1) [25]:

$$V_{th} = \frac{\varphi_b}{q} - \frac{\Delta E_c}{q} - \frac{\varphi_f}{q} - \frac{q \cdot \Delta Q_{it} t_{ox}}{\varepsilon_{ox}} \quad (1)$$

where φ_b is the barrier height for gate metal on the dielectric (3.2 eV for Ni on Si_3N_4), ΔE_c the conduction band offset between Si_3N_4 and GaN (1.5 eV), φ_f the conduction band distance from the Fermi-level in GaN (0.2 eV), t_{ox} the dielectric thickness (20 nm), ε_{ox} the permittivity of dielectric (6.6×10^{-13} F/cm), and ΔQ_{it} the net charge density at the interface ($\sim 3.4 \times 10^{12}$ cm^{-2} in this work which is reasonable and reported widely for the III-V group GaN-based materials) [26,27]. The calculated V_{th} of the VG-HEMT is found to be 3.2 V, which is roughly consistent with the simulation data at 3.1 V. Furthermore, the slight difference of the V_{th} value between the two devices is mainly caused by the increased drain current and transconductance values in the VG-HEMT considering that the effective vertical gate length is much less than that in the LG-HEMT. The maximum current density and R_{on} are found to be 793 mA/mm and $0.53 \text{ m}\Omega \cdot \text{cm}^2$ at $V_G = 7$ V in the VG-HEMT, while 381 mA/mm and $0.92 \text{ m}\Omega \cdot \text{cm}^2$ in LG-HEMT, respectively. The VG-HEMT shows a higher drain current mainly owing to the saving of the L_{GS} length by placing the source electrode under the gate and a shorter gate channel originated from the low-mobility trenched region. The shorter total channel length and narrower trenched-gate originated from the structural feature of the proposed VG-HEMT result in the increase of the drain current. Furthermore, a similar off-state breakdown voltage level (606 V vs. 615 V at $I_{D,off} = 1$ $\mu\text{A}/\text{mm}$) is revealed between the VG-HEMT and LG-HEMT, as shown in Figure 3c. The proposed VG-HEMT exhibits even a lower drain leakage current owing to a more uniform electric field distribution. Figure 3d gives the performance comparisons with other reported normally-off HEMTs, which clearly indicates the advantage of the proposed scheme by employing a vertical short gate structure [27–34].

To further investigate the electrical behaviors of the VG-HEMT, its energy band and electron density distributions at different biases are calculated and compared, as shown in Figure 4a,b. The conduction band of vertical channel is pulled down to the Fermi level with the increasing gate and drain bias and an electron density peak is formed in the conduction channel. The surface potential of the semiconductor can be affected by the different dielectric deposition processes due to the influence of the high-density dielectric/GaN interface traps (10^{12} – 10^{13} cm^{-2}) and the short distance to the conduction channel. As a result, the conduction band bending occurs at the interface, as shown in Figure 4a. The concentration of the accumulated electrons is given by Equation (2) [35]:

$$n_e = \frac{C_{ox}}{q} \cdot \left(V_g - \frac{\varphi_b - \varphi_{it} - \varphi_f - \Delta E_c}{q} \right) \quad (2)$$

where C_{ox} is the capacitance of the gate dielectric (3.32×10^{-7} F/cm²), V_g the applied gate voltage, and φ_{it} the impact on the surface potential caused by the interface electrons. Using the ΔQ_{it} value of 3.4×10^{12} cm^{-2} , the calculated peak n_e at $V_g = 7$ V is 7.8×10^{12} cm^{-2} , which is approximately consistent with the data of 7.2×10^{12} cm^{-3} for the blue line after integral calculation in Figure 4b.

Furthermore, the physical mechanisms of output current conduction in the VG-HEMT were analyzed. The I_D – V_D characteristics of these two devices are compared because they have similar electrode distance L_{GD} and gate length L_G . A decent source contact technology will make it easier to obtain a low source resistance and minimize the effect on the on-resistance. In this case, the surface roughness at the etched gate region becomes the major factor that influences the on-resistance of the device. The mobility degradation in the etched vertical channel is strongly dependent on several scattering factors. The sidewall channel mobility μ is modeled by the following expression based on Lombardi model [36]:

$$\frac{1}{\mu} = \frac{1}{\mu_{ac}} + \frac{1}{\mu_b} + \frac{1}{\mu_{sr}} \quad (3)$$

where μ_{ac} is the mobility contribution by acoustic phonon scattering, μ_b the carrier mobility in bulk, and μ_{sr} the mobility contribution by surface roughness scattering. In the simulations, μ_{ac} was determined to be $818 \text{ cm}^2/(\text{V}\cdot\text{s})$ using the equation $\mu_{ac} = (\text{BT}/E_{\text{eff}} + \text{C}/E_{\text{eff}}^{(1/3)}) \cdot (1/T)$ [24], where E_{eff} is the effective field controlled by the channel charge, T ($= 300 \text{ K}$) is the temperature, and B ($= 9 \times 10^7 \text{ cm/s}$) and C ($= 5.8 \times 10^2 \text{ cm}^{5/3}\cdot\text{V}^{-2/3}\cdot\text{s}^{-1}$) are the fitting parameters, respectively [37]. The μ_b value of $803 \text{ cm}^2/(\text{V}\cdot\text{s})$ is extracted from the calibration data. Considering that μ_{ac} and μ_b are almost constant for a technically mature GaN wafer at a certain temperature, μ in the vertical channel is mainly modulated by μ_{sr} , which can be expressed as [33]:

$$\mu_{sr} = \frac{\delta}{E_{\text{eff}}^\alpha} \tag{4}$$

where α is determined by the experimental fitting. And δ is inversely proportional to the root mean square (RMS) value of the surface roughness, and is the main factor resulting in mobility degradation at the etched surface. The μ_{sr} value was then determined to be $1114 \text{ cm}^2/(\text{V}\cdot\text{s})$ by employing the parameters extracted from the simulation. Therefore, the mobility value of $297 \text{ cm}^2/(\text{V}\cdot\text{s})$ was achieved for the sidewall channel in VG-HEMT. The quantitative effects of δ values on the drain current density and R_{on} are shown in Figure 4c,d, taking into account the effect from the roughness scattering [37]. The VG-HEMT exhibits much better current characteristics owing to the less scattering amount in the shorter gate channel, as shown in Figure 4c. Moreover, to further investigate the effect of etching damage on the output characteristic, as well as distinguish the specific damage between the sidewall and surface, more experiments will be carried out in future work.

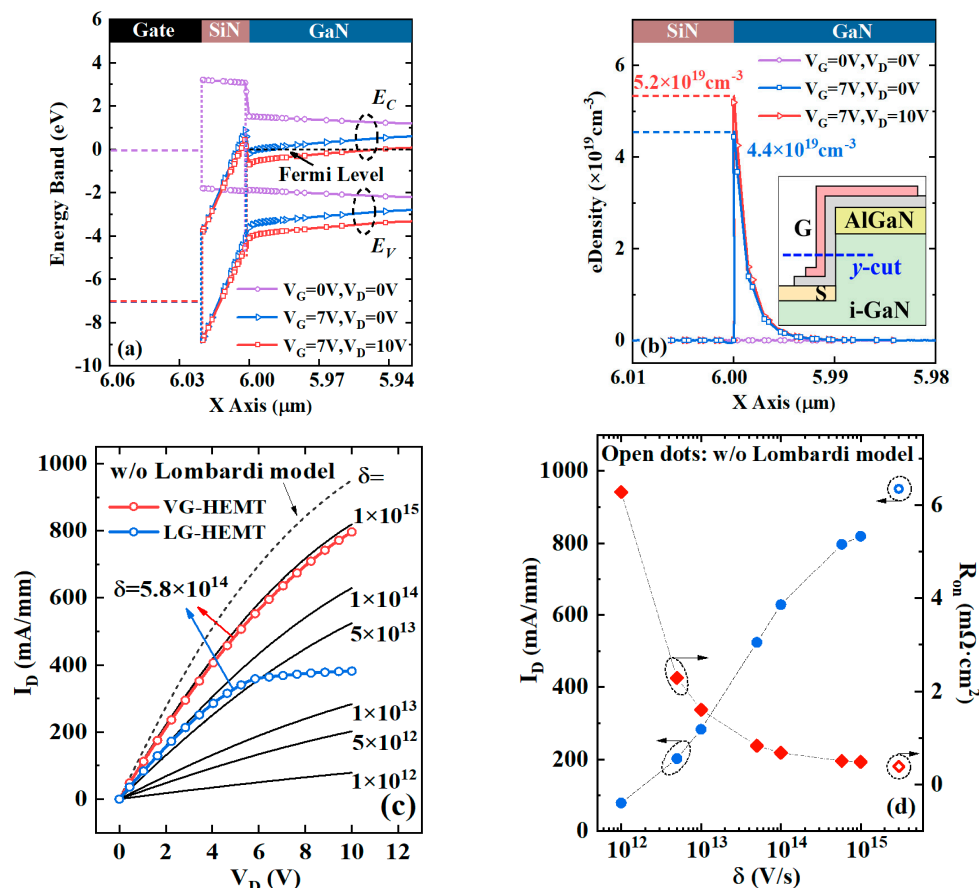


Figure 4. (a) Energy band and (b) electron concentration diagrams along the horizontal direction across the gate channel (“y-cut” marked in the inset). (c) I_D – V_D curves affected by different δ values using Lombardi model in the VG-HEMT. (d) Dependences of saturated current density and R_{on} on δ values.

Figure 5 shows the 2-D equipotential lines and electric field distributions near the gate region in the same dimension range of the devices at $V_D = 400$ V and $V_G = 0$ V. With comparison, the VG-HEMT exhibits more uniform electrostatic potential and electric field distribution at the gate corner toward the drain side where usually the electrical breakdown occurs due to the high field crowding. Without an additional field plate design which requires more lithography and metal deposition steps, the VG-HEMT can get a reduced electric field at the gate corner owing to the presence of a “natural field plate”, forming by the overlap of gate metal at the etched edge. The depletion region in the vertical gate structure is expanded to a wider range to sustain a higher voltage and hence reduce the device leakage current. Figure 5c,d show the detailed data plots of the electrostatic potential and electric field extracted in the 2DEG channel of both devices. The electrostatic potential increases more smoothly at the gate corner of the VG-HEMT, while a large field crowding happens in the LG-HEMT. The peak of electric field in the VG-HEMT is reduced to 26% compared with the LG-HEMT case, which indicates a better stability and reliability in the VG-HEMT. Furthermore, an improved breakdown voltage can be hopefully achieved when the length of the “natural field plate” is further optimized. To avoid a punch-through breakdown in the VG-HEMT due to the off-state conducting path formed in GaN bulk, carbon doping in GaN bulk to reduce the background carrier density and design of drain-side field plate will be considered and demonstrated in future work.

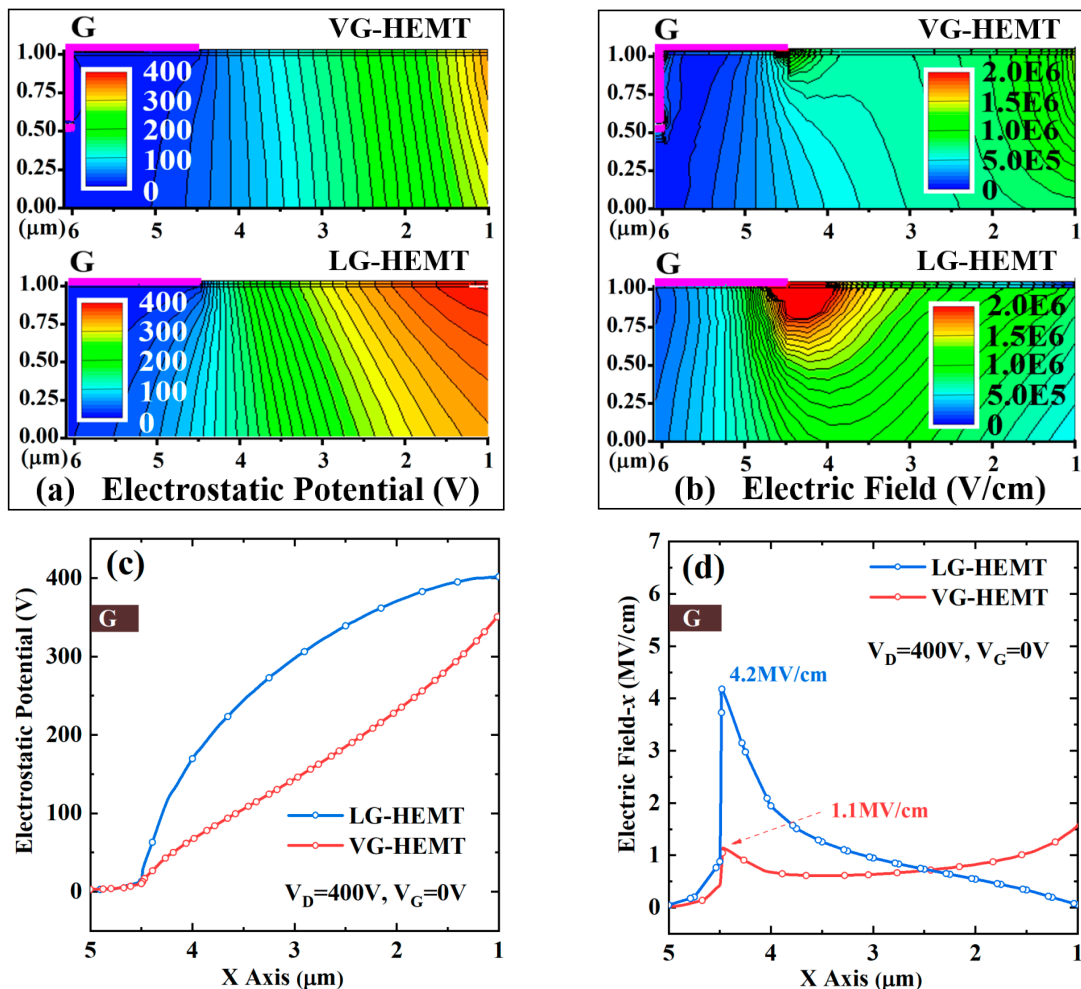


Figure 5. Comparisons of (a) electrostatic potential and (b) electric field distribution profiles between the LG-HEMT and VG-HEMT devices. The data plots in (c) and (d) are derived along the two-dimensional electron gas (2DEG) channel within 5 nm near the gate toward the drain side.

5. Conclusion

In summary, an innovative scheme with a vertical short gate structure in GaN-based HEMTs to realize normally-off operation is proposed and verified by TCAD simulations. The VG-HEMT exhibits a large V_{th} of 3.1 V and an improved output current density and R_{on} , which can greatly reduce the power loss of the device. Furthermore, the VG-HEMT displays a lower leakage current during the off state owing to the more uniform electric field distribution by reducing the peak electric field to 26% of the LG-HEMT case. The quantitative dependence of saturated current density and R_{on} on the scattering factors in the trenched vertical gate channel was investigated in detail which concludes the benefit of the proposed short vertical gate VG-HEMT scheme. Although the fabrication process of the VG-HEMT might be complicated and time-consuming, the device structure is proposed for the first time and does have several advantages. More improved performances will be achieved and demonstrated in the following experiments.

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