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Improved MRD 4H-SiC MESFET with High Power Added Efficiency

Shunwei Zhu, Hujun Jia *, Xingyu Wang, Yuan Liang, Yibo Tong, Tao Li and Yintang Yang

School of Microelectronics, Xidian University, Xi'an 710071, China

* Correspondence: hjjia@mail.xidian.edu.cn; Tel.: +86-137-7212-6387

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Abstract: An improved multi-recessed double-recessed p-buffer layer 4H–SiC metal semiconductor field effect transistor (IMRD 4H-SiC MESFET) with high power added efficiency is proposed and studied by co-simulation of advanced design system (ADS) and technology computer aided design (TCAD) Sentaurus software in this paper. Based on multi-recessed double-recessed p-buffer layer 4H–SiC metal semiconductor field effect transistor (MRD 4H-SiC MESFET), the recessed area of MRD MESFET on both sides of the gate is optimized, the direct current (DC), radio frequency (RF) parameters and efficiency of the device is balanced, and the IMRD MESFET with a best power-added efficiency (PAE) is finally obtained. The results show that the PAE of the IMRD MESFET is 68.33%, which is 28.66% higher than the MRD MESFET, and DC and RF performance have not dropped significantly. Compared with the MRD MESFET, the IMRD MESFET has a broader prospect in the field of microwave radio frequency.

Keywords: 4H-SiC; MESFET; IMRD structure; power added efficiency

1. Introduction

Nowadays, as the device size continues to decrease, the process difficulty increases significantly, both the power consumption and non-ideal effects are significant. The first-generation semiconductor Si and other materials are close to their theoretical limits in performance, while 4H Silicon Carbide (4H-SiC) has a wide band gap (3.26 eV), high thermal conductivity (4.9 W/(cm·K)), high breakdown electric field (4 MV/cm) and low dielectric constant (9.7), high electron saturation drift speed (2.7×10^7 cm/s), and exhibits superior performance compared to 3C-SiC, 6H-SiC, Si, GaAs, and so on. Based on the excellent characteristics of 4H-SiC, 4H-SiC metal semiconductor field transistors (4H-SiC MESFETs) are expected to be applied to various semiconductor fields [1–3]. However, current research on 4H-SiC MESFET mainly includes breakdown voltage, saturation drain current, electron saturation drift speed, frequency characteristics etc. [4–10]. There are a variety of ways to improve device performance, such as the use of double-recessed gates [4], recessed buffers and diffusion regions [5,6], doping distribution modification [7,8], silicon-on-insulator (SOI) technology [9,10] and so on, which can significantly improve device performance. At the same time, there is little research on efficiency [11,12]. For non-conventional 4H-SiC-based FETs, the characteristics of the device can be studied using numerical simulations [13–17].

In this paper, we reported a 4H-SiC MESFET with improved multi-recessed double-recessed p-buffer layer (IMRD) structure. Traditional 4H-SiC MESFETs have been experimentally verified. Many experimental results have been reported so far [18,19], but they are all fixed structures, and the effect of structural parameters on the results has not been studied. Based on multi-recessed 4H–SiC MESFETs with double-recessed p-buffer layer (MRD 4H-SiC MESFET) [20], we adopt a new design method optimized by technology computer aided design (TCAD) simulation and verified in advanced design system (ADS) software. The IMRD MESFET has both the excellent performance of MRD MESFET and

better power-added efficiency (PAE) and provides a new idea for high-power operational amplifier design at the device level.

2. Device Structure and Description

Figure 1a,b are the cross-sectional views of the MRD MESFET and the IMRD MESFET, respectively. In Figure 1a, the MRD MESFET contains a high-purity semi-insulating substrate (SI-Substrate), a p-type buffer layer (P-Buffer), an n-type channel layer (N-Channel), and two doped n-type cap layers (Source and Drain), the Nickel Schottky gate has a work function of 5.1 eV. By high energy ion implantation and high temperature annealing processes, two recessed areas are formed on both sides of the gate. The main difference between the two devices is the recessed regions on both sides of the gate. The length and width on both sides are L_1 = 0.15 µm, L_2 = 0.2 µm, H_1 = 0.1 µm and H_2 = 0.1 µm, other parameters are shown in Table 1. In the optimized IMRD MESFET, L_1 = 0.5 µm, L_2 = 0.2 µm, H_1 = 0.15 µm and H_2 = 0.2 µm, and the other parameters are consistent with the MRD MESFET.

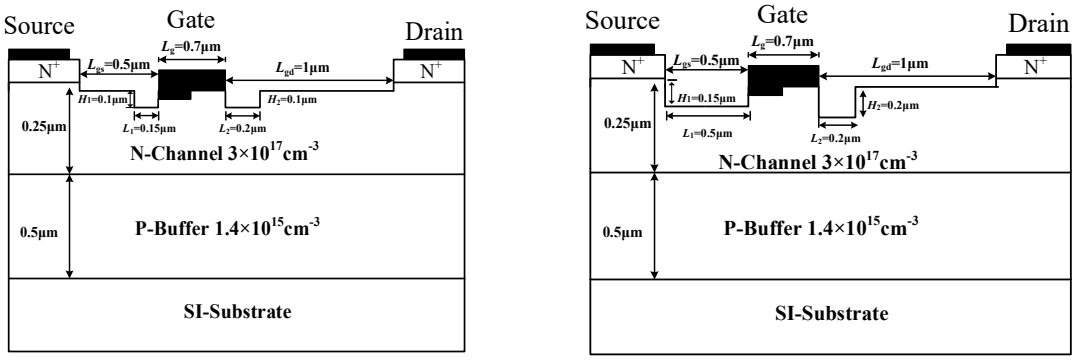

Figure 1. Schematic cross sections of the (**a**) MRD 4H-SiC metal semiconductor field effect transistor (MESFET), (**b**) improved multi-recessed double-recessed p-buffer layer (IMRD) 4H-SiC MESFET.

Table 1. Common parameters of the two structures.

Parameters	Values
P-Buffer Concentration	1.4×10^{15} cm^{-3}
N-Channel Concentration	3×10^{17} cm^{-3}
N-Cap layers Concentration	2×10^{19} cm^{-3}
L_{gs}	0.5 µm
L_{gd}	1.0 µm
L_s	0.5 µm
L_d	0.5 µm
L_g	0.7 µm
N-Channel Thickness	0.25 µm
P-Buffer Thickness	0.5 µm
Device Area (without SI-Substrate)	1 µm × 3.5 µm

The 2D TCAD simulator, Sentaurus is used in this paper. The simulation temperature is set to 300 K. A 5.1 eV Nickel Schottky gate work function is applied. The main model used in the simulation are Mobility (Enormal Doping Dep HighFieldsaturation (GradQuasiFermi)), Recombination (Auger SRH (DopingDep)), Incomplete Ionization, Effective Intrinsic and Density (BandGapNarrowing (OldSlotboom)) [21]. The interface state has a great impact on the device, in this paper, the gate of the two devices are formed by a metal-to-SiC contact to form a Schottky contact, so the gate does not have to consider the interface state. When the MESFET is passivated with a material such as Si_3N_4 or SiO_2, the performance is slightly degraded. When verifying the conventional 4H-SiC MESFET, Si_3N_4 was used as the passivation layer. When Si_3N_4 is used as the passivation layer, the device performance is

reduced by less than SiO_2 [22,23]. As a theoretical analysis, the influence of passivation on the device is not considered here. After obtaining the simulation results, the obtained model parameters are used in the ADS software to measure the PAE of the two devices. In the ADS simulation, the bias conditions of the device are shown in Figure 2. Direct current (DC) voltage Vg1 is −3.5 V, Vdd is 28 V, input power Pavs is 24 dBm, and frequency f is 1.2 GHz.

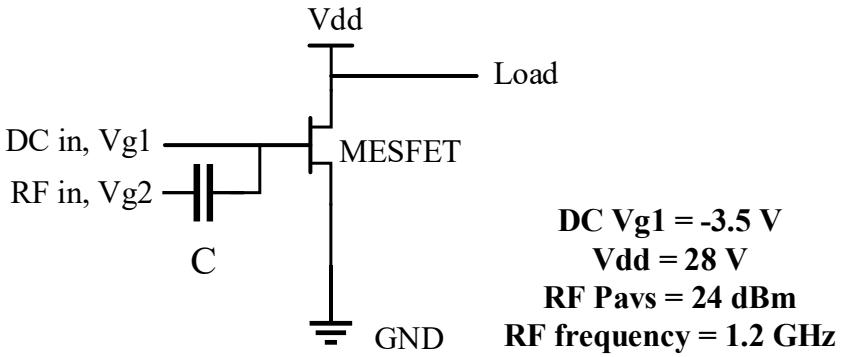

Figure 2. One Tone Load Pull Schematic for power-added efficiency (PAE) measurements.

3. Results and Discussion

3.1. Effect of the Length and Height of the Recessed Regions on the PAE

The effect of the length and height of the recessed regions on PAE is shown in Figure 3. When a parameter changes, the remaining parameters are the default values in Figure 1a. We can see in Figure 3a, when L_1 increases, PAE also increases. When L_1 reaches 0.5 μm, PAE reaches a maximum value; when L_2 is less than 0.1 μm, the PAE increases with L_2. When L_2 reaches 0.2 um, PAE reaches a maximum value. When L_2 is larger than 0.1 μm, PAE decreases with the increase of L_2. In Figure 3b, the trend of the effect of H_1 and H_2 on PAE agrees well. When H_1 and H_2 are less than 0.2 μm, PAE of H_1 and H_2 increase with the increase of H_1 and H_2. When H_1 and H_2 reach 0.2 μm, PAE of H_1 and H_2 reach the maximum value. When H_1 and H_2 are larger than 0.2 μm, PAE of H_1 and H_2 decrease as H_1 and H_2 increases.

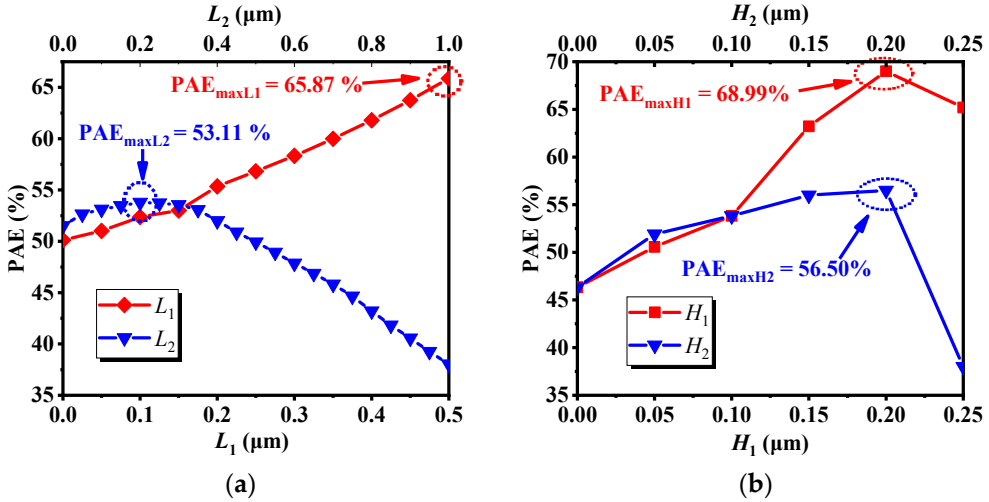

Figure 3. The effect of the (**a**) length and (**b**) height on PAE.

3.2. Optimized Results and Mechanism Discussion

Through further analysis of the results obtained in 3.1, we found that between L_1, L_2, H_1 and H_2 there is a relatively independent relationship. When L_2, H_1 and H_2 take different values, the trend of PAE with L_1 is almost the same as Figure 3a. The maximum value of PAE is found in L_1 = 0.5 μm.

In addition, for L_2, H_1 and H_2, the maximum value of PAE are found in L_2 = 0.2 µm, H_1 = 0.2 µm and H_2 = 0.2 µm. Based on the above results, L_1 = 0.5 µm, L_2 = 0.2 µm, H_1 = 0.2 µm and H_2 = 0.2 µm were selected as the optimal structural parameters, and the optimized device was obtained. The main parameters of the device are shown in Table 2. It can be seen from the table that although its saturated drain current I_{dsat} is too small, which is 35.2% lower than that of the MRD MESFET, and the DC characteristics are greatly weakened, its PAE reaches 70.85%, which is 33.40% higher than that of the MRD MESFET.

Table 2. Comparison of performance parameters of the two structures.

Parameters	MRD MESFET	IMRD MESFET
I_{dsat} (mA/mm)	358.97	233.02
g_m (mS/mm)	73.45	56.37
V_t (V)	−5.81	−6.89
C_{gs} (pF/mm)	0.128	0.13
C_{gd} (pF/mm)	0.39	0.02
Power-added efficiency (PAE) (%)	53.11	70.85

Figure 4 shows the effect of the length and height on I_{dsat}. It can be seen from Figure 4a that when L_1 = 0.5 µm and L_2 = 0.2 µm, the decline of I_{dsat} is small; In Figure 4b, it can be clearly seen that when H_1 is less than 0.15 µm, I_{dsat} decreases, but the value of decrease is not very large. When H_1 is greater than 0.15 µm, I_{dsat} drops sharply. Similarly, for H_2, when H_2 is less than 0.2 µm, the decrease of I_{dsat} is not large. When H_2 is larger than 0.2 µm, the decline of I_{dsat} is more obvious. The main cause of the weakening of the DC characteristics is that the thickness of the channel region becomes extremely thin, resulting in narrowing the channel of most electrons, and thus the DC characteristics are deteriorated. Based on the results above, L_1 = 0.5 µm, L_2 = 0.2 µm, H_1 = 0.15 µm and H_2 = 0.2 µm were selected as structural parameters, and the PAE was measured to be 68.33%. After optimization, the PAE of the IMRD MESFET is 28.66% higher than that of the MRD MESFET.

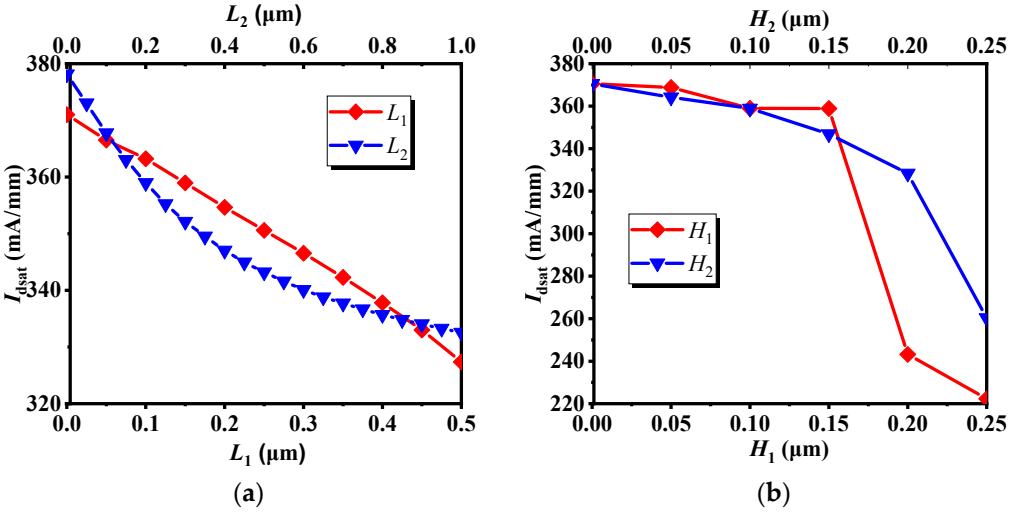

Figure 4. The effect of the (**a**) length and (**b**) height on I_{dsat}.

Figure 5 illustrates the effect of recessed region parameters (L & H) on V_t, Gm_{max}, C_{gs} and C_{gd}, the transconductance Gm_{max}, its physical meaning is the first-order partial conductance of the output drain current and the input voltage, C_{gs} is the gate-source capacitance, and C_{gd} is the gate-drain capacitance. In combination with Figure 3, it can be seen from Figure 5a,c,e that as L_1 increases, the threshold voltage V_t, the transconductance Gm_{max}, the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} decrease, but the PAE gradually increases; when L_2 increases, V_t increases first, then tends to be stationary, Gm_{max} gradually decreases, the change trend of C_{gd} and C_{gs} are about

the same. When L_2 is less than 0.1 μm, the changes of C_{gs} and C_{gd} are relatively stable. When L_2 is larger than 0.1 μm, C_{gs} and C_{gd} are gradually increased. Combined with Figures 3a and 5a,c,e, it can be found that the effects of C_{gs} and C_{gd} on PAE are obvious. It can be seen from the bias conditions of Figure 2 that C_{gs} and C_{gd} affect the input impedance and output impedance respectively, and the power consumed by the capacitor is proportional to the size of the capacitor. According to the definition of PAE, these two capacitors affect the input power and output power, so these two capacitors have a greater impact on the PAE. Similarly, in conjunction with Figure 3, it can be seen from Figure 5b,d,f that, when H_1 is less than 0.2 μm, as H_1 increases, V_t, Gm_{max}, C_{gs} and C_{gd} decrease, while PAE increases. When H_1 is larger than 0.2 μm, PAE decreases with H_1. For H_2, when H_2 increases gradually, V_t and Gm_{max} also decrease gradually, but when H_2 is less than 0.05 μm, C_{gs} and C_{gd} decrease with increasing H_2. When H_2 is greater than 0.05 μm, the change of C_{gs} and C_{gd} are relatively stable. When H_2 is less than 0.2 μm, PAE increases with the increase of H_2. When H_2 is greater than 0.2 μm, PAE decreases as H_2 increases. Combined with Figures 3b, 4b and 5b,d,f, although the capacitances C_{gs} and C_{gd} have a greater influence on PAE, as the H_2 increases, the conductive channel of the device still decreases. When the thickness of the conductive channel is less than 0.05 μm, the conductive channel is extremely thin, and its conductive properties are greatly weakened. At this time, both the AC signal and the DC signal will be greatly attenuated in the channel, resulting in a decrease in output power. Under the combined action of several factors, the PAE decreases as H_2 increases.

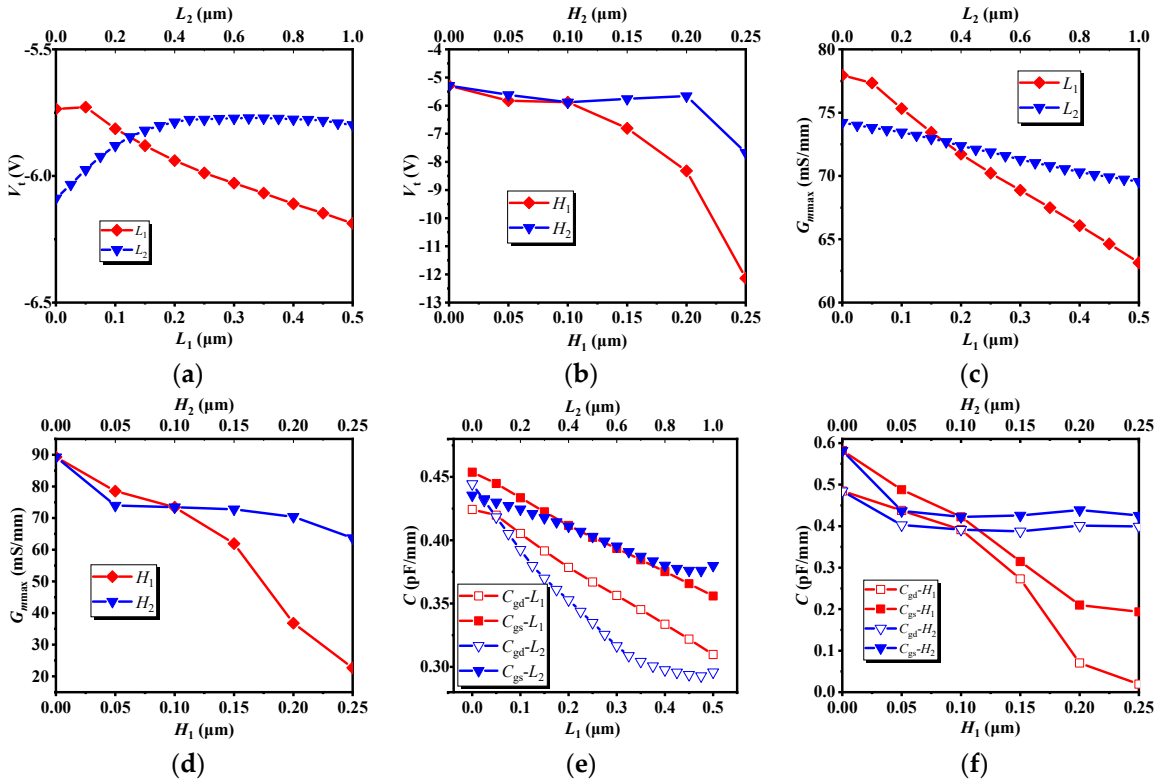

Figure 5. The effect of recessed region parameters on V_t, Gm_{max} and C_{gs}. (**a**) V_t-*L*. (**b**) V_t-*H*. (**c**) Gm_{max}-*L*. (**d**) Gm_{max}-*H*. (**e**) *C*-*L*. (**f**) *C*-*H*.

The power-added efficiency (PAE) is the difference in output and input power in place of radio frequency (RF) output power in the drain efficiency equation, which takes power gain G_p into account.

$$\mathrm{PAE} = \frac{P_{out} - P_{in}}{P_{dc}} = \eta_c\left(1 - \frac{1}{G_p}\right) \quad (1)$$

η_c is the drain efficiency and represents the ratio of output power to DC input power. In order to obtain a higher PAE, a larger power gain G_p is required. It can be seen from the equivalent circuit

diagram of the device, the size of the PAE is determined by these parameters together. For the threshold voltage V_t, only when the absolute value of V_t is reduced, can small voltage make the channel turn on. When the input voltage is constant, the smaller the absolute value of the threshold voltage is, the larger the channel current is, and the larger the output power P_{out} is, so that the PAE becomes larger. When Gm_{max} is reduced, its DC characteristic will also decrease. Since the input voltage is constant, the decrease of Gm_{max} causes the bias current I_d to decrease, so that the P_{dc} is reduced, according to the definition of PAE, the decrease of P_{dc} will cause the increase of PAE. The gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} have a greater influence on the PAE, in the equivalent circuit, C_{gs} and C_{gd} are in the input loop and output loop respectively. Because of the larger C_{gs} in the bias, the more AC input energy it consumes, the larger the C_{gd}, the smaller the AC output power of the load is. In addition, as the channel becomes thinner and thinner, it affects both the capacitance and the carrier's passage through the channel region. Although the PAE increases as the capacitance decreases, the extremely thin channel also makes the DC and AC characteristics affected seriously. From the analysis of 3.1–3.3, when the structural parameters of the device are changed, in order to obtain the optimal PAE, it is necessary to weigh the various parameters and find the optimal structural parameters on the premise that the other performance is guaranteed. Perhaps the above design process will sacrifice a small part of the performance, but the efficiency is greatly improved, achieving energy saving and emission reduction, which is very beneficial to the construction of green earth.

4. Conclusions

An improved MRD 4H-SiC MESFET with high power added efficiency is analyzed and studied by co-simulation of ADS and TCAD Sentaurus software in this paper. Based on MRD 4H-SiC MESFET, we optimize the MRD MESFET on both sides of the gate. In the recessed area, the DC, RF parameters and efficiency of the device are weighed, and the IMRD MESFET with the best PAE is finally obtained. The results show that the saturation drain current Idsat of the IMRD MESFET is 311 mA, the threshold voltage V_t is −6.99 V, the maximum transconductance Gm_{max} is 46.37 mS, the gate-source capacitance C_{gs} is 0.218 pF, and the gate-drain capacitance C_{gd} is 17.9 fF. The PAE is 68.33%, which is 28.66% higher than the MRD MESFET, and DC and RF performance have not dropped significantly. This paper proposes to lay a device-level theoretical basis and design method for further energy-efficient RF power amplifier.

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