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Improved DRUS 4H-SiC MESFET with High Power Added Efficiency

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Received: 22 November 2019; Accepted: 25 December 2019; Published: 27 December 2019

Abstract: A 4H-SiC metal semiconductor field effect transistor (MESFET) with layered doping and undoped space regions (LDUS-MESFET) is proposed and simulated by ADS and ISE-TCAD software in this paper. The structure (LDUS-MESFET) introduced layered doping under the lower gate of the channel, while optimizing the thickness of the undoped region. Compared with the double-recessed 4H-SiC MESFET with partly undoped space region (DRUS-MESFET), the power added efficiency of the LDUS-MESFET is increased by 85.8%, and the saturation current is increased by 27.4%. Although the breakdown voltage of the device has decreased, the decrease is within an acceptable range. Meanwhile, the LDUS-MESFET has a smaller gate-source capacitance and a large transconductance. Therefore, the LDUS-MESFET can better balance DC and AC characteristics and improve power added efficiency (PAE).

Keywords: 4H-SiC MESFET; simulation; power added efficiency (PAE)

1. Introduction

As a third-generation semiconductor, silicon carbide (SiC) has significant advantages in materials and devices, with high critical electrical field, high thermal conductivity, and high electron saturation velocity [1–3]. SiC based metal-semiconductor field-effect transistors (MESFETs) have become the key components for high-power, high-efficiency and high-frequency microwave applications because of their excellent properties. They offer wider bandwidth operation and lower system size than Si and GaAs based on MESFET technologies [4–7]. Based on those excellent performance, 4H-SiC MESFETs have broad application prospects in aerospace, satellite communications, and active phased array radars. Previously, the main research on SiC-MESFET was to balance the DC and AC characteristics and improve the output power density. With the idea of energy saving and emission reduction, high efficiency and low energy consumption have become the direction of device design. Thus, some improved structures have been reported for improving the power added efficiency. Such as a novel 4H-SiC MESFET with multi-recessed p-buffer layer for high energy-efficiency applications [8], an improved UU-MESFET with high power added efficiency [9], multi-recessed 4H–SiC metal semiconductor field effect transistor (MRD-MESFET) with high power added efficiency [10], an improved 4H-SiC MESFET with a partially low doped channel [11]. However, the trade-off between PAE and DC AC parameters is still a troublesome problem.

The DRUS-MESFET [12] is proposed to increase the breakdown voltage and improve the output power density of the device based on the double-recessed MESFET (DR-MESFET) [13]. But the saturation current and PAE of the device is low. Considering the saturation current and the power added efficiency, an improved double-recessed 4H-SiC MESFET with partly undoped space region

(LDUS-MESFET) is proposed and simulated. The new structure introduced layered doping under the lower gate and optimized the thickness of the undoped region. Using software ISE-TCAD and ADS to simulate the LDUS-MESFET, the DC and AC parameter values and power added efficiency of the device are obtained. By comparing with the DRUS-MESFET, it can be seen that the LDUS-MESFET is more in line with "green high efficiency, energy saving and emission reduction" thoughts.

2. Device Structure and Simulation Method and Fabrication Feasibility

2.1. Device Structure

Schematic cross-section of the DRUS-MESFET and the LDUS-MESFET are shown in Figure 1a,b, respectively. They both have a semi-insulating substrate, a p-type buffer layer, an n-type channel layer, and two highly doped n-type cap layers. The semi-insulating substrate is modeled as a compensation-doped (vanadium) semiconductor with a high concentration of deep level impurities [13]. Among them, the role of the p buffer layer is to reduce the influence of substrate defects on the active layer and improve noise performance and device gain [14]. Both of these structures have upper and lower gates, which control a thinner and a thicker part of the channel, respectively. The difference between the two structures is that the LDUS-MESFET has a layered doping under the lower gate, wherein the upper layer region has a doping thickness of H_1 = 0.05 μm and a concentration of 6×10^{17} cm^{-3} (to have a meaningful comparison, the lower layer region doping concentration of the LDUS-MESFET based on the DRUS-MESFET is also set at 3×10^{17} cm^{-3}), and the thickness of the undoped space region (US) is optimized for high efficiency. The optimization result is H_2 = 0.05 μm. The other parameters of the two structures are shown in Table 1.

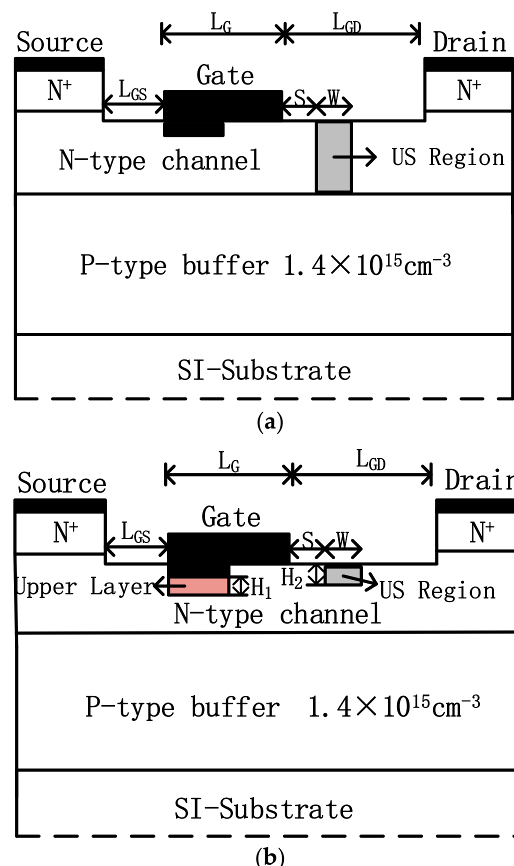

Figure 1. Schematic cross sections of the (**a**) double-recessed 4H-SiC MESFET with partly undoped space region (DRUS-MESFET), (**b**) 4H-SiC metal semiconductor field effect transistor with layered doping and undoped space regions (LDUS-MESFET).

Table 1. Common parameters of the two structures

Parameters	Values
P-Buffer Concentration	1.4×10^{15} cm^{-3}
N-Channel Concentration	3×10^{17} cm^{-3}
N-Cap layers Concentration	2×10^{19} cm^{-3}
Upper layer Concentration	6×10^{17} cm^{-3}
N-Cap layers Thickness	0.2 µm
N-Channel Thickness	0.25 µm
P-Buffer Thickness	0.5 µm
Recess gate Thickness	0.05 µm
Recess gate Width	0.35 µm
W	0.3 µm
S	0.2 µm
L_{gs}	0.5 µm
L_{gd}	1.0 µm
L_s	0.5 µm
L_d	0.5 µm
L_g	0.7 µm
H_1	0.05 µm
H_2	0.05 µm

2.2. Simulation Method

Two dimensional numerical device characteristics are realized with ISE-TCAD. The simulator is calibrated with experimental data in the micrometer regime [15], and the agreement between experimental data and simulation results is obtained as shown in Figure 2. In order to accurately simulate the electrical characteristics of the 4H-SiC MESFET device structure, the main physical models used are mobility (Enormal, Doping Dep, High Field saturation (GradQuasiFermi)), recombination (Auger, SRH (DopingDep)), incomplete ionization, effective intrinsic density (Band Gap Narrowing (OldSlotboom)). The DC and AC parameters of the device are obtained by ISE-TCAD simulation, and these parameters are input into the ADS software to simulate the power added efficiency of the device. In the ADS simulation, the model used is EE-FET3, an empirical analytical nonlinear model used to fit the electrical properties of MESFETs. And the working bias conditions were set as follows: V_{gs} was −3.5 V, V_{ds} was 28 V, RF was 1.2 GHz and input power Pavs was 24 dBm.

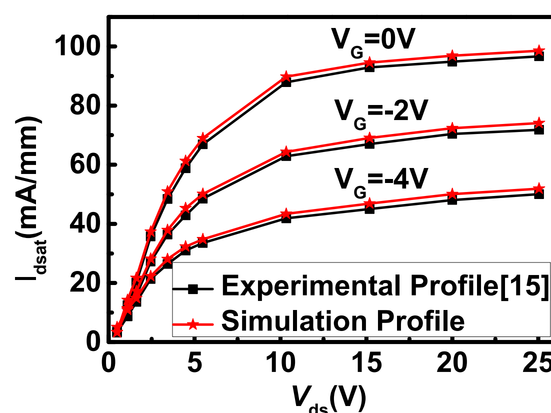

Figure 2. Comparison of experimental data and simulation data on output current.

2.3. Fabrication Feasibility

The LDUS-MESFET can be fabricated using the same procedures as reported in [16]. It is worth noting that the doping concentration of 6×10^{17} cm^{-3} region under the lower gate can be formed by ion implantation and activation process. Through high temperature and multi-energy ion implantation with phosphorous, and activation of the implanted ions can be achieved by inductively heating at a

desired time and temperature in an Ar atmosphere [17]. The formation of undoped space region is formed by high energy ion implantation of deep level vanadium and high temperature annealing (the resistivity of the US region is 2×10^6–7.6×10^6 Ω·cm).

The recessed gate area of the transistors can be fabricated as reported in [16] as follows: First, a thermal oxide layer is deposited on top of the channel, the thermal oxide layer is etched through the position of the recessed area and continues to be etched into the interior of the channel to form a recessed area having a thickness of 0.05 µm. Second, Nickel with a work function of 5.1 eV was deposited on the recessed area to form a Schottky contact.

3. Results and Discussion

3.1. The Effect of the Doping Concentration (N_d) and Thickness(H_1) of the Upper Layer Region on the Device Parameters

The effect of the thickness and doping concentration of the upper layer region on DC and AC parameters are shown in Figure 3. It can be seen from the Figure 3a that as the doping concentration increases, the absolute value of the threshold voltage increases significantly. When H_1 is less than 0.05 µm, the absolute value of Threshold voltage (V_t) is gradually decreasing with the increase of H_1. Because there is a longitudinal concentration gradient in the channel. The concentration gradient produces a longitudinal electric field that weakens the pinch-off voltage, which results in a decrease in the absolute value of the threshold voltage. When H_1 is greater than 0.05 µm, the absolute value of V_t is increasing with the increase of H_1. Because as the doping thickness increases, the number of electrons in the channel increases, causing the threshold voltage to drift negatively. At H_1 = 0.05 µm, the absolute value of the threshold voltage has a minimum value. In Figure 3b. As the doping concentration increases, Gate-source capacitance (C_{gs}) also increases. At the same time, C_{gs} shows an upward trend with the increase of H_1. In Figure 3c,d, as the doping concentration increases, the saturation current (I_{dsat}) increases significantly, and the breakdown voltage decreases. When H_1 rises from 0 to 0.05 µm, the saturation current increases rapidly. When H_1 increases from 0.05 µm, the rising trend of saturation current becomes slow.

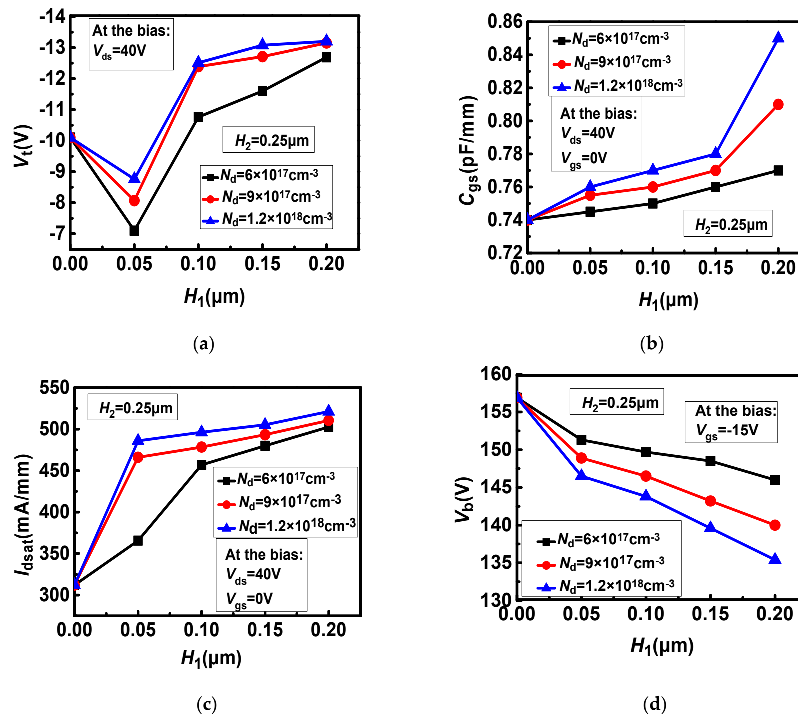

Figure 3. The effect of H_1 and N_d on the device parameters: (**a**) V_t–N_d and H_1, (**b**) C_{gs}–N_d and H_1, (**c**) I_{dsat}–N_d and H_1, (**d**) V_b–N_d and H_1.

3.2. The Effect of the Doping Concentration (N_d) and Thickness of the Upper Layer Region (H_1) on PAE

The influences of the doping concentration and thickness of upper layer region on PAE is shown in Figure 4. It can be seen from the figure that as the doping concentration of the upper layer region increases, the PAE significantly decreases. When the thickness of the upper layer region is less than 0.05 μm, the PAE increases with the increase of H_1. When H_1 is greater than 0.05 μm, the PAE decreases with the increase of H_1. When the thickness of the upper layer region is 0.05 μm, the PAE reaches a maximum value.

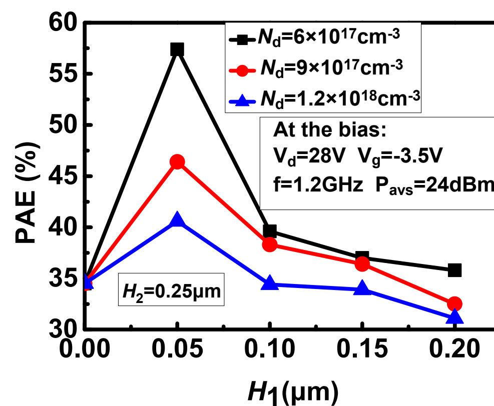

Figure 4. The effects of N_d and H_1 on the PAE.

3.3. Optimization of the Undoped Region Thickness (H_2)

Based on the thickness and doping concentration of the upper layer region determined above, the thickness of the undoped region is optimized to obtain better power added efficiency and DC AC parameters. The effect of the thickness of the undoped region on the DC, AC parameters and PAE of the device is shown in Figure 5. In Figure 5a. We can see that as H_2 increases, the absolute value of the threshold voltage gradually decreases. At the same time, when H_2 is less than 0.05 μm, the breakdown voltage increases as H_2 increases, when H_2 is greater than 0.05 μm, the breakdown voltage shows a basically constant trend with the increase of H_2. In Figure 5b. As H_2 increases, the transconductance (g_m) shows a decreasing trend. When H_2 is less than 0.15 μm, the transconductance decline trend is more gradual. When H_2 is greater than 0.15 μm, the transconductance decreases sharply as H_2 increases. When H_2 increases, C_{gs} shows an upward trend. In Figure 5c. As H_2 increases, the saturation current shows a linear decline. When H_2 is less than 0.05 μm, the PAE increases as H_2 increases, and when H_2 is greater than 0.05 μm, the PAE decreases as H_2 increases. The PAE reaches the maximum at H_2 = 0.05 μm.

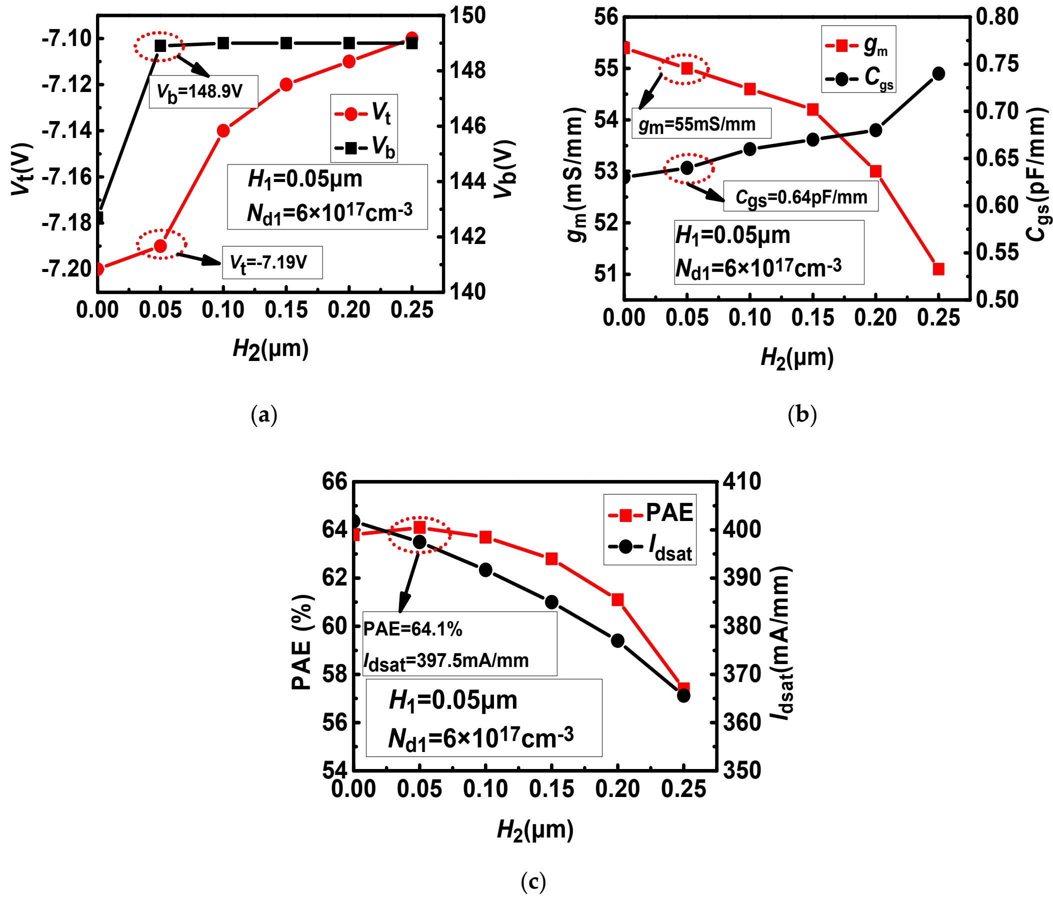

Figure 5. The effect of H_2 on the device parameters: (**a**) V_t, V_b–H_2, (**b**) g_m, C_{gs}–H_2, (**c**) PAE, I_{dsat}–H_2.

3.4. Mechanism to Improve Device Parameters

Through the analysis of Figures 4 and 5, it can be acquired that when H_1 = 0.05 µm, H_2 = 0.05 µm, $N_d = 6 \times 10^{17}$ cm^{-3}, the power added efficiency reaches the maximum value of 64.1%. It can be seen from Equation (1) that PAE is an efficiency that considers DC and AC parameters [18]. The parameters V_t, g_m and C_{gs} simulated above have an impact on power added efficiency. The larger the absolute value of the threshold voltage of the device, the more difficult it is that the gate voltage is pinched off, which results in higher DC power consumption and smaller PAE. As the maximum transconductance of the device increases, the power-added efficiency of the device tends to decrease linearly. This is because when the device transconductance increases, it means that the ability of the gate to control the current is increased, and the channel resistance is increased, resulting in an increase in the DC power consumption of the device, and the power added efficiency of the device is reduced. The larger the C_{gs}, the greater the energy lost when charging and discharging the capacitor, resulting in a larger P_{dc}, which in turn reduces the PAE. The LDUS-MESFET has a smaller threshold voltage and capacitance than the DRUS-MESFET. Although the transconductance is improved compared with the DRUS-MESFET, it can be seen from the simulation that the threshold voltage V_t and C_{gs} have a greater influence on the PAE than the transconductance. So the PAE of the LDUS-MESFET is 85.8% higher than the DRUS-MESFET.

$$\text{PAE} = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{dc}}} \tag{1}$$

where P_{out} is output power, P_{in} is input power and P_{dc} is DC power.

It can be seen from Table 2 that the saturation current is increased by 27.4% compared with the DRUS-MESFET. It can be obtained from Equation (2) that the saturation current is proportional to the amount of charge in the channel and the effective thickness of the channel [14]. Heavy doping

under the lower gate and reducing the thickness of the undoped region in the channel increase the saturation current. The breakdown occurs at the edge of the gate near the drain side, and the thickness of the undoped region has a certain influence on the breakdown voltage. So the LDUS-MESFET has a lower breakdown voltage than the DRUS-MESFET. But the range of reduction is acceptable. The transconductance reflects the gate voltage's ability to control the channel current of the device. The partly high doping under the lower gate makes the transconductance of the LDUS-MESFET larger than the DRUS-MESFET. The threshold voltage refers to the gate-source voltage when the channel is pinched off. Since the LDUS-MESFET has a longitudinal concentration gradient in the channel, the concentration gradient produces a longitudinal electric field that weakens the pinch-off voltage, which results in a decrease in the absolute value of the threshold voltage. So the LDUS-MESFET has a smaller threshold voltage than the DRUS-MESFET. Compared with the DRUS-MESFET, the LDUS-MESFET has a reduced thickness of the undoped region near the drain side of the gate. So that the drain side depletion layer can be expanded and the source side expansion is reduced, this makes C_{gs} decrease.

$$I_{dsat} = Q(x)v(x) = Zb(x)qn(x)v(x) \tag{2}$$

where Z is the channel width, $b(x)$ is the effective depth of the channel, q is the electron charge, $n(x)$ is the electron density, and $v(x)$ is the electron velocity.

Table 2. Comparison of performance parameters of the two structures.

Parameters	DRUS-MESFET	LDUS-MESFET
I_{dsat} (mA/mm)	312	397.5
V_b (V)	156.9	148.9
g_m (mS/mm)	43.8	55
V_t (V)	−10.1	−7.19
C_{gs} (pF/mm)	0.74	0.64
PAE (%)	34.5	64.1

4. Conclusions

An improved DRUS 4H-SiC MESFET with layered doping under lower gate is proposed and simulated in this paper to increase the PAE of the device. On the basis of the DRUS-MESFET, in order to maximize the power added efficiency, an upper layer region of 0.05 μm thick is introduced under the lower gate, and the thickness of the partly undoped region of the DRUS-MESFET was optimized. The structure achieves a PAE of 64.1%, which is 85.8% larger than the DRUS-MESFET. In addition, the LDUS-MESFET has a certain improve in saturation current, threshold voltage, transconductance, and gate-source capacitance. Although the breakdown voltage is reduced, the drop value is within the acceptable range. Overall, the LDUS-MESFET has wider application in the radio frequency direction.

Author Contributions: Data curation, X.W.; formal analysis, T.Z.; project administration, H.J.; writing—original draft, Y.L.; writing—review and editing, T.L., Y.T., S.Z., and Y.Y. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the National Natural Science Foundation of China (NSFC) under Grant No. 61671343.

Conflicts of Interest: The authors declare no conflict of interest.

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