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Analysis of Current Variation with Work Function Variation in L-Shaped Tunnel-Field Effect Transistor

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Abstract: In this paper, an investigation is performed to analyze the L-shaped tunnel field-effect transistor (TFET) depending on a gate work function variation (WFV) with help of technology computer-aided design (TCAD) simulation. Depending on the gate voltage, the three variations occur in transfer curves. The first one is the on-state current (I_{ON}) variation, the second one is the hump current (I_{HUMP}) variation, and the last one is ambipolar current (I_{AMB}) variation. According to the simulation results, the I_{ON} variation is sensitive depending on the size of the tunneling region and could be reduced by increasing the tunneling region. However, the I_{HUMP} and I_{AMB} variations are relatively irrelevant to the size of the tunneling region. In order to analyze the cause of this difference, we investigated the band-to-band tunneling (BTBT) rate according to WFV cases. The results show that when I_{ON} is formed in L-shaped TFET, the BTBT rate relies on the WFV in the whole region of the gate because the tunnel barrier is formed in the entire area where the source and the gate meet. On the other hand, when the I_{HUMP} and I_{AMB} are formed in L-shaped TFET, the BTBT rate relies on the WFV in the edge of the gate.

Keywords: tunnel field-effect transistor (TFET); L-shaped TFET; high-κ/metal gate (HKMG); work-function variation (WFV); band-to-band tunneling; on-state current (I_{ON}) variation; hump current (I_{HUMP}) variation; ambipolar current (I_{AMB}) variation

1. Introduction

Recently, an L-shaped tunnel field-effect transistor (TFET) has attracted the attention of a lot of researchers as a substitutional device for a metal-oxide-semiconductor (MOS) field-effect transistor (MOSFET) [1–6]. The L-shaped TFET features a mesa-shaped structure and an intrinsic Si region located between the source and gate dielectric layer to obtain high band-to-band tunneling (BTBT) due to the larger tunneling area than the planar TFET. The L-shaped TFET has remarkable advantages for low-voltage operation due to its small subthreshold swing (S) of less than 60 mV/dec, low-level OFF-state current (I_{OFF}) and high complementary MOS (CMOS) compatibility [7–10]. Based on the characteristics, the electrical performance of the L-shaped TFET can be more improved dramatically by applying the high-κ/metal gate (HKMG) technology [11–13]. Thus, it is expected that the L-shaped TFET is applicable to the real industry. However, the application of HKMG brings a work-function (WF) variation (WFV) issue due to the non-uniformity of metal gate grains in orientation depending

on the fabrication processes [14–17]. Therefore, in order to apply the TFET to the real application, the WFV in TFET should be investigated. Although there are several studies about the WFV effects on TFET, they have some common issues. The mentioned papers have focused on variation in electrical characteristics (e.g., threshold voltages (V_T) and ON-state current (I_{ON})) in general structures (e.g., planar, fin, nanowire) and have not proposed the improvement of WFV in TFET [14–18].

This paper aims to study the effects of WFV in L-shaped TFET with the help of technology computer-aided design (TCAD) simulation. The L-shaped TFET is expected to improve the WFV due to the large tunneling area. Because the WFV has been studied, we know that the channel area and the WFV have a high correlation [19,20]. The contents of this paper are as follows. In Section II, the structure and dimension of the studied L-shaped TFET are explained. The WFV induced by the grain of the metal gate is set reflecting the actual gate physical properties. In Section III, the quantitative analysis is performed by confirming the location of metal grains and BTBT rate to monitor the variation of I_{ON}, hump current (I_{HUMP}) and ambipolar current (I_{AMB}) of the L-shaped TFET.

2. Device Structure

The structure of L-shaped TFET for WFV analysis is shown in Figure 1a. It features that thin intrinsic Si is deposited to restrict tunnel width for enhancing BTBT. All of the source, drain and channel materials consist of Si. The body thickness (T_B) of 20 nm, the lateral channel length (L_{ch}) of 50 nm, vertical tunneling thickness (L_{tun}) of 6 nm and the SiO_2 gate oxide thickness (T_{OX}) of 1 nm are applied. p-type body doping (N_B) of 1×10^{17} cm^{-3} is set. Then, both Si source and drain doping concentrations (N_S, N_D) are set as 1×10^{20} cm^{-3} with opposite doping types Boron and Arsenic. For confirming the effect for the area of the tunneling barrier, the source height (H_S) is varied from 10 nm to 50 nm. The gate area is split into 10 nm × 10 nm units considering the grain size of TiN and it is assumed to be an identical square shape [21]. In the real fabrication process, the sputtered TiN is mainly crystallized in <200> (60%) and in <111> (40%) which correspond to 4.6-eV and 4.4-eV WFs, respectively [19,22]. In order to compare with planar TFET as a control group, the planar TFET has the same parameter for W, T_B, L_{ch}, N_S, N_D and N_B (Figure 1b). All the specifications are summarized in Table 1.

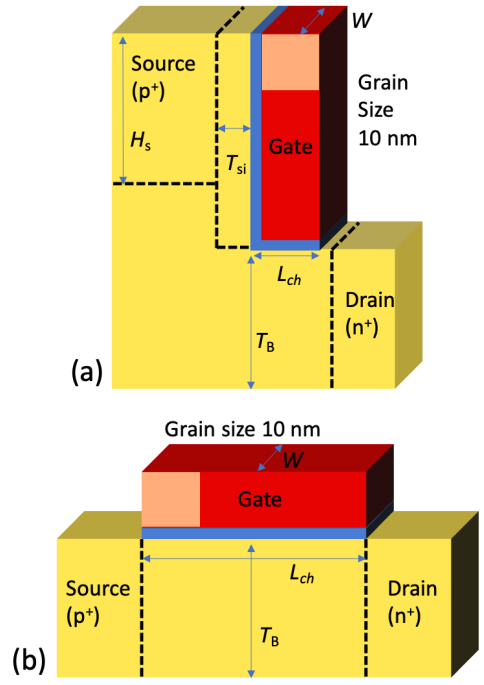

Figure 1. Schematic diagram of (**a**) the L-shaped tunnel field-effect transistor (TFET) and (**b**) the planar TFET. The L-shaped TFET features a vertical- band-to-band tunneling (BTBT) (parallel to the gate-field direction) in the intrinsic Si layer.

Table 1. Device parameters of devices used for technology computer-aided design (TCAD) simulation.

Parameters	Value	
Device	L-shaped TFET	Planar TFET
Source doping concentration (N_S)	10^{20} cm^{-3} (p-type)	
Drain doping concentration (N_D)	10^{20} cm^{-3} (n-type)	
Body doping concentration (N_B)	10^{17} cm^{-3} (p-type)	
Channel length (L_{ch})	50 nm	
Channel width (W)	30 nm	
Metal grain size	10 nm	
Intrinsic layer thickness (T_{Si})	6 nm	none
Gate oxide thickness (T_{OX})	1 nm	
Drain voltage (V_D)	1.0 V	
Source height (H_S)	varied	

The characteristics of the L-shaped TFET is simulated by the Synopsys Sentaurus^{TM}. The Shockley–Read–Hall (SRH) and dynamic nonlocal BTBT model are used for accurate characteristics [23,24]. The dynamic nonlocal BTBT model is essential to examine lateral- and vertical-BTBT in the L-shaped TFET, since it can dynamically determine and calculate all tunneling paths based on the energy band profile [3,25–27]. In detail, the BTBT model calibrated with experimental results [28]. The BTBT generation rate per unit volume (G) defined as

$$G = A\left(\frac{F}{F_0}\right)^P \exp\left(-\frac{B}{F}\right) \quad (1)$$

in the uniform electric field limit where F_0 = 1 V/m and P = 2.5 for indirect tunneling [29]. The prefactor (A) and the exponential factor (B) are Kane parameters while the F is electric field [30,31]. The extracted A and B parameters of the BTBT model in Si TFET are 4×10^{14} cm^{-1}s^{-1} and 9.9×10^{6} V/cm, respectively. Additionally, modified local density approximation (MLDA) is used for including quantum phenomena [32,33]. The MLDA model is needed to calculate the confined carrier distributions, especially inside the ultra-thin intrinsic Si tunnel region in which BTBT occurs. All the models are summarized in Table 2.

Table 2. Models in TCAD simulation.

Definition	Model
Bandgap narrowing	Old slot boom
Fermi Statistic	Fermi
Phonon scattering	Constant mobility
Multi-valley for quantum confinement	MLDA
SRH recombination	SRH/TAT
Nonlocal BTBT	Band to Band
WFV	4.6/4.4 eV (60%/40%) (Random generation)

3. Results and Discussion

Figure 2a shows the transfer characteristics of the planar TFET and L-shaped TFET with various source heights (H_S) at 1.0 V of drain voltages (V_{DS}). In each case of H_S, the 30 samples are simulated, and each sample contains randomly generated TiN grains in the gate. The I_{ON} of the L-shaped TFET increases as the H_S increases. The result shows that the L-shaped TFET can improve the weak drivability of I_{ON}, which is a weakness of TFET. In addition, the average S (S_{avg}), defined as the average inverse slope of the transfer curve while I_D changes from 10^{-15} μA/μm to 10^{-11} μA/μm, is shown from 35 to 45 mV/decade for the L-shaped TFET which means that the L-shaped TFET suggests possible applications for the low power operation [34,35]. In transfer curves, we measure three regions: I_{ON}, I_{HUMP} and I_{AMB} variations. Each variation extracted the difference between the maximum and

minimum values of the V_{GS} values represented by each sample when the I_{ON}, I_{HUMP} and I_{AMB} are formed. Firstly, the I_{ON} variation is investigated. The variation of I_{ON} is extracted from Figure 2a at 10^{-9} A/μm of drain current (I_D). For the I_{ON} variation, it is found that the greater the H_S value, the smaller the I_{ON} variation and the I_{ON} variation of the L-shaped TFET could be reduced compared with that of the planar TFET (Figure 2b). For the planar TFET, the tunnel barrier that determines the current, is formed only in the area adjacent to the source and channel [14,36]. This means that the I_{ON} variation in planar TFET relies on the WFV in areas adjacent to the source, not on the whole area of the gate. However, for the L-shaped TFET, the tunneling area affected by the WFV is relatively wider than that of the planar TFET because the tunnel barrier is formed in the entire area where the source and gate meet [1]. Figure 3a shows a sample produced by a random WFV. Inside the gate, 4.4 eV and 4.6 eV grains are placed. Based on this sample, the vertical-BTBT generated in the source area can be found to be high where the grain of 4.4 eV is located (Figure 3b). In other words, when the tunnel barrier has a large area, the BTBT rate can have an average effect.

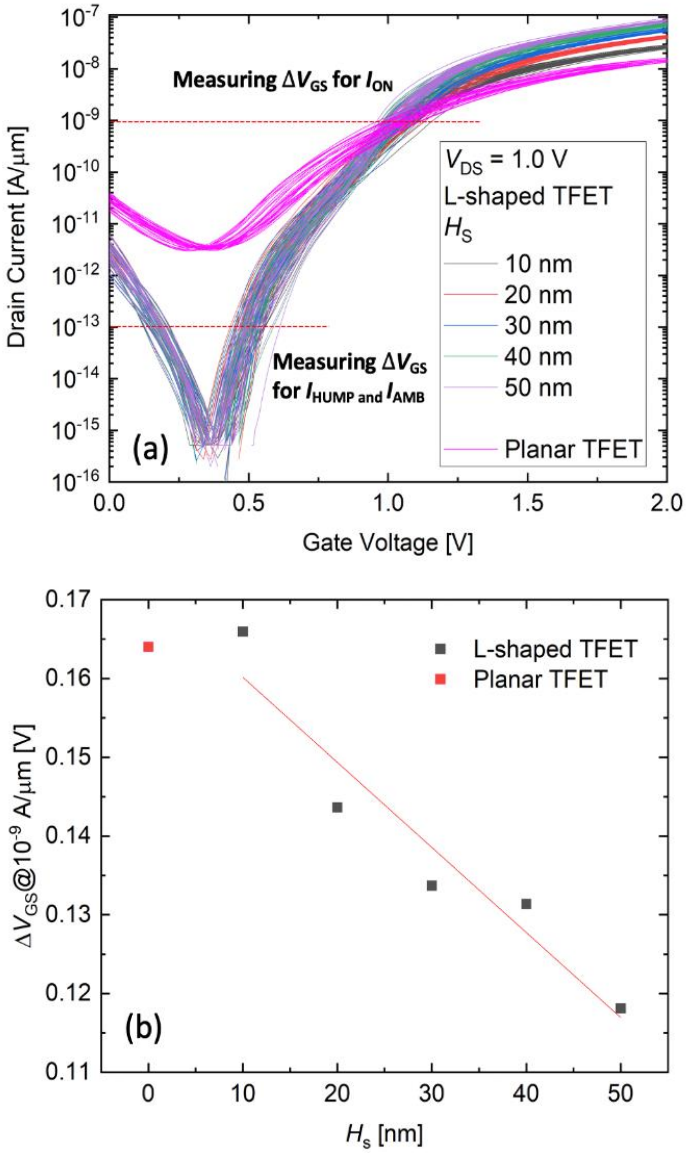

Figure 2. (**a**) Transfer curves of the L-shaped TFET. In each case of H_S, 30 random samples for WFV are generated. (**b**) Dependency on H_S and I_{ON} variation.

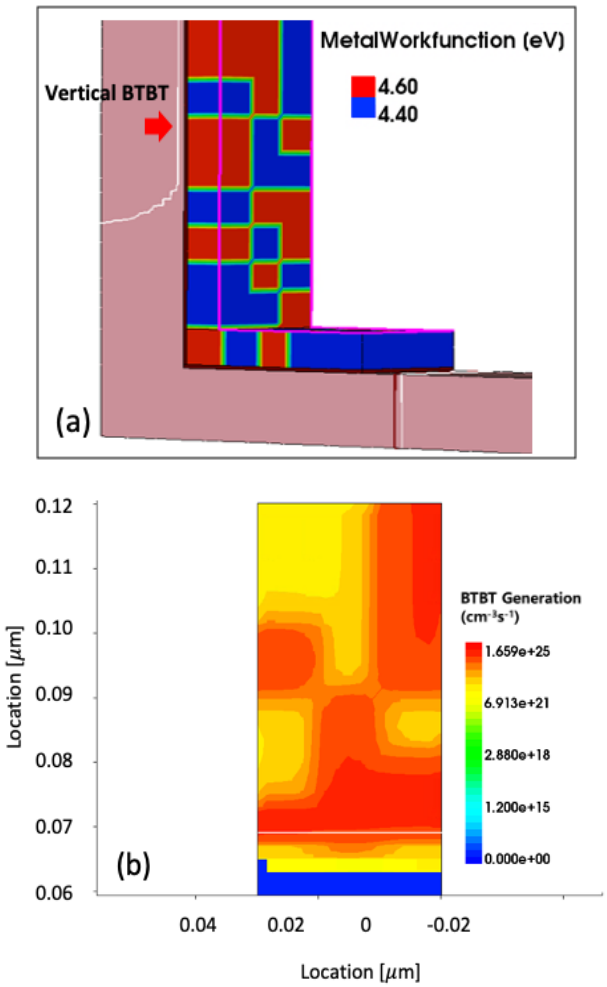

Figure 3. (**a**) TiN-grains distribution in gate area (**b**) BTBT rate on source region. The vertical-BTBT generated in the source area can be found to be high.

Next, the I_{HUMP} variation is investigated. For I_{HUMP}, as reported in the previous papers, the L-shaped TFET has vertical-BTBT and lateral-BTBT [37–39]. The lateral-BTBT is formed at low gate bias (V_{GS}) due to low V_T, resulting in a hump phenomenon. As shown in Figure 4a, the variation of I_{HUMP} is extracted from Figure 2a at 10^{-13} A/μm of I_D and it shows similar variations regardless of the change in the H_S value. To confirm this, we investigate two cases where the hump effect is high and low (Figure 4b). In the transfer curves, the two samples have almost the same I_{ON} values, while the samples have different I_{HUMP} values. For the sample with a high hump effect shown in Figure 4c, a high BTBT occurs mainly at the edge of the source area (Figure 4e). On the contrary, for the sample with a low hump effect shown in Figure 4d, a low BTBT is confirmed (Figure 4f). Specifically, the lateral-BTBT is measured highly where 4.4 eV grain is located in the source edge region, which causes a hump effect. As a result, the hump phenomenon is not related to the intrinsic Si area because tunneling occurs only at the edge of the source region.

Finally, the variation of the I_{AMB} is investigated. As shown in Figure 5a, the variation of I_{AMB} is extracted from Figure 2a at 10^{-13} A/μm of I_D. For I_{AMB} variation, little dependency on the L-shaped TFET is shown with H_S values. To confirm this, we investigate two cases where the hump effect is high and low (Figure 5b). In the transfer curves, it shows almost the same current in all regions except the I_{AMB}. As a result of confirming the high and low I_{AMB} samples (Figure 5c,d), it can be found that the BTBT occurs mainly in the edge of the drain at the gate, where there is a 4.6 eV grain (Figure 5e, Figure 5f).

In conclusion, the L-shaped TFET could be a solution to reduce I_{ON} variation for WFV in TFET. However, the WFV reduction effect is not seen on whole electrical performance, especially for the I_{HUMP} and I_{AMB}. These parameters are only affected by the edge region of the gate. Thus, for the real application of the L-shaped TFET, the WFV improvement should proceed through simultaneous applications of gate underlap technology that can reduce I_{AMB} and the dual WF gate, reducing the I_{HUMP} [25,40,41].

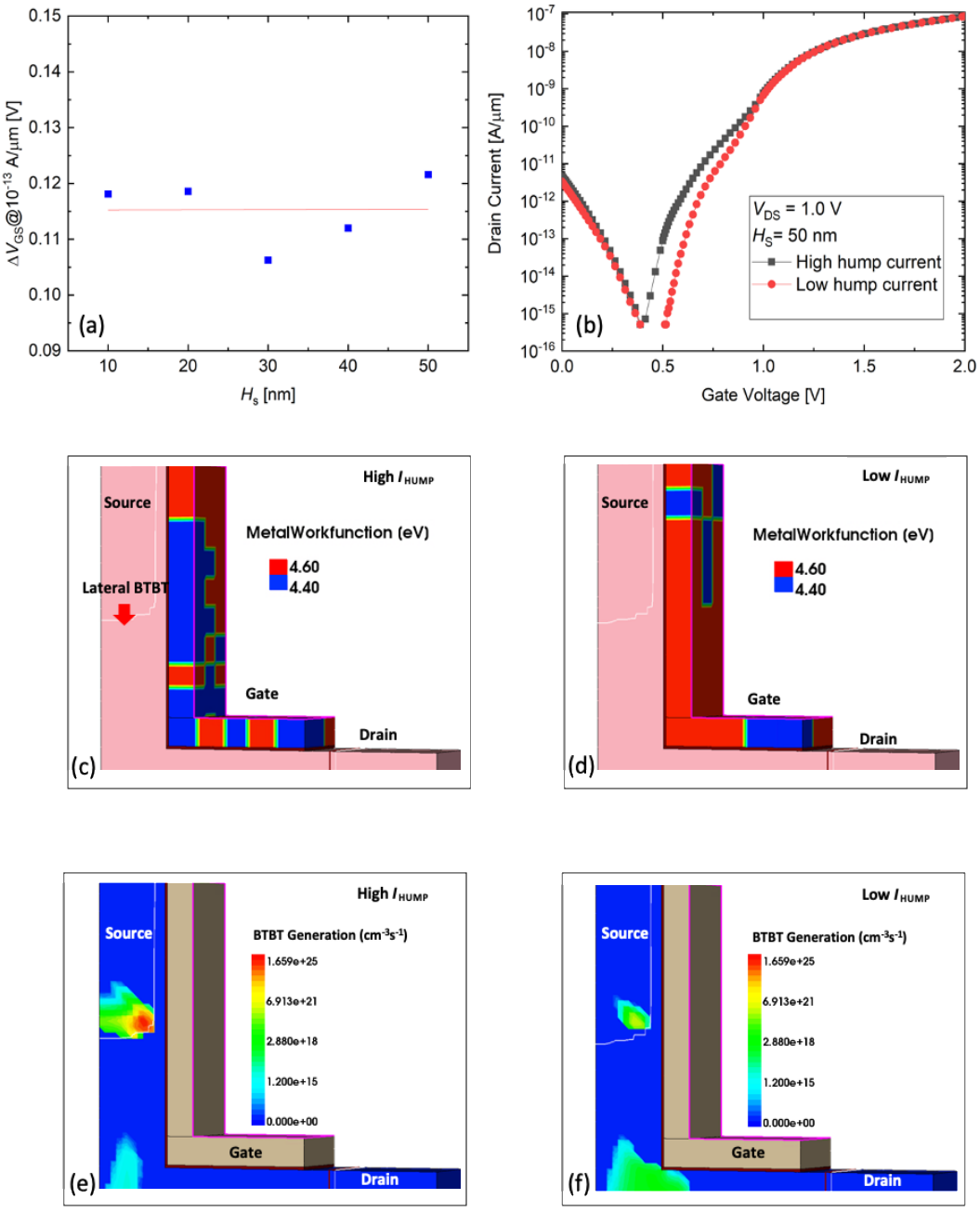

Figure 4. (**a**) I_{HUMP} variation dependency on H_S. (**b**) Transfer characteristics with high and low I_{HUMP}. TiN-grains distribution in gate area for (**c**) high I_{HUMP} sample and (**d**) low I_{HUMP} sample. BTBT rate for (**e**) high I_{HUMP} sample and (**f**) low I_{HUMP} sample.

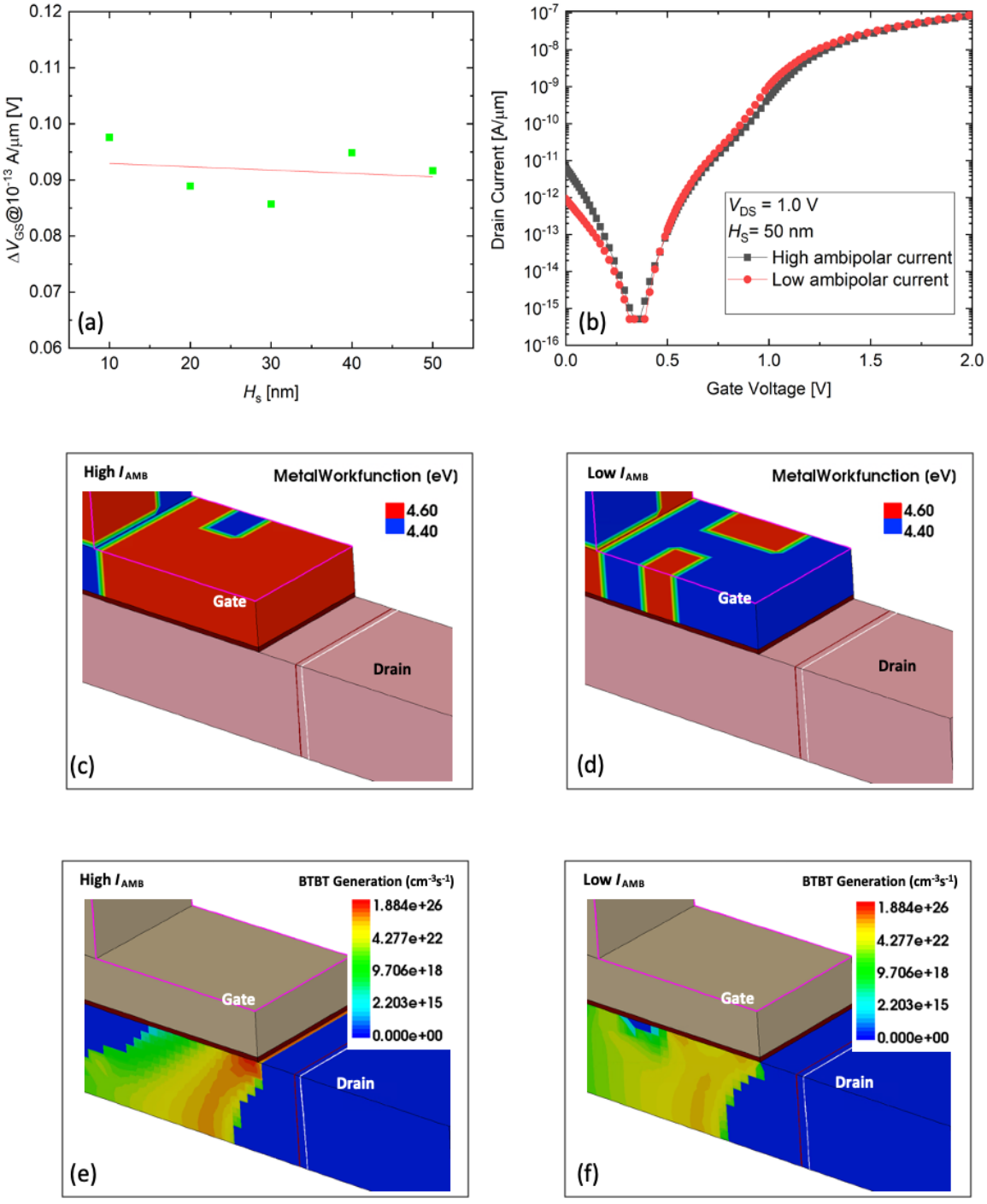

Figure 5. (**a**) I_{AMB} variation dependency on H_S. (**b**) Transfer curves with high and low I_{AMB}. TiN-grains distribution in gate area for (**c**) high I_{AMB} sample and (**d**) low I_{HUMP} sample. BTBT rate for (**e**) high I_{HUMP} sample and (**f**) low I_{AMB} sample.

4. Conclusions

In this paper, the L-shaped TFET is investigated for WFV. We investigate all the variations divided into I_{ON}, I_{HUMP}, I_{AMB} and study each variation. The improved results are shown for WFV in the L-shaped TFET versus the planar TFET because the L-shaped TFET uses the wide tunnel barrier region. Based on these results, it was confirmed that increasing the tunnel area in the TFET device can be a method to decrease WFV. Therefore, the I_{ON} variation could be reduced by an increase in the

tunneling region. However, the I_{HUMP} and I_{AMB} variations are relatively irrelevant to the size of the tunneling region.

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