



Article

# Research on Total Ionizing Dose Effect and Reinforcement of SOI-TFET

Chen Chong, Hongxia Liu \* , Shulong Wang \*  and Xiaocong Wu

Key Laboratory for Wide-Band Gap Semiconductor Materials and Devices of Education, The School of Microelectronics, Xidian University, Xi'an 710071, China; 18829029042@163.com (C.C.); m13720759895@163.com (X.W.)

\* Correspondence: hxliu@mail.xidian.edu.cn (H.L.); slwang@xidian.edu.cn (S.W.); Tel.: +86-029-88204085 (H.L.)

**Abstract:** Since the oxide/source overlap structure can improve the tunneling probability and on-state current of tunneling field effect transistor (TFET) devices, and the silicon-on-insulator (SOI) structure has the effect of resisting the single event effect, SOI-TFET with the oxide/source overlap structure is a device with development potential. The total ionizing dose (TID) effect on SOI-TFET was studied by discussing the switching ratio, band–band tunneling rate, threshold voltage, sub-threshold swing and bipolar effect of the device under different doses of irradiation. At the same time, simulations prove that selecting the proper thickness of the buried oxide (BOX) layer can effectively reduce the influence of the TID effect. This provides a way of direction and method for research on the irradiation effects on the device in the future.

**Keywords:** silicon-on-insulator (SOI); total ionizing dose (TID); tunneling field effect transistor (TFET)



**Citation:** Chong, C.; Liu, H.; Wang, S.; Wu, X. Research on Total Ionizing Dose Effect and Reinforcement of SOI-TFET. *Micromachines* **2021**, *12*, 1232. <https://doi.org/10.3390/mi12101232>

Academic Editor: Bassem Salem

Received: 23 September 2021

Accepted: 8 October 2021

Published: 10 October 2021

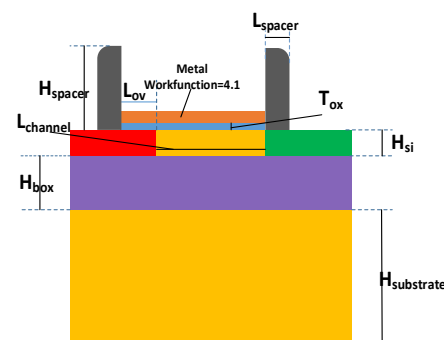
**Publisher's Note:** MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.



**Copyright:** © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

## 1. Introduction

With the development of integrated circuits, the characteristic size of devices is decreasing. TFET has become one of the potential new devices in the field of low voltage and low power consumption circuits because of its low subthreshold swing, high current switching ratio and low subthreshold leakage [1–5]. However, there are few studies on the radiation resistance of TFET devices [6–9]. This paper focuses on the TID effect in SOI-TFET with oxide/source overlap, the structure of the device is described in Figure 1. The gate of the device overlaps the oxide and the source can increase the on-state current [10–12], while the SOI structure can eliminate the latch-up effect and reduce parasitic capacitance [13–16]. It is found that the current switch ratio and subthreshold swing of the device deteriorates while threshold voltage has a slight drop, but it is not too sensitive after irradiation. The bipolar effect of TFET will be repressed to some degree by radiation, however, the greater the negative voltage of gate, the less the inhibition of radiation on bipolar effect. In addition, the optimal thickness of the buried oxide (BOX) layer is either 20 or 120 nm, where the device has the strongest resistance to the total ionizing dose effects.



**Figure 1.** Cross-sectional view of SOI-TFET.

## 2. Analysis of Total Dose Effect Mechanism

### 2.1. The Generation of Trapped Charge in the Oxide Layer

When some oxide layers in the device, such as the gate oxide layer, the buried oxide layer of the SOI structure, and the field oxygen isolation layer, are irradiated, a large number of electron-hole pairs will be generated inside. When there is an electric field inside the oxide layer, electrons and the hole will move in the opposite direction under the action of the electric field. Since the mobility of electrons is much greater than that of the holes, the electrons will be swept out of the oxide layer in the order of ps. The formula for the total amount of holes generated by irradiation in the oxide layer is as Equation (1):

$$N_h = f(E_{ox})g_0t_{ox}D \quad (1)$$

where  $E_{ox}$  is the electric field intensity in the oxide layer, and  $g_0$  is the density of electron-hole pairs generated under a unit irradiation dose, which is a material-related parameter. Generally speaking, the average energy required to generate a pair of electron-hole pairs is 3 times the material forbidden bandwidth.  $t_{ox}$  is the thickness of the oxide layer, and  $D$  is the radiation dose, for which the unit is generally rad (material).

### 2.2. The Generation of Trapped Charge in the Interface State

In addition to introducing trapped charges in the oxide layer, irradiation also introduces interface states at the Si/SiO<sub>2</sub> interface. At the Si/SiO<sub>2</sub> interface in the semiconductor, although the interface still maintains the continuity of the crystal lattice, the surface tension of the Si-H and Si-O bonds are very high due to the different lattice constants of the two materials. Irradiation will catalyze the rupture of these bonds, leading to the destruction of the periodic potential field of the lattice at the interface. The destruction of the periodic potential field can be equivalent to superimposing a new fixed potential field on the original periodic potential field. The energy level of the charged center of this electrostatic field is located in the center of the band gap, which is the interface state.

## 3. Methods

### 3.1. Physical Model

The Sentaurus software used in this paper is a computer-aided simulation tool specially under the Synopsys company for device simulation. First, make the device structure in the SDE module, and then add the required physical model in the Sdevice module. For TFET devices, the source region is heavily doped and the condition of  $E - E_F \gg k_0T$  cannot be met, so the Fermi distribution is adopted. The activation statement in Sdevice is: Physics {Fermi}. In TFET devices, mobility requires additional consideration of ionized impurity scattering models ( $\mu_{dop}$ ), interface scattering models ( $\mu_{InterSc}$ ), and high field velocity saturation models ( $\mu_F$ ). The Shockley–Read–Hall (SRH) composite in indirect composite mode is the main composite method used in TFET devices. Moreover, the presence of interface states at the interface of the semiconductor will introduce additional recombination effects, so the surface SRH recombination model needs to be considered. The non-local band-to-band (BTBT) model treats the electric field at each point in the tunnel path as a variable, which is more realistic. Therefore, the non-local BTBT model was adopted.

In this paper, the influence of TID radiation effect on SOI-FDSOI was studied by adding the radiation and interface trap models. The way to add the radiation model is to add the following statement in the physics module of Sdevice:

```
Radiation (DoseRate = @DoseRate@ DoseTime = (@initialTime@,@finalTime@) DoseT-Sigma = @DoseTSigma@)
```

The unit of DoseRate is rad/s, which represents the dose rate of the irradiated device; DoseTime specifies the time range during which the device is exposed to a certain dose rate environment; DoseTSigma (unit: s): can be combined with DoseTime to specify the Gauss of the radiation exposure and the standard deviation of the rise and fall. The generation of

electron-hole pairs due to radiation is an electric field-dependent process and is modeled as follows:

$$G_r = g_0 D Y(E) \quad (2)$$

$$Y(E) = \left( \frac{E + E_0}{E + E_1} \right)^m \quad (3)$$

where the default value of  $g_0$  is  $7.6 \times 10^{12} \text{ rad}^{-1} \cdot \text{cm}^{-3}$ , which represents the number of electron-hole pairs generated after a unit volume of the target is irradiated with a dose of 1 rad,  $D$  is the radiation dose,  $Y(E)$  is the electric field-related hole generation rate function,  $G_r$  is the number of holes that have not undergone initial recombination,  $E$  is the electric field parameter in V/cm, and  $E_0$ ,  $E_1$  and  $m$  are constants with sizes of 0.1 V/cm,  $1.35 \times 10^6$  V/cm, and 0.9, respectively.

### 3.2. Device Model

The device model built in Sentaurus (computer-aided simulation software) is shown in Figure 1, and the model parameters of the device are shown in Table 1. The substrate, source, drain and channel are all made of silicon. BOX is  $\text{SiO}_2$ , and the gate oxide layer uses high-K gate dielectric  $\text{HfO}_2$ . The side wall is  $\text{Si}_3\text{N}_4$ .

**Table 1.** Device parameters used for the simulation.

Parameter Name	Symbol	Value	Unit
Channel length	$L_{\text{channel}}$	45	nm
Gate oxide thickness	$T_{\text{ox}}$	2	nm
Silicon film thickness	$H_{\text{Si}}$	10	nm
BOX thickness	$H_{\text{box}}$	20	nm
Substrate thickness	$H_{\text{substrate}}$	50	nm
Metal work function	$\Phi_{\text{M}}$	4.17	eV
Channel doping	Boron	$1 \times 10^{16}$	$\text{cm}^{-3}$
Substrate doping	Boron	$1 \times 10^{16}$	$\text{cm}^{-3}$
Spacer height	$H_{\text{spacer}}$	20	nm
Spacer length	$L_{\text{spacer}}$	2	nm
Gate source overlap length	$L_{\text{ov}}$	6	nm

## 4. Results and Discussion

In order to study the influence of the TID effect on the performance parameters of the device, this section adopts the method of adding a fixed charge for simulation analysis. The idea of the simulation is to quantify the effect of fixed charge and interface state trap charge caused by irradiation in the BOX layer on the performance of the device, which is equivalent to the density of interface state trap charge. This is achieved by adding the following statement in the command file of Sdevice:

```
Physics (RegionInterface = "R.box/R.channel")
{Charge (Uniform Conc=@Conc@e12)}
```

The effect of positive charge with interface density of  $2.93 \times 10^{12} \text{ cm}^{-2}$  on the device is equivalent to that of a 300 krad ( $\text{SiO}_2$ ) dose  $\gamma$ -ray radiating device, and the effect of a positive fixed charge with interface density of  $3.26 \times 10^{12} \text{ cm}^{-2}$  is equivalent to that of 500 krad ( $\text{SiO}_2$ ) dose  $\gamma$ -ray radiating device, as described in some papers [17,18]. The interface densities of 0,  $3.5 \times 10^{10}$ ,  $50 \times 10^{10}$ ,  $100 \times 10^{10}$ ,  $150 \times 10^{10}$ ,  $200 \times 10^{10}$ ,  $250 \times 10^{10}$ ,  $300 \times 10^{10}$  and  $350 \times 10^{10} \text{ cm}^{-2}$  were selected to characterize the damage to the device irradiated by 0–500 krad ( $\text{SiO}_2$ ). The transfer characteristic curve obtained is shown in Figure 2. As the interface charge density increases, the curve shifts to the left, which means that the threshold voltage decreases. The reason is that as the positive charge density on the surface of the BOX is higher, the negative charge density of the channel (near the BOX) is higher, and the device is more likely to be turned on.

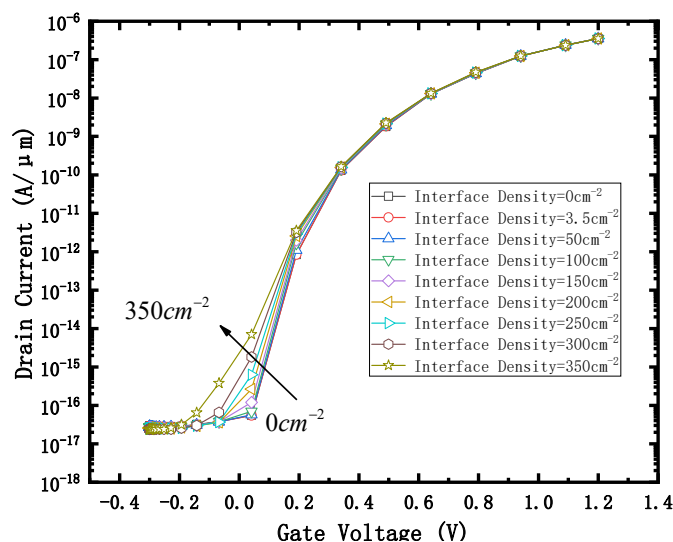


Figure 2. Id-Vg curve with different Interface Density.  $V_{\text{drain}} = 0.8 \text{ V}$ .

4.1. Current Switching Ratio  $I_{\text{on}}/I_{\text{off}}$  and eBTBT Generation

Figure 2 shows that when the gate voltage is 1.2 V, the on-state current of the device does not change significantly with the increase of the irradiation dose, while when the gate voltage is 0.2 V, the leakage current of the device increases significantly with the increase of irradiation dose. The  $I_{\text{on}}/I_{\text{off}}$  curve obtained is shown in Figure 3.

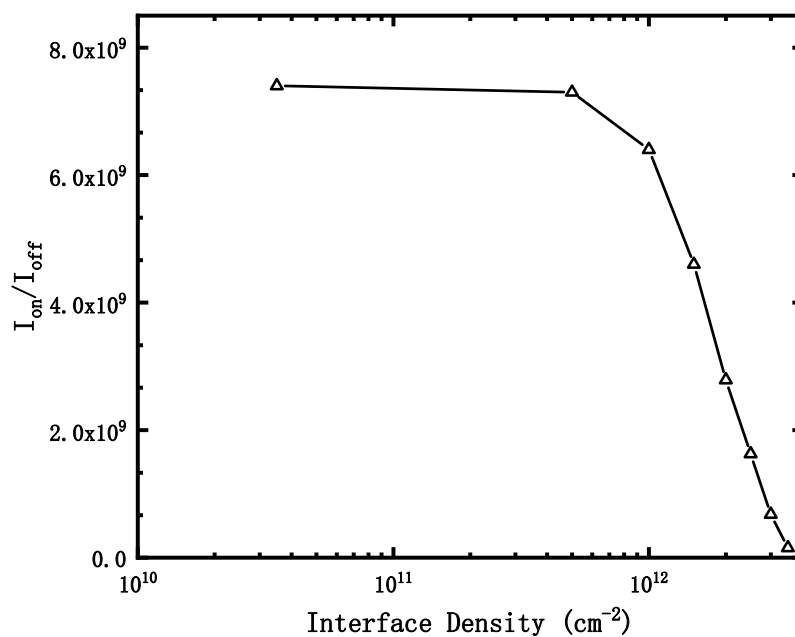


Figure 3.  $I_{\text{on}}/I_{\text{off}}$  with different interface density.

It can be seen that when the effect of irradiation on the device is equivalent to a positive charge of  $0.5 \times 10^{12} \text{ cm}^{-2}$  at the interface, the current switching ratio  $I_{\text{on}}/I_{\text{off}}$  of the device begins to decrease significantly. When the irradiation dose is 500 krad ( $\text{SiO}_2$ ) (corresponding to the positive charge density at the interface is about  $3.5 \times 10^{12} \text{ cm}^{-2}$ ), the  $I_{\text{on}}/I_{\text{off}}$  decreases to  $1.56 \times 10^8$ .

Compare the energy band diagrams at 0.2 V and 1.2 V (the tangent position is 2 nm upward at the interface between box layer and silicon film), as shown in Figure 4. It is found that:

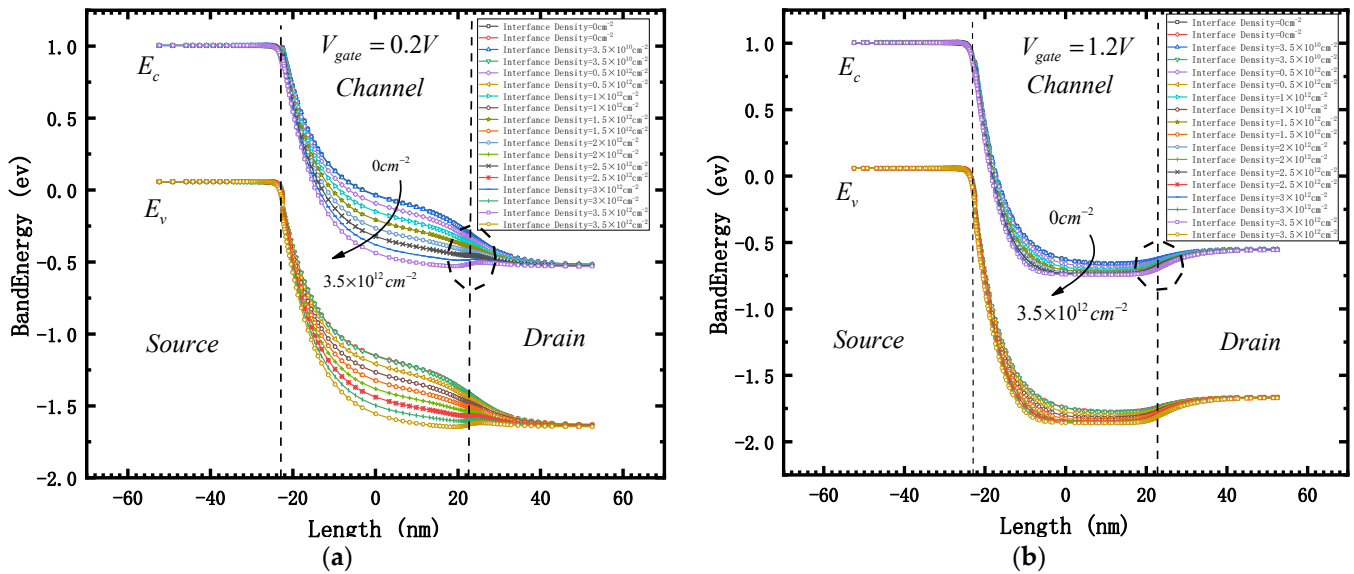


Figure 4. Band diagram with different interface density. (a) Gate voltage = 0.2 V; (b) gate voltage = 1.2 V.

(1) The smaller the gate voltage, the smaller the control ability of the gate to the channel and barrier region of the device, and the more obvious the influence of the electric field generated by the interface state on the channel and barrier region. Therefore, when the gate voltage is 0.2 V, the change range of the energy band is significantly higher than when the gate voltage is 1.2 V.

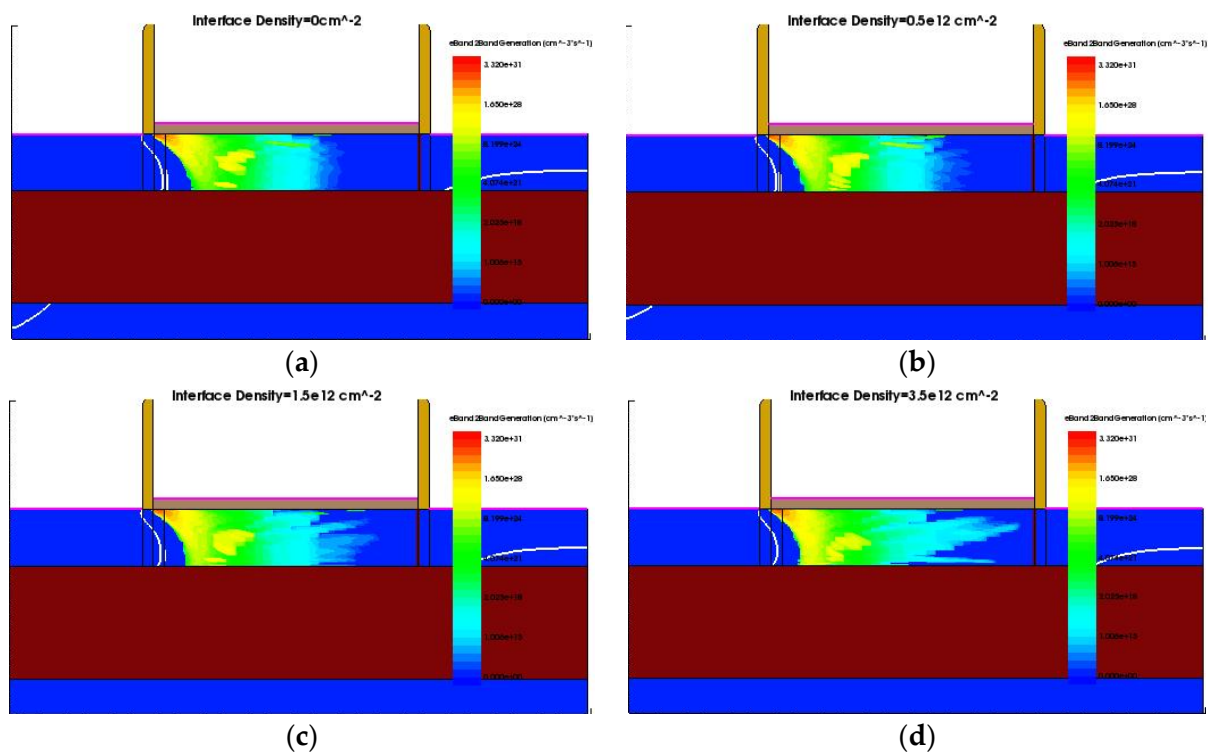
(2) The influence of interface states on the energy bands of the channel and barrier regions is much greater than that of source and drain regions. Therefore, the energy bands of source and drain regions do not change obviously, regardless of whether the gate voltage is 0.2 V or 1.2 V.

(3) The higher the concentration of interface state positive charge (the greater the total irradiation dose), the lower the energy band in the channel region. Therefore, when the gate voltage is 0.2 V, the device is at the off state. However, due to the irradiation, the channel energy band is reduced, the barrier difference  $\Delta\Phi$  between the two ends of the tunneling junction is increased, and the barrier width  $\lambda$  is decreased. These all result in increases to tunneling probability and the leakage current  $I_{off}$ .

(4) When the gate voltage is 1.2 V, the energy band in the channel region of the device is already very low due to the influence of the gate voltage. Therefore, with the increase of the irradiation dose, although the energy band in the channel region is further reduced, combined with the analysis of (2), it can be found that the influence of the barrier region (the circle part in the two figures) on the electron motion changes from the acceleration of electron drift when the gate voltage is 0.2 V to barrier blocking when is 1.2 V. Combined with the analysis of (1), it can be explained that when the gate voltage is 1.2 V, the on-state current ion of the device does not change greatly.

(5) Combined with the analysis of (3) and (4), we can explain why the current switching ratio  $I_{on}/I_{off}$  of the device decreases with the increase of irradiation dose.

The electron band-to-band tunneling probability (eBTBTGeneration) of the device ( $V_{gate} = 0.2 V$ ) with different interface density of states is shown in Figure 5:

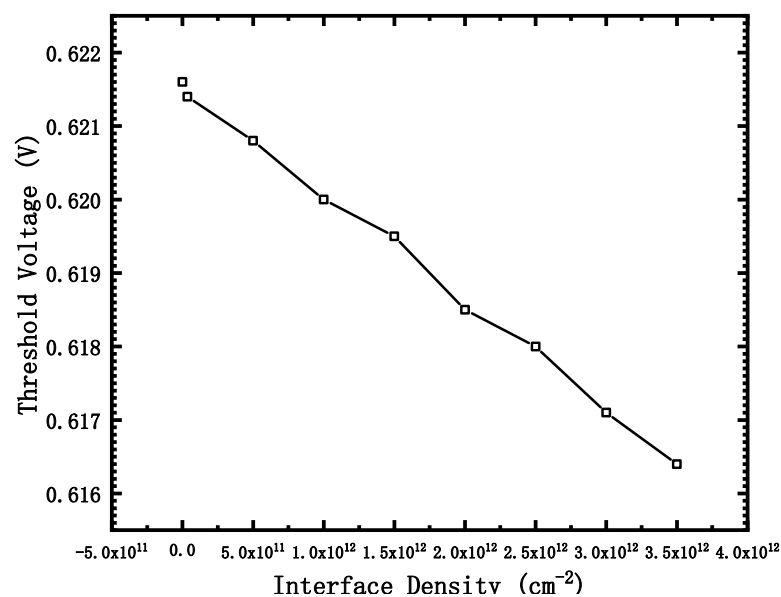


**Figure 5.** eBTBTGeneration profile. (a) Interface density =  $0 \text{ cm}^{-2}$ ; (b) interface density =  $0.5 \times 10^{12} \text{ cm}^{-2}$ ; (c) interface density =  $1.5 \times 10^{12} \text{ cm}^{-2}$ ; (d) interface density =  $3.5 \times 10^{12} \text{ cm}^{-2}$ .

It can be seen that, at the off state, the tunneling probability of the tunneling junction is indeed increasing, and the tunneling leakage current is positively correlated with the total radiation dose.

#### 4.2. Threshold Voltage and Subthreshold Swing

Taking the corresponding gate voltage when the current reaches  $10^{-8} \text{ A}/\mu\text{m}$  as the threshold voltage  $V_{th}$ , the variation curve of the threshold voltage with the dose is shown in Figure 6.



**Figure 6.** Threshold with different interface density.

It can be seen that the threshold voltage decreases with the increase of the irradiation dose. The threshold voltage can be understood as the gate voltage applied by the gate when the tunneling current reaches  $10^{-8}$  A/ $\mu\text{m}$ . We can know that the positive charge of the interface state will decrease the energy band of the channel region of the device, which is the same as the effect of gate voltage on the energy band in the channel region. Therefore, irradiation will take a portion of the gate voltage, making the device easier to turn on. However, the threshold voltage of the device is not seriously affected by the TID effects.

For TFET devices, the average subthreshold swing is generally used to measure the subthreshold swing characteristics, the formula is as follows Equation (4):

$$SS_{\text{ave}} = \frac{V_{g2} - V_{g1}}{\log_{10} I_2 - \log_{10} I_1} \quad (4)$$

The curve of average subthreshold swing extracted from the transfer characteristic curve (the gate voltage corresponding to leakage current of  $10^{-15}$  magnitude is  $V_{g1}$ , and the gate voltage corresponding to leakage current of  $10^{-10}$  magnitude is  $V_{g2}$ ) with the dose is shown in Figure 7.

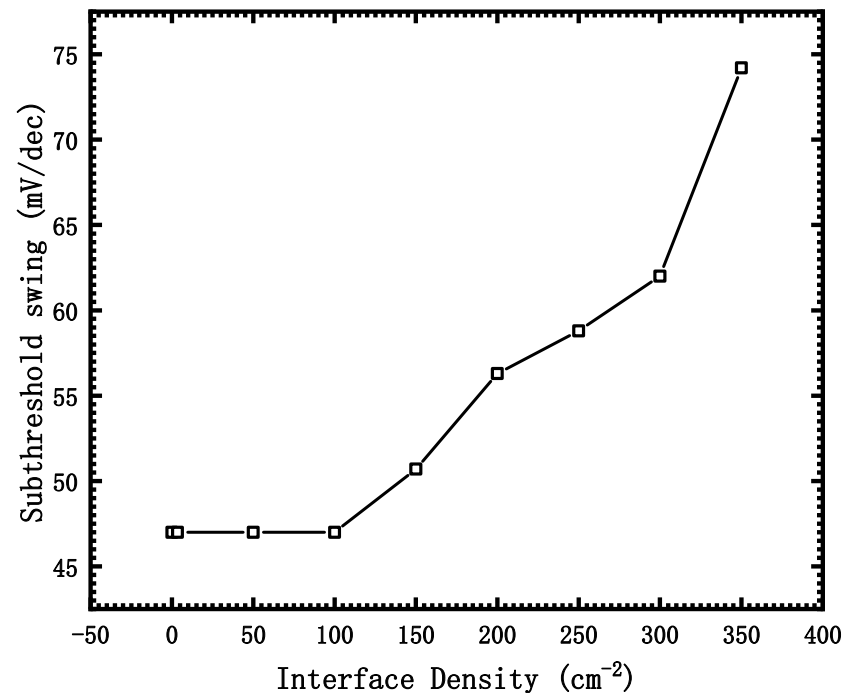


Figure 7. Subthreshold swing with different Interface Density.

It can be seen that the subthreshold swing of the device begins to increase obviously after the interface density of states reaches  $100 \text{ cm}^{-2}$ . After the interface density of states reaches  $350 \text{ cm}^{-2}$ , the subthreshold swing of the device deteriorates from  $47 \text{ mV/dec}$  to  $74.2 \text{ mV/dec}$ .

From the definition of subthreshold swing, the derivation of Equation (5) can be achieved:

$$SS = \frac{dV_G}{d \log_{10} I_D} = \frac{dV_G}{d\psi_s} \cdot \frac{d\psi_s}{d \log_{10} I_D} = \left(1 + \frac{C_D}{C_{\text{ox}}}\right) \cdot \frac{d\psi_s}{d \log_{10} I_D} \quad (5)$$

where  $C_{\text{ox}}$  is the gate oxide capacitance,  $C_D$  is the depletion capacitance and  $\psi_s$  is the surface potential. Due to the existence of the interface trap charge, a trap capacitance in parallel with  $C_D$  will be added, which will increase the equivalent depletion layer



capacitance  $C_D$ . The higher the interface trap concentration, the larger the equivalent depletion layer capacitance  $C_D$ , and the larger the subthreshold swing.

#### 4.3. Bipolar Effect

Because of the symmetrical structure of source and drain in TFET, taking n-type TFET as an example, when a large negative pressure is applied to the gate, band to band tunneling will occur in the drain region and body region, resulting in the increase of leakage current and the bipolar effect [19–22], as seen in Figure 8.

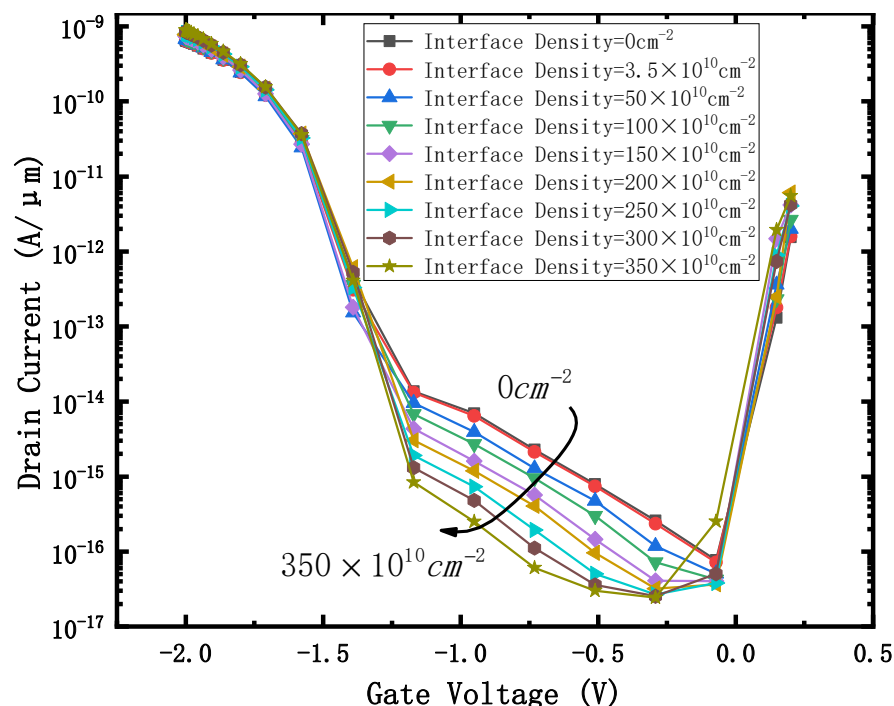


Figure 8.  $I_d$ -negative gate voltage with different Interface Density.

It can be seen that when the absolute value of negative voltage is very low ( $-1.2\text{ V}\sim 0\text{ V}$ ), the conduction current of the device decreases with the increase of irradiation dose; when the absolute value of negative voltage is large ( $>1.2\text{ V}$ ), and the irradiation dose has little effect on the conduction current of the device.

The tangent diagram of the energy band of the device under different negative gate voltages is shown in Figure 9 (transverse tangent of 2 nm upward at the interface between box layer and silicon film). It can be seen that the higher the irradiation dose, the lower the energy band in the channel region of the device. The more negative the gate voltage, the higher the energy band in the channel region, which indicates that the polarity of the electric field generated by the gate voltage in the channel region of the device is opposite to that caused by the total dose of irradiation. When the negative bias voltage is greater than  $-1.2\text{ V}$ , the electric field generated by the gate voltage is equivalent to the additional electric field caused by the total dose irradiation, and the total dose effect is obvious. It can be seen in Figure 9b that the higher the irradiation dose, the lower the channel energy band, and the more difficult it is to open the tunneling junction. Therefore, the negative conduction current will be suppressed with the increase of the irradiation dose. When the negative bias voltage is less than  $-1.2\text{ V}$ , the electric field intensity generated by the gate voltage in the channel increases, and the effect of the additional electric field caused by the total dose irradiation is not obvious. It can be seen in Figure 9a that, although the irradiation dose is equivalent to a  $350 \times 10^{10}\text{ cm}^{-2}$  interface-positive charge, the effect of the gate voltage still makes the tunneling junction have a considerable barrier difference  $\Delta\Phi$ , and the effect of the irradiation dose on the negative guide current is not obvious.



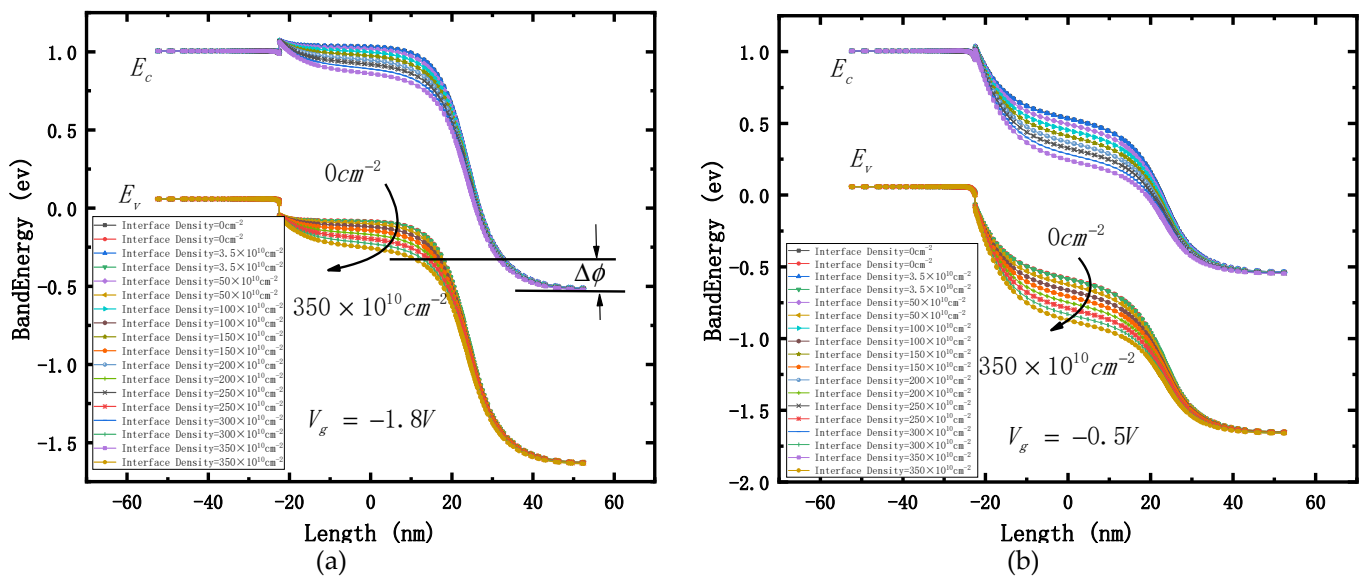


Figure 9. Band diagram with different interface density. (a) Gate voltage =  $-1.8\text{ V}$ ; (b) gate voltage =  $-0.5\text{ V}$ .

### 5. Hardening of BOX layer

The influence of a total dose irradiation on the device is quantified by the ratio of the drain current  $I_{\text{after}}$  after irradiation to the drain current  $I_{\text{before}}$  when the device is not irradiated. The thicknesses of the simulated box layers were 20, 40, 60, 80, 100 and 120 nm, respectively. The drain bias of the device was  $0.8\text{ V}$ , the gate voltage of the device was scanned from  $0.2\text{ V}$  to  $1.2\text{ V}$ , and the scanning point interval was  $0.2\text{ V}$ . The simulation method was to add the radiation model and the traps model. The irradiation rate was  $100\text{ rad/s}$  and the irradiation time was (0 s, 2000 s). The curves of  $I_{\text{after}}/I_{\text{before}}$  with different thicknesses of the box layer are shown in Figure 10:

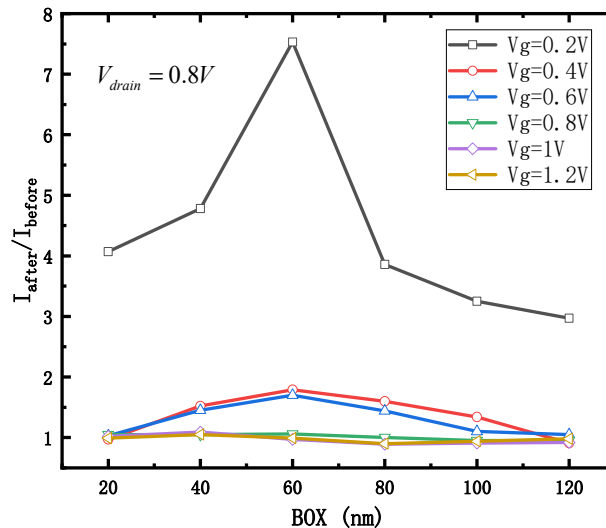
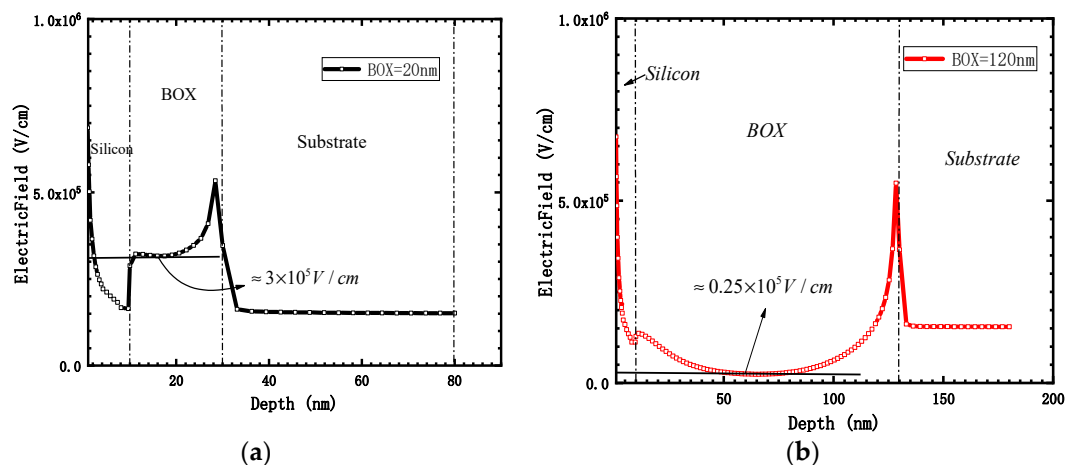


Figure 10.  $I_{\text{after}}/I_{\text{before}}$  with different thicknesses of BOX layer.

It can be seen that, with the increase of the thickness of the box layer, the ratio of  $I_{\text{after}}/I_{\text{before}}$  first increases, and then decreases. Generally speaking, when the thickness of the box layer is about 20 nm and 120 nm, the influence of the box layer on the total dose effect of the device is the smallest.

When the thickness of the box layer is 20 nm, the total dose effect will be at a very low level due to the small volume of the box layer and the limited area of fixed charge induced by irradiation.

When the thickness of the box layer is 120 nm, although the volume of the box layer of the device is increased under the same bias, the thicker the box layer, the smaller the internal electric field intensity, which is positively correlated with the generation rate of holes per unit volume. As shown in Figure 11 ( $V_{\text{gate}} = 1.2 \text{ V}$ , along the central vertical tangent of the channel), it can be seen that when the box layer thickness was 20 nm, most of the field strength of the device box layer was maintained at  $3 \times 10^5 \text{ V/cm}$ . When the box layer thickness was 120 nm, most of the field strength of the device box layer was maintained at  $0.25 \times 10^5 \text{ V/cm}$ , which is reduced by 12 times.



**Figure 11.** Tangent diagram of vertical distribution of electric field, (a) BOX = 20 nm; (b) BOX = 120 nm.

## 6. Conclusions

This paper focuses on the TID effect in SOI-TFET with an oxide/source overlap. It is found that radiation will obviously deteriorate the subthreshold swing and current switch ratio of device, while the threshold voltage is not affected obviously. When the negative voltage is not too large, the bipolar effect will be suppressed to some degree. The optimal thickness of the BOX layer is either 20 nm or 120 nm, where the device has the strongest resistance to total ionizing dose effects. This is of great significance for studying the radiation effect of TFET devices.

**Author Contributions:** Conceptualization and writing—original draft preparation, C.C.; methodology, S.W. and X.W.; validation, C.C. and X.W.; writing—review and editing, H.L. and S.W. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research was funded by the National Natural Science Foundation of China (grant no. U1866212).

**Conflicts of Interest:** The authors declare no conflict of interest.

## References

- Samuel, T.S.A.; Balamurugan, N.B.; Bhuvaneswari, S.; Sharmila, D.; Padmapriya, K. Analytical modelling and simulation of single-gate SOI TFET for low-power applications. *Int. J. Electron.* **2014**, *101*, 779–788. [\[CrossRef\]](#)
- Raad, B.R.; Nigam, K.; Sharma, D.; Kondekar, P.N. Performance investigation of bandgap, gate material work function and gate dielectric engineered TFET with device reliability improvement. *Superlattices Microstruct.* **2016**, *94*, 138–146. [\[CrossRef\]](#)
- Anand, I.V.; Samuel, T.S.A.; Vimala, P.; Shenbagavalli, A. Modelling and Simulation of Hetero-Dielectric Surrounding Gate TFET. *J. Nano Res.* **2020**, *62*, 47–58. [\[CrossRef\]](#)
- Lee, R.; Kwon, D.W.; Kim, S.; Kim, D.H.; Park, B.G. Investigation of Feasibility of Tunneling Field Effect Transistor (TFET) as Highly Sensitive and Multi-sensing Biosensors. *J. Semicond. Technol. Andence* **2017**, *17*, 141–146. [\[CrossRef\]](#)
- Wu, J.; Taur, Y. Reduction of TFET OFF-Current and Subthreshold Swing by Lightly Doped Drain. *IEEE Trans. Electron. Devices* **2016**, *63*, 1–4. [\[CrossRef\]](#)
- Ding, L.; Gnani, E.; Gerardin, S.; Bagatin, M.; Driussi, F.; Palestri, P.; Selmi, L.; Royer, C.L.; Paccagnella, A. Total Ionizing Dose Effects in Si-Based Tunnel FETs. *IEEE Trans. Electron. Devices* **2014**, *61*, 2874–2880. [\[CrossRef\]](#)

7. Ding, L.; Gnani, E.; Gerardin, S.; Bagatin, M.; Driussi, F.; Selmi, L.; Royer, C.L.; Paccagnella, A. Impact of bias conditions on electrical stress and ionizing radiation effects in Si-based TFETs. *Solid-State Electron.* **2016**, *115*, 146–151. [[CrossRef](#)]
8. Liu, H.; Cotter, M.; Datta, S.; Narayanan, V. Soft-error performance evaluation on emerging low power devices. *IEEE Trans. Device Mater. Reliab.* **2014**, *14*, 732–741.
9. Hemmat, M.; Kamal, M.; Afzali-Kusha, A.; Pedram, M. Hybrid TFET-MOSFET circuit: A solution to design soft-error resilient ultra-low digital circuit. *Integr. VLSI J.* **2017**, *57*, 11–19. [[CrossRef](#)]
10. Chander, S.; Bhowmick, B.; Baishya, S. Heterojunction fully depleted SOI-TFET with oxide/source overlap. *Superlattices Microstruct.* **2015**, *86*, 43–50. [[CrossRef](#)]
11. Mitra, S.K.; Bhowmick, B. Impact of interface traps on performance of Gate-on-Source/Channel SOI TFET. *Microelectron. Reliab.* **2019**, *94*, 1–12. [[CrossRef](#)]
12. Mitra, S.K.; Bhowmick, B. An Analytical Drain Current Model of Gate-On-Source/Channel SOI-TFET. *Silicon* **2019**, *11*, 3031–3039. [[CrossRef](#)]
13. Pandey, C.K.; Dash, D.; Chaudhury, S. Improvement in Analog/RF Performances of SOI TFET Using Dielectric Pocket. *Int. J. Electron.* **2020**, *107*, 1844–1860. [[CrossRef](#)]
14. Ghosh, P.; Bhowmick, B. Analysis of Kink Reduction and reliability issues in Low-voltage Dual Tunnel Diode based SOI TFET. *Micro Nano Lett.* **2019**, *15*, 130–135. [[CrossRef](#)]
15. Rao, M.; Ranjan, R.; Pradhan, K.P.; Sahu, P.K. Performance analysis of symmetric High-k Spacer (SHS) Trigate SOI TFET[C]//. In Proceedings of the 2016 3rd International Conference on Devices, Circuits and Systems (ICDCS), Coimbatore, India, 3–5 March 2016; pp. 133–136.
16. Mitra, S.K.; Goswami, R.; Bhowmick, B. A hetero-dielectric stack gate SOI-TFET with back gate and its application as a digital inverter. *Superlattices Microstruct.* **2016**, *92*, 37–51. [[CrossRef](#)]
17. Lee, M.S.; Lee, H.C. Dummy Gate-Assisted n-MOSFET Layout for a Radiation-Tolerant Integrated Circuit. *IEEE Trans. Nucl. Sci.* **2013**, *60 Pt 2*, 3084–3091. [[CrossRef](#)]
18. Gaillardin, M.; Martinez, M.; Paillet, P.; Raine, M.; Andrieu, F.; Faynot, O.; Thomas, O. Total Ionizing Dose Effects Mitigation Strategy for Nanoscaled FDSOI Technologies. *IEEE Trans. Nucl. Sci.* **2014**, *61*, 3023–3029. [[CrossRef](#)]
19. Rahimian, M.; Fathipour, M. Junctionless nanowire TFET with built-in N-P-N bipolar action: Physics and operational principle. *J. Appl. Phys.* **2016**, *120*, 225702. [[CrossRef](#)]
20. Kuamr, A.; Chatterjee, N.; Pandey, S.; Kardam, U.; Gupta, M. Analytical Modeling and Simulation Based Investigation of Advanced TFET Architecture[C]//. In Proceedings of the 2016 International Conference on Micro-Electronics and Telecommunication Engineering (ICMETE), Ghaziabad, India, 22–23 September 2016.
21. Zhang, Y.B.; Sun, L.; Xu, H.; Han, J.W. Simulation and comparative study of tunneling field effect transistors with do pant-segregated Schottky source/drain. *Jpn. J. Appl. Phys.* **2016**, *55*, 04ED09. [[CrossRef](#)]
22. Chandan, B.V.; Dasari, S.; Yadav, S.; Sharma, D. Approach to suppress ambipolarity and improve RF and linearity performances on ED-Tunnel FET. *IET Micro Nano Lett.* **2019**, *14*, 86–90. [[CrossRef](#)]