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A 7.6-nW 1-kS/s 10-Bit SAR ADC for Biomedical Applications

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Abstract: This paper presents a 10-bit successive approximation register analog-to-digital converter with energy-efficient low-complexity switching scheme, automatic ON/OFF comparator and automatic ON/OFF SAR logic for biomedical applications. The energy-efficient switching scheme achieves an average digital-to-analog converter switching energy of $63.56 CV_{ref}^2$, achieving a reduction of 95.34% compared with the conventional capacitor switching scheme for CDACs. With the switching scheme, the ADC can lower the dependency on the accuracy of V_{cm} and complexity of DAC control logic and DAC driver circuit. Moreover, dynamic circuits and automatic ON/OFF technology are used to reduce power consumption of comparator and SAR logic. The prototype is designed and fabricated in a 180 nm CMOS with a core size of $500 \mu\text{m} \times 300 \mu\text{m}$ (0.15 mm^2). It consumes 7.6 nW at 1 kS/s sampling rate and 1.8-V supply with an achieved signal-to-noise-and-distortion ratio of 45.90 dB and a resulting figure of merit of 51.7 fJ/conv.-step.

Keywords: analog-to-digital converter (ADC); energy-efficient; successive approximation register (SAR)



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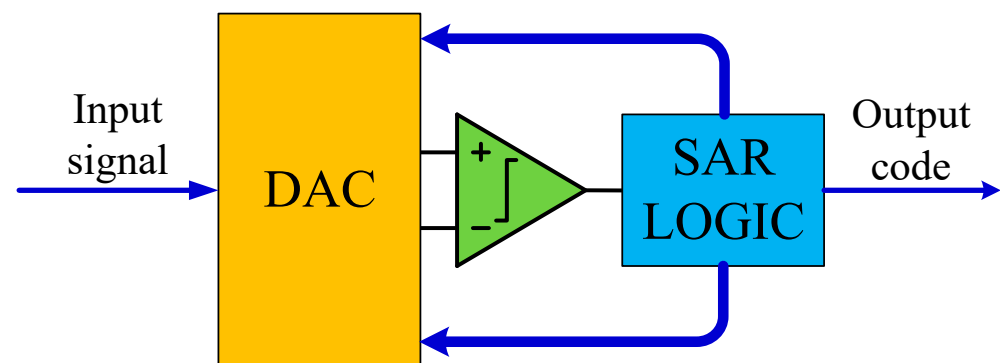
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1. Introduction

The development of low-power integrated circuits (ICs) will help bring portable and implantable biomedical devices and biosensors to the market. Analog front end (AFE) circuits in these products may consume most of the total power budget because they usually need to remain online to sense input signals continuously [1]. Various biomedical signals and their frequency ranges are shown in Table 1. Most biomedical signals have frequencies below 1 kHz. Figure 1 shows the basic processing units in a biomedical implantable device [2]; ADC is an intermediate unit that converts analog signals into digital signals. Successive-approximation register (SAR) analog-to-digital converter (ADC) has become an appropriate choice for low-power biomedical applications in recent years due to its low-power characteristics [2–5]. Figure 2 shows the basic components in an SAR ADC. Among the building blocks in an SAR ADC, a capacitive DAC always consumes a significant part of the total power consumption [6–8]. Recently, some energy-efficient switching schemes have been proposed to reduce the energy consumption of DAC capacitor arrays. [8–10]. Compared to conventional techniques [11], Charge-Recovery [8], Charge-Sharing [8], Capacitor-Splitting [8], Set-and-down [10], and V_{cm} -based [9] techniques reduce the switching energy by 12.52%, 24.99%, 37.48%, 81.26%, and 87.52%, respectively. However, these schemes have various drawbacks. Capacitor-Splitting [8] and V_{cm} -based [9] schemes have complex DAC drive circuits, the Set-and-down scheme [10] has large common-mode voltage shift, and the V_{cm} -based scheme [9] has a high dependence on the middle reference voltage (V_{cm}).

Table 1. Frequency ranges of various biomedical signals.

Biomedical Signals	Frequency Range
ECG [2]	0.05–100 Hz
ECoG [12]	70–110 Hz
EMG [13]	50–150 Hz
EEG [14]	0–100 Hz

**Figure 1.** Block diagram of biomedical implantable device.**Figure 2.** Building blocks of SAR ADC.

In this paper, the energy-efficient and low-complexity switching scheme [15] is used to realize successive approximation conversion. In the first comparison, no switching energy was consumed due to the use of top-plate sampling technology [10]. In the second comparison, no switching energy was consumed due to the closed-loop charge recycling method [16]. From the third comparison to the $(N-1)$ th comparison, the reference voltage of the corresponding capacitor in the lower voltage capacitor array changes from gnd to V_{ref} . In the last comparison, the reference voltage of the last capacitor in the lower voltage capacitor array changes from gnd to V_{cm} . From the third comparison to the last comparison, since there is only one capacitor-switching reference voltage for each comparison, the power consumption is low. As a result, the energy-efficient and low-complexity switching scheme achieves an average switching energy of $63.56 CV_{ref}^2$. Compared with the conventional switching scheme [11], this switching scheme reduces the switching energy by 95.34%. In addition, only the least significant bit (LSB) depends on the accuracy of V_{cm} , and each capacitor only uses two reference voltages, which reduces the dependence on the accuracy of V_{cm} and the complexity of DAC control logic and DAC driver circuit. An automatic ON/OFF comparator is used to achieve low power consumption. The comparator consists of three parts: the automatic ON/OFF clock circuit, the dynamic preamplifier stage, and the dynamic latch stage. The automatic ON/OFF clock circuit allows the comparator to work only during comparing. Automatic ON/OFF SAR Logic consists of three parts: automatic ON/OFF clock circuit, shift control, data latch. The automatic ON/OFF clock signal is generated by the comparator output signal, and the clock is output only when the comparator is active. In order to simplify the DAC control logic and DAC driver circuit, the latch of SAR logic uses a dynamic latch with differential output. When the proposed SAR ADC uses 180 nm CMOS process and operates at a sampling rate of 1 kS/s, the ADC achieves 45.90 dB SNDR and 58.79 dB SFDR and consumes only 7.6 nW [17]. The proposed SAR ADC is suitable for portable and implantable medical sensors.

This paper is organized as follows. Section 2 describes the ADC architecture and low-power circuits. Section 3 shows the measurement results and the comparison with other ADCs. Finally, Section 4 concludes.

2. Proposed ADC Architecture

As shown in Figure 3, the proposed SAR ADC consists of comparator, SAR logic, capacitor array DAC and DAC drive circuit. Because each capacitor of the capacitor array DAC has only two reference voltages, the DAC drive circuit and DAC control logic are simple. In addition, because the last capacitor uses V_{cm} as the reference voltage, the number of unit capacitors is reduced by half.

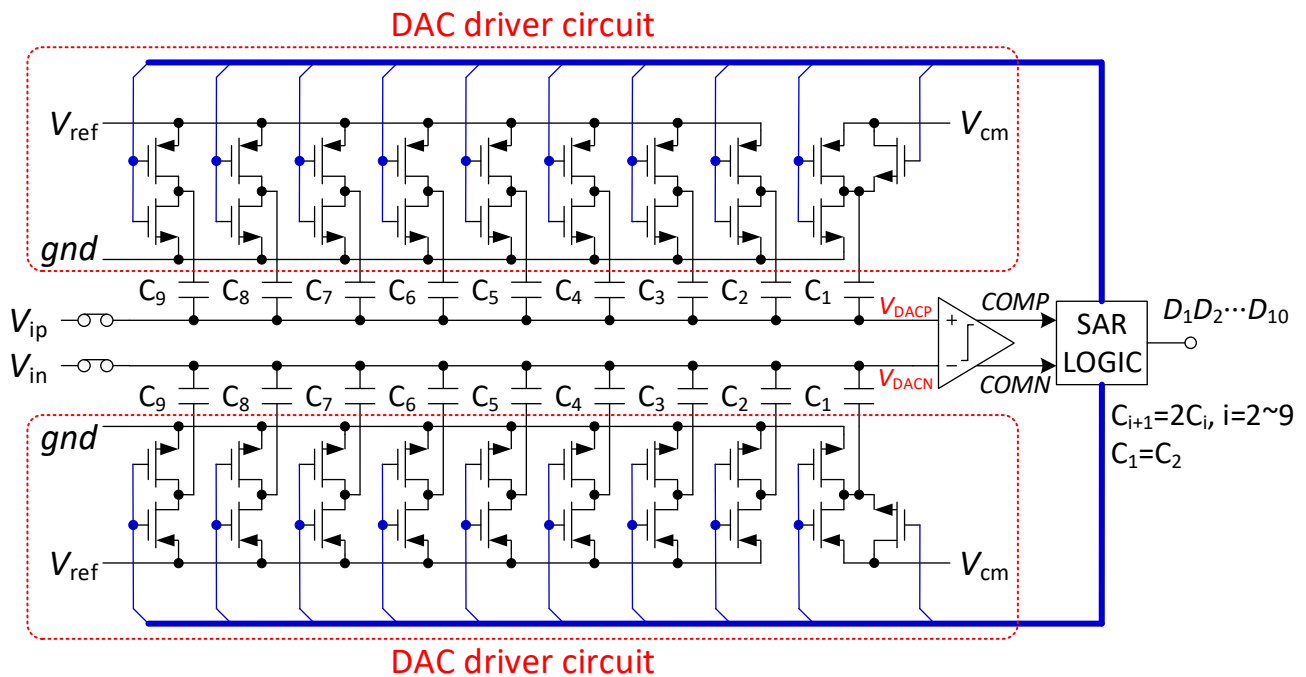


Figure 3. Proposed 10-bit SAR ADC architecture.

2.1. Switching Scheme

As shown in Figure 4, the operation of the switching scheme can be performed in five phases: sampling, the 1st comparison, the 2nd comparison, the 3rd to $(N-1)$ th comparison, and the N th comparison.

Sampling: In the sampling phase, the input signals are sampled on the top-plates of all capacitors via sampling switch, with the bottom-plates of the largest capacitors connecting to V_{ref} and other capacitors to gnd .

The 1st comparison: After sampling, the sampling switches are turned off. The output voltages of the DAC capacitor array are found to be

$$\begin{cases} V_{DACP}(1) = V_{ip} \\ V_{DACN}(1) = V_{in} \end{cases} \quad (1)$$

The comparator compares the sampling signals (V_{ip} and V_{in}) and gets D_1 (MSB). No switching energy is consumed in the first comparison.

$$E_1 = 0 \quad (2)$$

The 2nd comparison (level-shift- gnd): If $D_1 = 1$, the reference voltage of the largest capacitor in the positive capacitor array changes from V_{ref} to gnd . If $D_1 = 0$, the reference voltage of the largest capacitor in the negative capacitor array becomes gnd . As a result, the voltage of the higher side is decreased by $V_{ref}/2$, and the output voltages are found to be

$$\begin{cases} V_{DACP}(2) = V_{ip} - D_1 \frac{V_{ref}}{2} \\ V_{DACN}(2) = V_{in} - (1 - D_1) \frac{V_{ref}}{2} \end{cases} \quad (3)$$

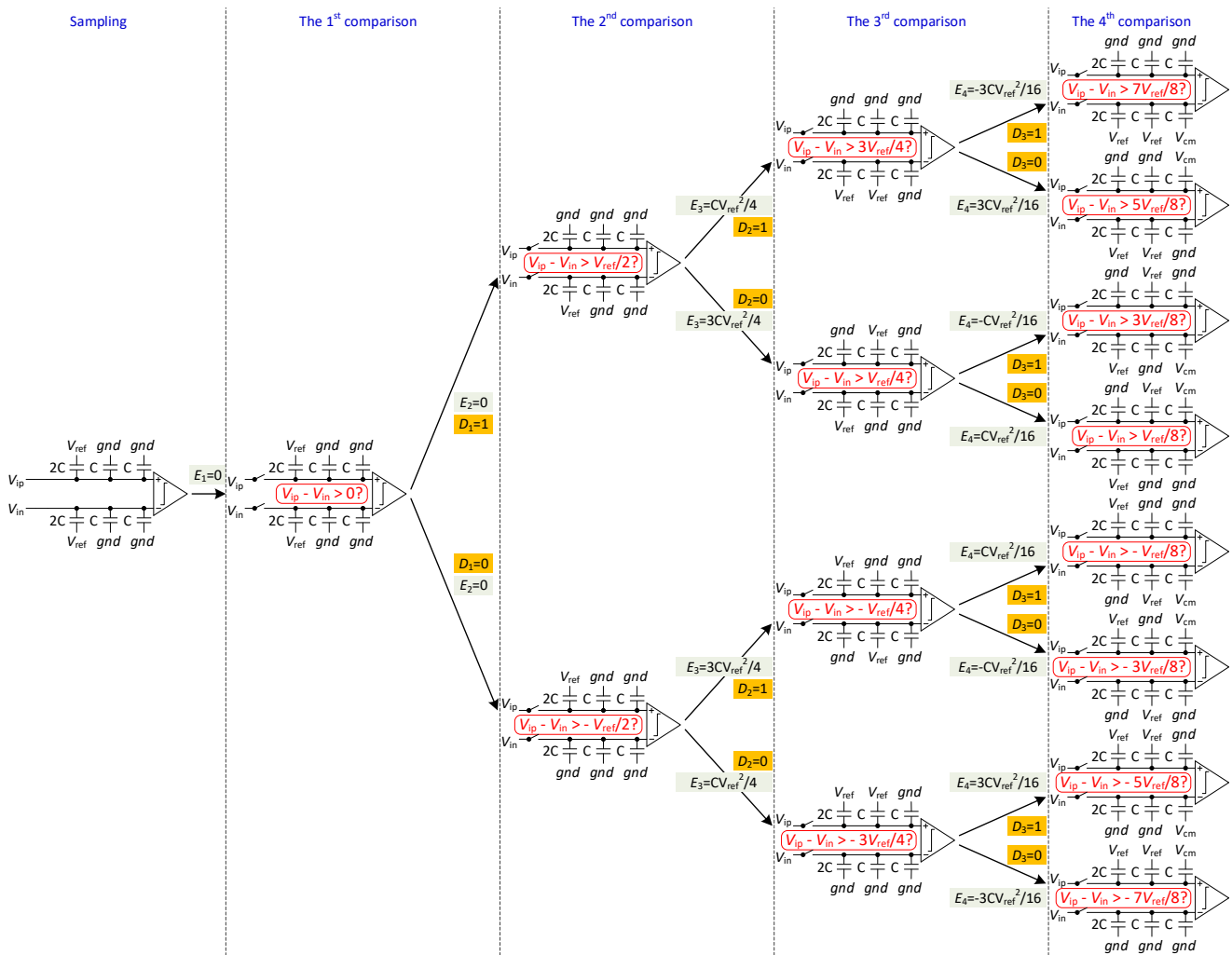


Figure 4. Switching procedure of 4-bit SAR DAC.

The comparator compares $V_{DACP}(2)$ with $V_{DACN}(2)$ and gets D_2 . Due to the closed-loop charge recycling method [16], there is no switching energy consumption in the second comparison.

$$E_2 = 0 \tag{4}$$

The 3rd to $(N-1)$ th comparison (“up” operation): According to the previous comparison results, the reference voltage of the corresponding capacitor in the lower voltage capacitor array is switched from gnd to V_{ref} , while the other one (in the higher voltage capacitor array) remains unchanged. For example, in the third comparison, if $D_2 = 1$, the reference voltage of the second largest capacitor in the negative capacitor array is switched from gnd to V_{ref} . If $D_2 = 0$, the reference voltage of the second largest capacitor in the positive capacitor array is switched from gnd to V_{ref} . The ADC repeats the procedure until the $(N-1)$ th comparison is completed. The output voltages of each comparison are found to be

$$\begin{cases} V_{DACP}(i) = V_{ip} - D_1 \frac{V_{ref}}{2} + \sum_{j=2}^{i-1} (1 - D_j) \frac{V_{ref}}{2^j} \\ V_{DACN}(i) = V_{in} - (1 - D_1) \frac{V_{ref}}{2} + \sum_{j=2}^{i-1} D_j \frac{V_{ref}}{2^j} \end{cases} \tag{5}$$

The comparator compares $V_{DACP}(i)$ with $V_{DACN}(i)$ and gets D_i . During the switching procedure, there is only one capacitor switch for each comparison, resulting in less switch-

ing activity and lower energy. Based on the switching energy calculation method in [6], the switching energy of each comparison is found to be

$$E_i = \left\{ \begin{array}{l} 2^{N-i-1} - 2^{N-2i} - D_{i-1} \sum_{j=1}^{i-2} D[j] 2^{N-j-i-1} \\ -(1 - D_{i-1}) \sum_{j=1}^{i-2} (1 - D[j]) 2^{N-j-i-1} \end{array} \right\} CV_{ref}^2 \quad (6)$$

*N*th comparison: In the *N*th comparison, the reference voltage of the last capacitor in the lower side is switched from *gnd* to V_{cm} while the other one (on the higher side) remains unchanged. The output voltages and switching energy are found to be

$$\left\{ \begin{array}{l} V_{DACP}(N) = V_{ip} - D_1 \frac{V_{ref}}{2} + \sum_{j=2}^{N-1} (1 - D_j) \frac{V_{ref}}{2^j} \\ V_{DACN}(N) = V_{in} - (1 - D_1) \frac{V_{ref}}{2} + \sum_{j=2}^{N-1} D_j \frac{V_{ref}}{2^j} \end{array} \right\} \quad (7)$$

$$E_N = \left\{ \begin{array}{l} D_1(1 - D_{N-1}) \left[2^{-2} - 2^{-N} - \sum_{j=1}^{N-2} (1 - D[j]) 2^{-j-1} \right] \\ +(1 - D_1) D_{N-1} \left[2^{-2} - 2^{-N} - \sum_{j=1}^{N-2} D[j] 2^{-j-1} \right] \end{array} \right\} CV_{ref}^2 \quad (8)$$

The average switching energy of the switching scheme is derived as

$$E_{average} = \frac{11 \dots 1}{D_1 D_2 \dots D_{N-1} = 00 \dots 0} \left(\sum_{i=1}^N E_i \right) = (2^{N-4} - 2^{-1} + 2^{-4}) CV_{ref}^2 \quad (9)$$

Figure 5 shows switching energy at each output code for different switching schemes. The average switching energy of the switching scheme used for 10-bit SAR ADC is $63.56 CV_{ref}^2$. Compared with the conventional switching scheme [11], the used switching scheme [15] and Capacitor-Splitting [8], Set-and-down [10], and V_{cm} -based [9] schemes reduce the switching energy by 95.34%, 37.48%, 81.26%, and 87.52%, respectively. Figure 6 presents the 500-run Monte Carlo simulation results of the proposed DAC switching scheme with unit capacitor mismatch of $\sigma_u/C_u = 1\%$. The RMS DNL and the RMS INL of the proposed DAC switching scheme are 0.325 LSB and 0.326 LSB, respectively.

2.2. Automatic ON/OFF Comparator

A low-power two-stage full dynamic comparator is reported in [18]. In order to save more power consumption of the comparator, an automatic ON/OFF clock circuit is added to the comparator. As shown in Figure 7a, the comparator consists of automatic ON/OFF clock circuit, dynamic preamplifier stage, and dynamic latch stage. In the dynamic preamplifier stage, V_{DACP} and V_{DACN} are the output signals of the DAC capacitor array and are connected to the differential inputs of the comparator. *AP* and *AN* are differential outputs of the dynamic preamplifier stage. In the dynamic latch stage, *COMP* and *COMN* are the comparison results, which are obtained by *AP*, *AN*, and *CCLK* driving the latch. In the process of result latching, no power-to-ground current path is formed, so the comparator only has a dynamic power supply. The automatic ON/OFF clock circuit generates the clock for comparator operation. When the \overline{RST} is high or $P_{10} + N_{10}$ (P_{10} and N_{10} are the 10th comparison result that latched in SAR logic) is high, there is no clock output, the comparator is in the OFF state, and the comparator has no power consumption. Figure 7b shows the timing diagram of the comparator.

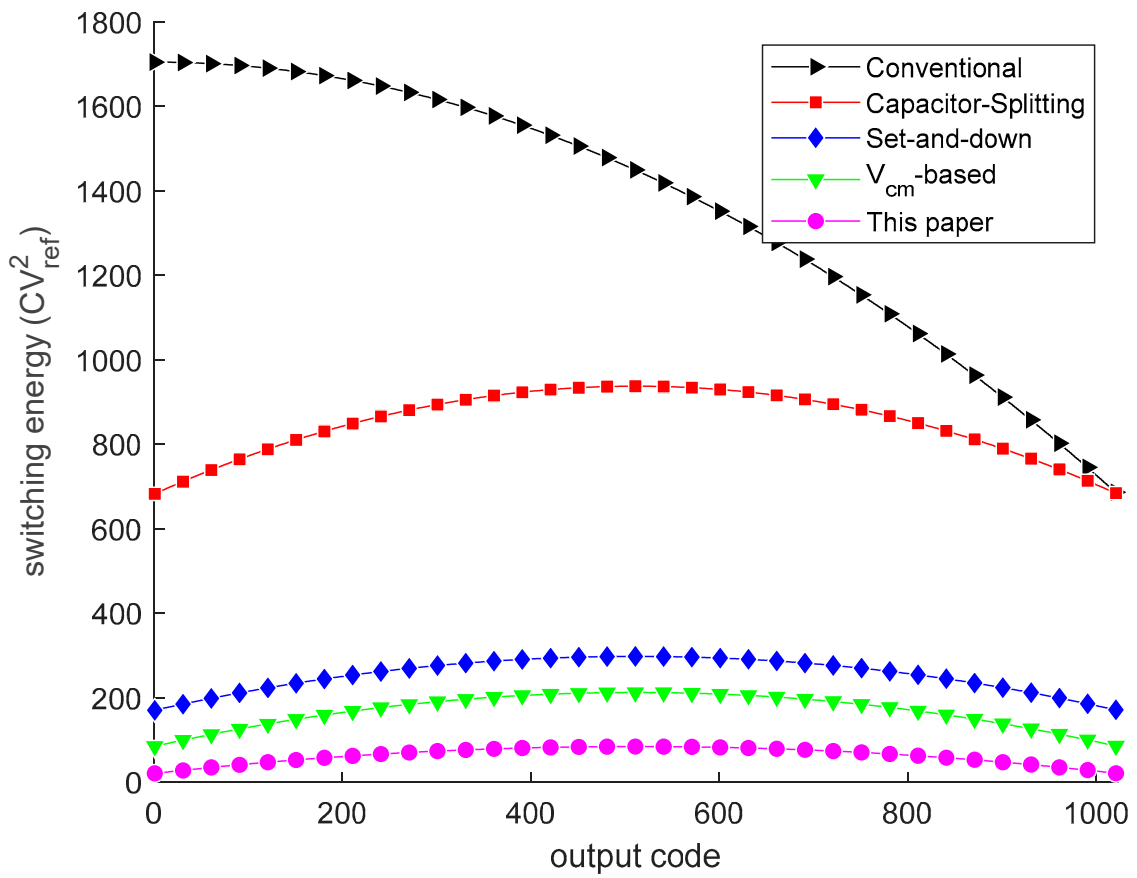


Figure 5. Switching energy against output codes. The black [11], red [8], blue [10], green [9], and magenta curves are switching energy.

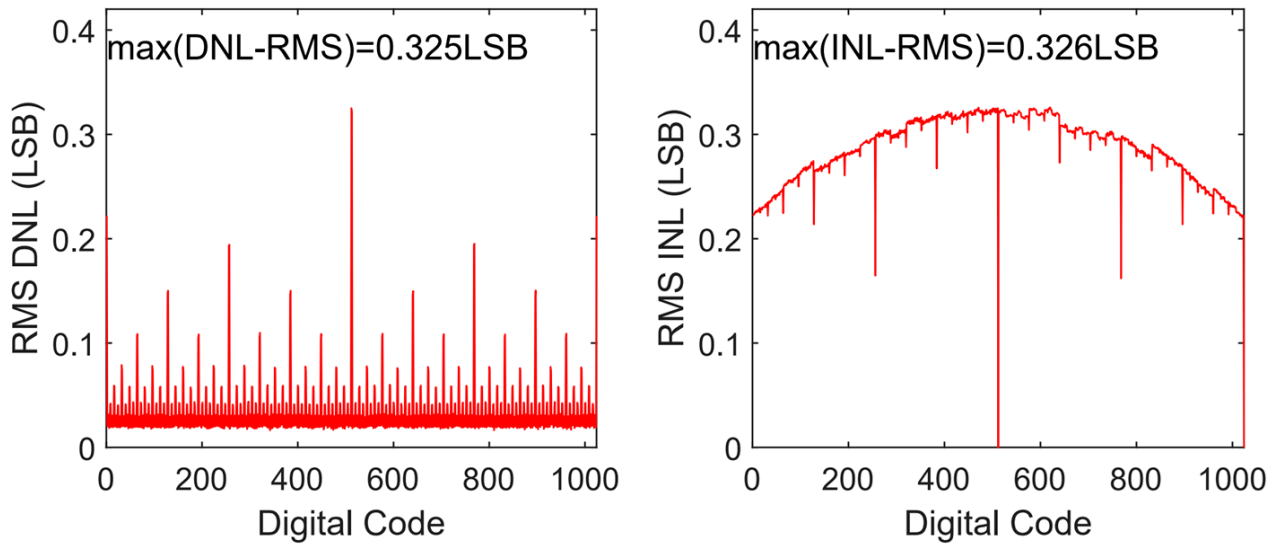


Figure 6. DNL and INL versus output code of the proposed switching scheme.

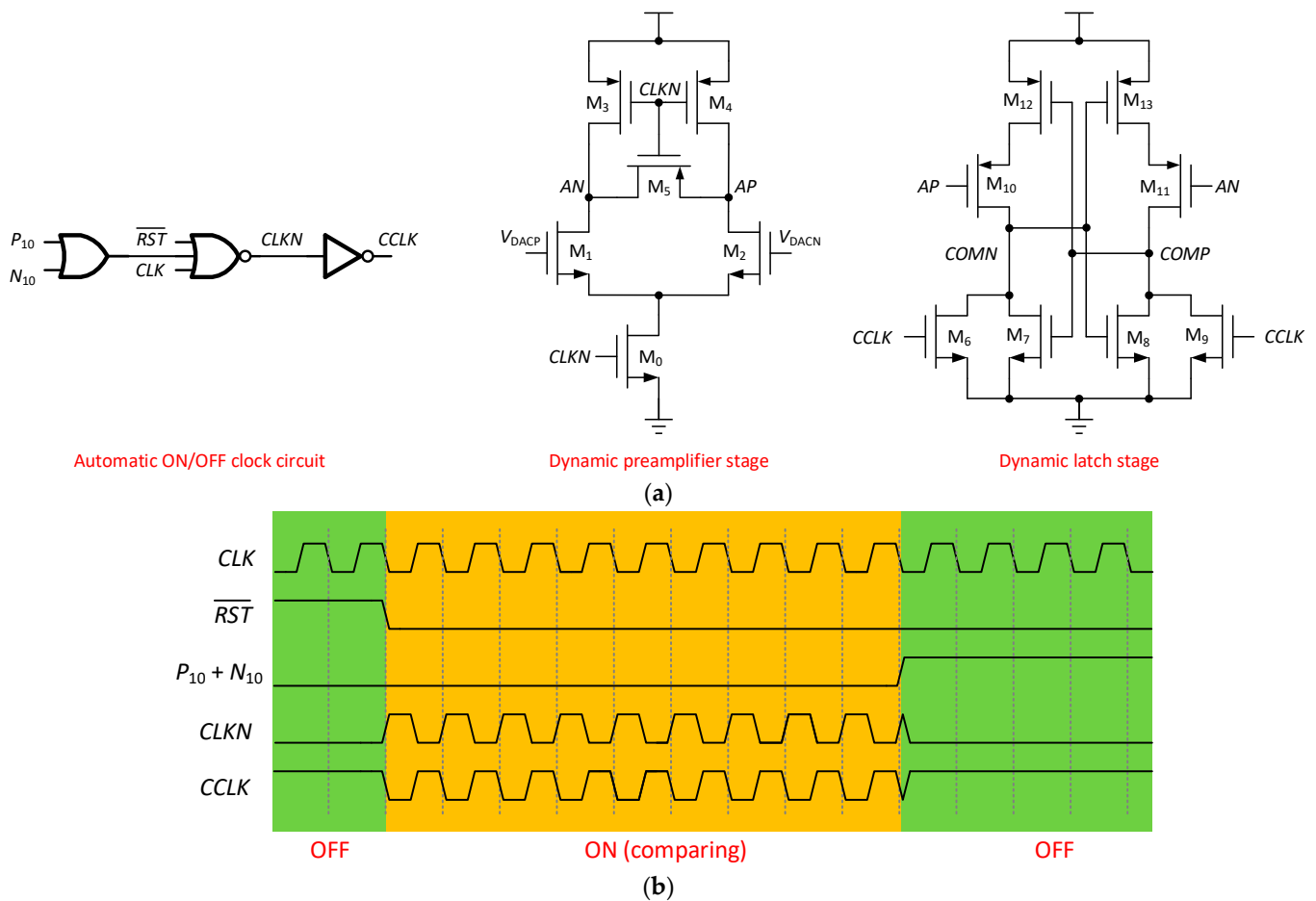


Figure 7. Automatic ON/OFF comparator. (a) Schematic diagram; (b) Timing diagram.

2.3. Automatic ON/OFF SAR Logic

As shown in Figure 8, the automatic ON/OFF SAR logic consists of an automatic ON/OFF clock circuit, a sequencer, and a data register. The sequencer is a shift register that shifts the set signal through a series of D flip-flops. The set signal is then used to activate the Latch in the data register. When the last D flip-flop in the sequencer is triggered, the sequencer will be reset and await the next conversion cycle. The data register is composed of dynamic latches, which can latch the differential outputs of the comparator and output differential data. Differential output makes DAC logic circuit simpler. The automatic ON/OFF clock circuit is used to provide the drive clock signal for the shift register. Drive clock is only ON while comparison results are being latched, thus reducing SAR logic power consumption. Figure 8b shows the timing diagram of the SAR logic.

2.4. DAC Driver Circuit

As shown in Figure 9, each capacitor requires two reference voltages. The reference voltages of C_2 to C_9 capacitors are V_{ref} and gnd , and the drive circuit can be realized by CMOS inverter. The reference voltage of C_1 capacitor is V_{cm} and gnd , and the driving circuit adopts a hybrid structure of CMOS transmission gate and CMOS inverter circuit.

2.5. Capacitor Array

Figure 10 illustrates the floorplan of the capacitor array DAC for a single side. Both sides have identical layout design. DAC capacitors and dummy capacitors are represented by squares (unit capacitors) in different colors. DAC capacitors are surrounded by dummy capacitors to minimize the proximity effects and second-order lithographic errors. Additionally, a common centroid layout is used to reduce parasitic effects.

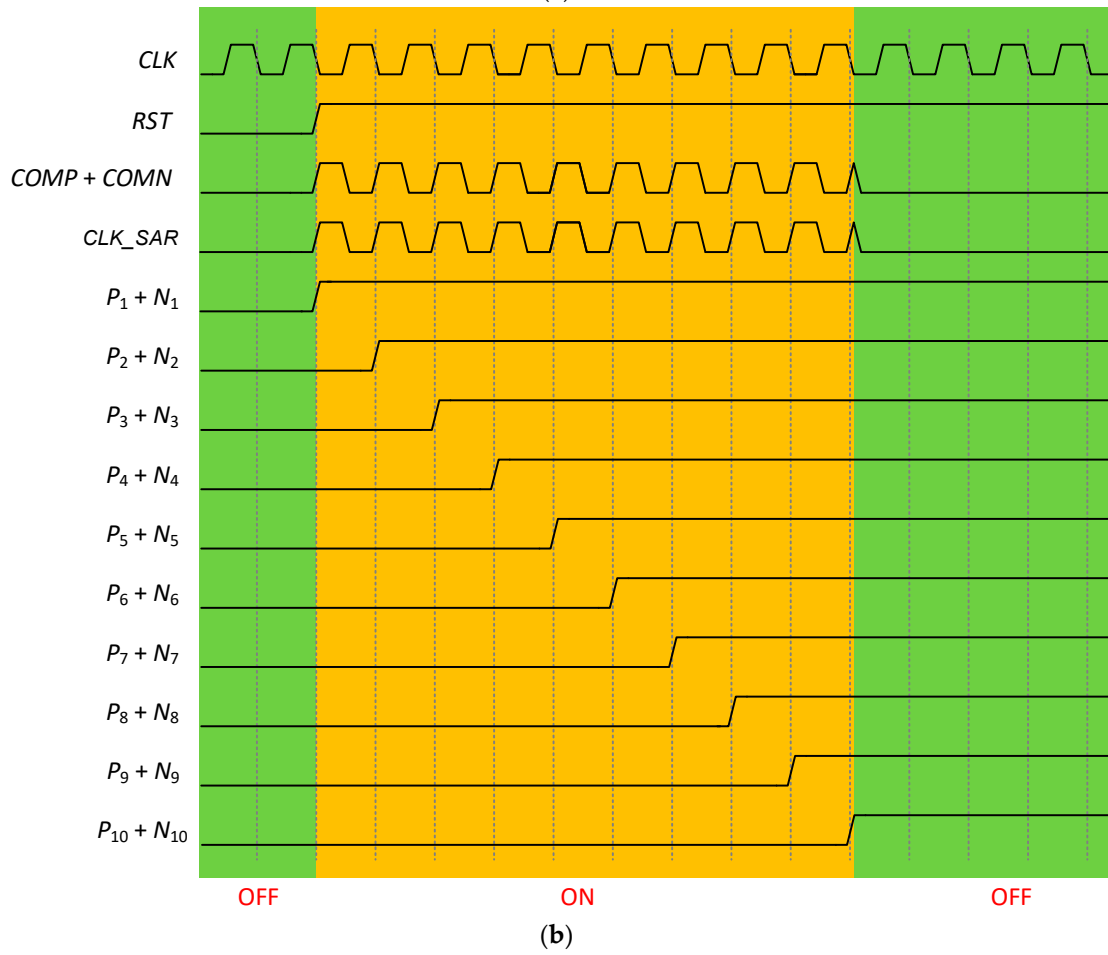
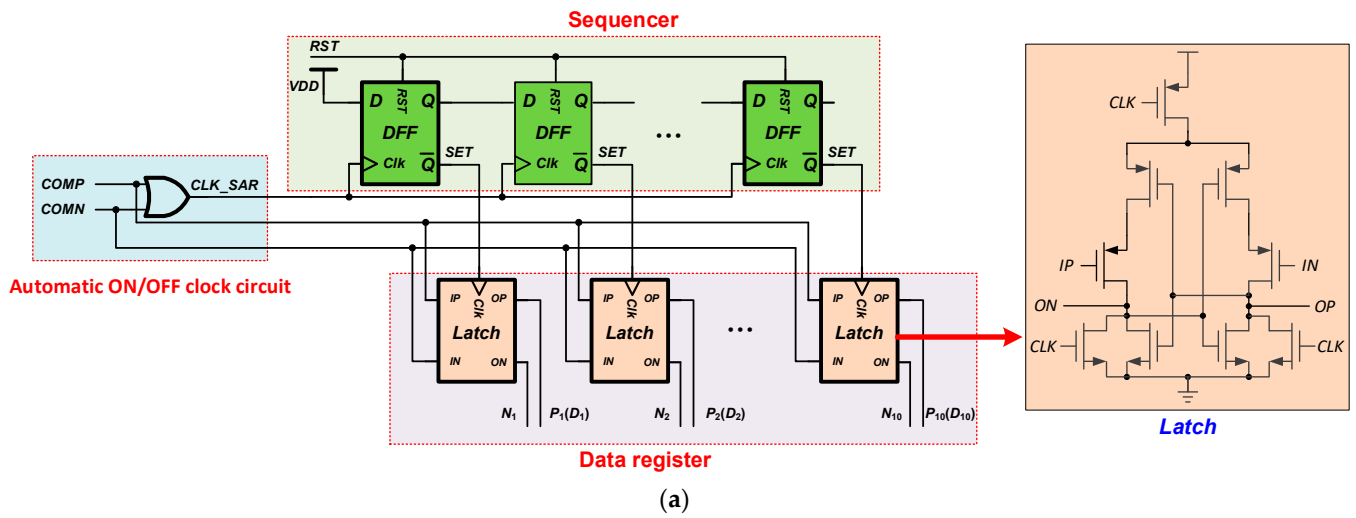


Figure 8. Automatic ON/OFF SAR logic. (a) Block diagram; (b) Timing diagram.

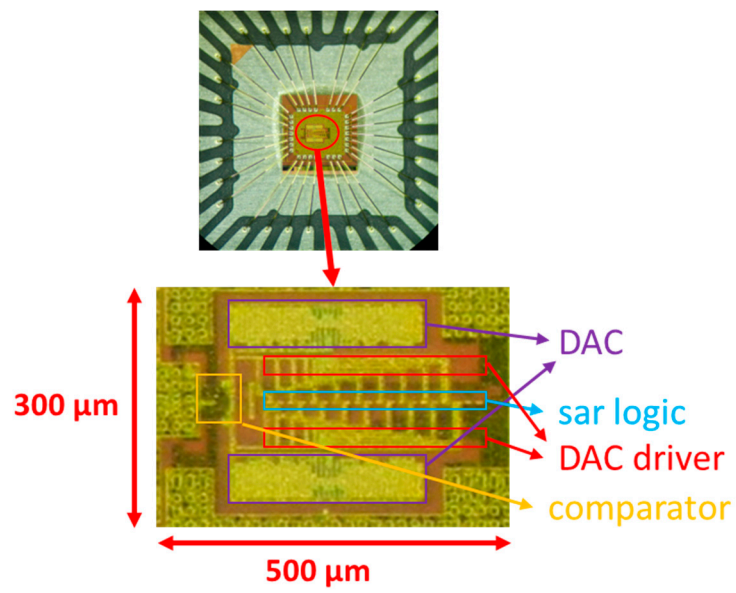
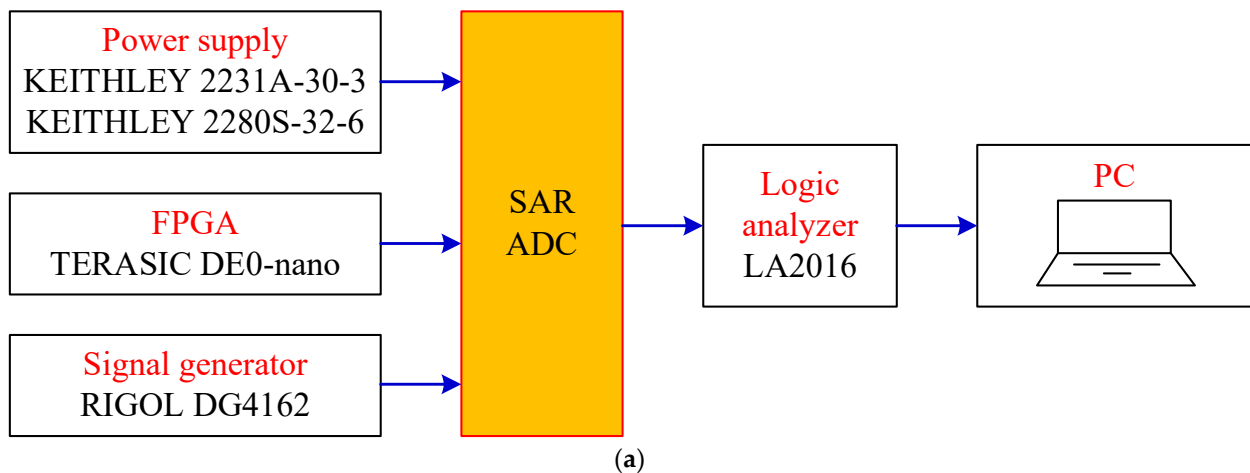
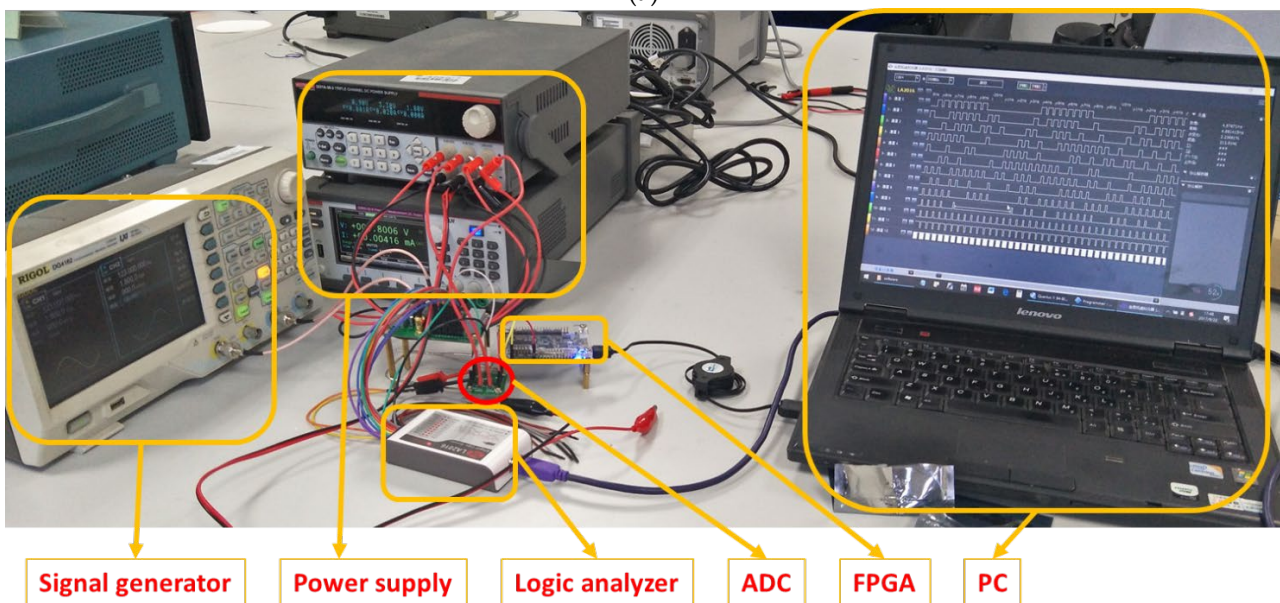


Figure 11. Chip micrograph.



(a)



(b)

Figure 12. Measurement environment. (a) Block diagram; (b) Photo.

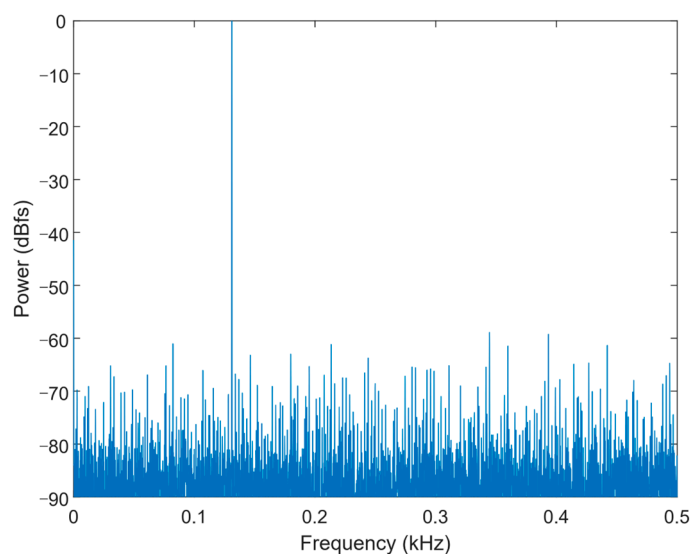


Figure 13. FFT spectrum.

Table 2. Performance comparison.

Specification	[19]	[20]	[21]	This Work
Technology (nm)	65	180	65	180
Resolution (bit)	14	10	8	10
Supply Voltage (V)	0.8	1	0.6	1.8
Sampling Rate (kS/s)	10	1	0.5	1
Power (nW)	1980	120	1.8	7.6
ENOB (bit)	12.5	9.76	7.14	7.2
FoM (fj/conv.-step)	34.2	138.4	25.5	51.7

4. Conclusions

This paper has presented a low-power SAR ADC for biomedical applications. The ADC uses an energy-efficient, low-complexity switching scheme to reduce power consumption. Because of the top-plate sampling and level-shift-gnd operations, the switching scheme did not consume energy in the first and second comparisons. Thanks to the use of V_{cm} for the last capacitor, the total capacitance is reduced by half, so the energy consumption of DAC is also reduced. In addition, because of the automatic ON/OFF technology, the comparator and SAR logic only generate energy consumption during operation. The proposed SAR ADC achieves FoM of 51.7 fj/conv.-step at 1.8 V supply and 1 KS/s sampling rate. If the ADC adopts a low-voltage design method, more energy consumption will be saved. The proposed low-power SAR ADC is suitable for biomedical applications.

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