



# **Communication An Experimental Investigation of the Degradation of CMOS Low-Noise Amplifier Specifications at Different Temperatures**

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**Abstract:** To investigate the relationship between the specifications degradation of a low-noise amplifier (LNA) and temperature, we experimentally investigated the degradation characteristics of the specifications of the LNA at different temperatures. The small-signal gain (S21) of the LNA decreases with increasing temperature. This paper discusses and analyzes the experimental results in detail, and the reasons for the degradation of LNA specifications with temperature changes are known. Finally, we have tried to use the structure already available in the literature for the PA temperature compensation circuit for the temperature compensation of the LNA. The results show that the existing circuit structure for PA temperature compensation in the literature can also effectively compensate for the S21 and NF degradation of the LNA due to the temperature increase.

Keywords: CMOS; specification degradation; temperature; LNA



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# 1. Introduction

A low-noise amplifier (LNA) is used in the first stage of a radio frequency (RF) transceiver to amplify a signal with low noise [1]. At the same time, the specification of the LNA will change with the change in temperature because the parameters of semiconductors are very sensitive to the change in temperature [2,3]. Therefore, their system will fail when the specifications of LNAs decrease with the temperature change; thus, they cannot meet the minimum requirements required for the system's normal operation.

Current research on LNAs focuses on the optimization of performance specifications, such as bandwidth [4–6], linearity [7–9], gain [10,11], noise figure [12,13], and power consumption [14–16]. For example, in 2016, G. Nikandish et al. [4] proposed a feedback amplifier circuit to increase the bandwidth of the LNA. In 2016, Sunhwan Jang et al. from the United States published a paper entitled "A High-Gain Power-Efficient Wideband V-Band LNA in 0.18 µm SiGe Bipolar Complementary Metal-Oxide Semiconductor (BiCMOS)", in which Sunhwan Jang et al. used an effective wideband gain shaping method to improve the gain of LNAs at low power consumption [11]. Furthermore, at the 2018 18th Mediterranean Microwave Symposium, O. Memioglu et al., scholars from Middle East Technical University, presented a cascaded topology with excellent noise figures consisting of cascaded topology with inductive source degradation of co-sourced devices [7]. In 2020, Yuito Sawayama et al. from Okayama Prefectural University in Japan achieved a low-noise figure LNA by replacing the primary inductor with an external inductor in the input matching circuit [13]. In 2021, Roman Yu. Musenov, an academic from Russia, et al. proposed a single-ended lowpower LNA based on 90 nm CMOS technology, which achieves low power consumption by employing current reuse techniques [15]. These studies focus on improving the bandwidth, linearity, and gain of LNAs, and reducing the noise figure and power consumption.

In this paper, we investigate the relationship and law of degradation of LNA specifications with temperature changes, taking 50 MHz–450 MHz CMOS LNAs as an example.

The reasons for the degradation of LNA specifications, such as gain and noise figure with increasing temperature, are discussed and analyzed. Based on this, we also designed a circuit for compensating the temperature characteristics of this LNA, which consists of a diode and two resistors. The simulation results show that this compensation circuit can effectively compensate for the degradation of S21 and NF due to temperature. The results can provide a theoretical reference for the design of the temperature compensation circuit of LNA. On the other hand, it can provide effective guidance for optimizing the system design.

# 2. Structure and Experimental Setup of LNA

2.1. The Structure of LNA

The schematic diagram of the LNA and the chip micrograph are shown in Figures 1 and 2, respectively.



Figure 1. The schematic diagram of the LNA [17].

As shown in Figure 1, the LNA is manufactured using a 0.18 um CMOS process [17]. In this LNA, a shunt feedback structure is used in the matching stage to reduce the noise factor of the LNA [17]. The load of the matching stage uses a PMOS (positive channel metal oxide semiconductor) current source in parallel with a resistor, mainly to relax voltage headroom and achieve adequate performance in process corners [17,18].

Figure 2 shows a micrograph of the chip of the LNA, which was gold wire bonded to a PCB (printed circuit boards) board to facilitate temperature characterization experiments in an environmental chamber. The left and right ends of the PCB are the input and output, respectively, which are connected to the test system via a 50-ohm matched subminiature version A (SMA). In addition, external inductors and resistors are used at the input and output of the PCB to achieve better matching. Two supply voltages are used for this LNA, 1.8 V and 3.3 V, respectively.



Figure 2. The micrograph of the chip of the LNA.

#### 2.2. Experimental Environment and Setup

As shown in Figure 3, the experiments were conducted in a chamber (SC<sup>3</sup> 1000) that can support conducting high- and low-temperature experiments from -40 °C to



125 °C. However, due to the constraints of the experimental cable, only the temperature characteristics of the LNA from -40 °C to 90 °C are investigated.

**Figure 3.** Measurement environment and setup: (**a**) a schematic diagram of the S-parameter measurement; (**b**) a schematic diagram of the NF measurement; (**c**) a physical diagram of the measurement environment.

In the experimental process, we focused on the temperature characteristics of the gain and noise figure. The gain and noise figures were measured with a vector network analyzer (VNA) (AV3672B) and a noise figure analyzer (N8975A). In addition, a Rohde & Schwarz power supply (NGMO2) was used for the power supply required in the experiments.

# 3. Results and Discussions

# 3.1. The S21

The temperature characteristics of the LNA gain are shown in Figure 4. From the figure, we can see that S21 is not only a function of temperature, but also a function of frequency. As the temperature increases, the S21 of the LNA gradually decreases. S21 decreases with increasing frequency, only differing at individual points. This may be caused by jitter in the measurement system during the measurement process.

The specific causes of the degradation of the gain of the LNA with increasing temperature are discussed below.

The expressions for  $I_{DS}$  in the linear and nonlinear regions, respectively, are [19,20]

$$I_{DS-linear} = \frac{W\mu_n C_{ox}}{2L} \left[ 2(V_{GS} - V_{TH}) V_{DS} - V_{DS}^2 \right]$$
(1)

$$I_{DS-nonlinear} = \frac{W\mu_n C_{ox}}{2L} (V_{GS} - V_{TH})^2$$
<sup>(2)</sup>

where *W* is the gate width,  $\mu_n$  is the carrier mobility,  $C_{ox}$  is the gate oxide capacitance per unit area, *L* is the gate length,  $V_{GS}$  is the gate voltage,  $V_{TH}$  is the threshold voltage, and  $V_{DS}$  is the drain voltage.



Figure 4. Measured gain with frequency variations.

According to Equations (1) and (2), the transduction in the linear and nonlinear regions is [19,20]

$$g_{m-linear} = \sqrt{2\mu_n \frac{WC_{ox}}{L}} I_{DS-linear}$$
(3)

$$g_{m-nonlinear} = \sqrt{2\mu_n \frac{WC_{ox}}{L}} I_{DS-nonlinear}$$
(4)

where the expression for the carrier mobility is [21]

$$\mu_n(T) = \mu_n(T_0) \left(\frac{T}{T_0}\right)^{-m}$$
(5)

where  $T_0 = 300$  K,  $m = 1.5 \sim 2$ .

According to Equation (5), the  $\mu_n$  degrades with increasing temperature. And according to Equations (3) and (4), it is known that the transconductance of both linear and nonlinear regions is positively related to carrier mobility. Therefore, the transconductance of both linear and nonlinear regions will degrade with increasing temperature. In addition, the transconductance is the gain [19,20]; thus, the LNA's gain is also degraded as the temperature increases. Therefore, the decrease in S21 with increasing temperature decreases carrier mobility with increasing temperature.

We already know that the S21 degrades as the temperature rises. Figure 4 shows that when the temperature change range is the same, the S21 changes at different frequencies are also different. For example, Figure 5 shows the evolution of S21 in the temperature range of -40 °C to 90 °C.

As shown in Figure 5, S21 decreases by 3.54 dB, 3.2 dB, and 3.02 dB for 70 MHz, 230 MHz, and 450 MHz, respectively, when the temperature increases by 130 °C. This indicates that the  $\mu_n$  is temperature-dependent and frequency-dependent.



**Figure 5.** Variation of S21 in the temperature range from -40 °C to 90 °C.

#### 3.2. The Noise Figure (NF)

The noise figure of the LNA as a function of temperature is shown in Figure 6. As shown in Figure 6, the noise coefficient of the LNA increases with temperature; this means that the noise performance of the LNA degrades with increasing temperature. In addition, the noise figure of the LNA varies with frequency rather than monotonically. That is, the noise figure of the LNA increases or decreases with increasing frequency. This indicates that the noise figure of the LNA is not only a function of temperature, but also a function of frequency.



Figure 6. Measured noise figure with frequency variations.

The following is a specific discussion of the causes of the increase in the noise coefficient of the LNA with increasing temperature. The expression of the  $NF_{min}$  of LNA is [22]

$$NF_{\min} = 1 + 2\pi K (C_{gs} + C_{gd}) \sqrt{\frac{R_s + R_d}{g_m}}$$
 (6)

where *K* is the Fukui constant,  $C_{gs}$  and  $C_{gd}$  are the gate-source and gate-drain capacitance,  $R_s$  and  $R_d$  are the source and drain resistance, and  $g_m$  is the transconductance.

The transconductance degrades with increasing temperature. In addition, the source/drain resistance also increases with temperature. Therefore, according to Equation (6), the increase in source/drain resistance and the degradation of the transconductance will increase the NF<sub>min</sub> of the LNA as the temperature increases. Consequently, there is an increase in the LNA noise figure with the temperature rise. This indicates that the increase in source/drain resistance and the transconductance degradation are the two main reasons for the rise in the noise figure with increasing temperature.

It is already known from Figure 6 that the noise figure of the LNA increases with temperature. This is because the NF changes differently for different frequencies in the same temperature variation range. For example, Figure 7 shows the variation of the noise figure to varying frequencies in the field of -40 °C to 90 °C. As shown in Figure 7, the noise figure at 50 MHz, 270 MHz, and 450 MHz increases by 1.22 dB, 0.74 dB, and 1.02 dB, respectively, when the temperature increases from -40 °C to 90 °C. This also shows that the  $\mu_n$  is not only temperature-dependent but also frequency-dependent.



**Figure 7.** Variation of the NF in the temperature range from -40 °C to 90 °C.

#### 4. On-Chip Temperature Compensation for LNAs

A circuit structure for multistage PA temperature compensation was proposed in the literature [23]; based on this structure, we propose a temperature compensation circuit for stacked PAs [24]. Considering the simple structure of this compensation circuit and our existing research base, in this subsection, we try to use the temperature compensation circuit structure for the multistage PA proposed in the literature [23] for the compensation of S21 and NF of the LNA. Furthermore, we explore whether the compensation circuit structure presented in [23] can be used for the temperature compensation of other microwave/RF circuits such as LNAs in addition to multistage PAs. The structure of the circuit used for LNA temperature compensation circuit in the literature [23], as shown in Figure 8. As shown in Figure 8, this compensation circuit consists of a diode (D<sub>1</sub>) and two resistors (R and R<sub>1</sub>).



Figure 8. Temperature compensation circuit structure for the LNA [23].

Since the circuit structure used is the same as that of the literature [23], the temperature compensation principle of this temperature compensation circuit for the LNA is also the same as that of the literature [23]. Therefore, to avoid repetition, it is not presented again.

According to the literature [23], when the temperature increases from  $T_L$  to  $T_H$ , Equations (1) and (2) can be expressed, respectively, as

$$I_{DS-linear} = \frac{W\mu_n C_{ox}}{2L} \Big[ 2((V_{GS} + \Delta V_{g1}) - V_{TH}) V_{DS} - V_{DS}^2 \Big]$$
(7)

$$I_{DS-nonlinear} = \frac{W\mu_n C_{ox}}{2L} \left( \left( V_{GS} + \Delta V_{g1} \right) - V_{TH} \right)^2 \tag{8}$$

where  $\Delta V_{g1}$  is the variation of  $V_{g1}$  between two temperatures ( $T_H$  and  $T_L$ ).

According to Equations (7) and (8), the  $I_{DS}$  will increase with the increase of  $\Delta V_{g1}$ . Furthermore, from Equations (3) and (4), the transconductance is proportional to the drain current; i.e., it increases with the increase of the  $I_{DS}$ . This means that the temperature compensation circuit increases the transconductance with the rise in the  $\Delta V_{g1}$ ; thus, the temperature compensation of the transconductance is realized. That is, the compensation of S21 is realized.

Figure 9 gives the simulation results of S21 with and without compensation, from which when the temperature increases from -40 °C to 90 °C, S21 changes by 0.4 dB with compensation, while S21 changes by 3.5 dB without compensation; this indicates that the compensation circuit is effective in compensating S21 with a temperature change.



Figure 9. Simulation results of S21 with and without compensation.

From Equation (6), NF will decrease with the increase of the transconductance. Therefore, under the temperature compensation circuit, NF will reduce with the rise of the  $\Delta V_{g1}$ ; thus, this will achieve the temperature compensation of NF. The simulation results for the NF with and without compensation are shown in Figure 10. It can be seen from this that the NF with temperature compensation varies less with temperature, while the NF without temperature compensation increases with temperature. Specifically, when the temperature increases from -40 °C to 90 °C, the NF changes by 0.02 dB with temperature compensation, while the NF changes by 0.3 dB without temperature compensation. This indicates that the temperature compensation circuit effectively compensates for the NF degradation with temperature increase.



Figure 10. Simulation results of the NF with and without compensation.

The above is the working principle of the temperature compensation circuit proposed in this subsection, mainly to increase the transconductance by increasing the gate voltage to achieve the compensation of S21 and NF with temperature change. The simulation results in Figures 9 and 10 show that the temperature compensation circuit structure proposed in the literature [23] applies not only to the temperature compensation of PA, but also to the temperature compensation of LNA.

#### 5. Conclusions

This paper investigates the key specifications of LNAs, such as gain and noise figures, from an experimental point of view at different temperatures using a CMOS 50 MHz–450 MHz LNA as an example. The S21 decreases with temperature increase while the noise figure increases. Furthermore, it is found that one of the leading causes of the degradation of the gain and noise characteristics is the degradation of the transconductance. The results can guide temperature-compensated circuit design to complement the degradation of the specification. On the other hand, it is also proved that the temperature compensation circuit structure proposed in the literature [23] applies to the temperature compensation of LNAs.

The specification degradation of the LNA is not only related to temperature, but also to humidity, high- and low-temperature shock, and time. Therefore, future work in this paper will consider the relationship between the specification degradation of the LNA with humidity, the number of high- and low-temperature shocks, and time. **Author Contributions:** Conceptualization, S.Z. and J.W.; methodology, S.Z. and J.W.; software, S.Z.; validation, S.Z. and J.W.; formal analysis, J.W.; investigation, S.Z.; resources, J.W.; data curation, S.Z.; writing—original draft preparation, S.Z.; writing—review and editing, J.W.; visualization, S.Z.; supervision, J.W.; project administration, J.W.; funding acquisition, J.W. All authors have read and agreed to the published version of the manuscript.

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### References

- 1. Zhang, Y.; Yuan, J. CMOS Transistor Amplifier Temperature Compensation: Modeling and Analysis. *IEEE Trans. Device Mater. Reliab.* **2012**, *12*, 376–381. [CrossRef]
- Jayaraman, K.; Khan, Q.; Chi, B.; Beattie, W.; Wang, Z.; Chiang, P. A self-healing 2.4GHz LNA with on-chip S11/S21 measurement/calibration for in-situ PVT compensation. In Proceedings of the 2010 IEEE Radio Frequency Integrated Circuits Symposium, Anaheim, CA, USA, 23–25 May 2010; pp. 311–314.
- 3. Shin, S.; Leung, M.C.; Hsiao, S. A temperature variation compensated 60-GHz low-noise amplifier in 90-nm CMOS technology. In Proceedings of the Asia-Pacific Microwave Conference 2011, Melbourne, VIC, Australia, 5–8 December 2011; pp. 211–214.
- 4. Nikandish, G.; Yousefi, A.; Kalantari, M. A Broadband Multistage LNA With Bandwidth and Linearity Enhancement. *IEEE Microw. Wirel. Compon. Lett.* 2016, 26, 834–836. [CrossRef]
- Choi, H.-W.; Kim, C.-Y.; Choi, S. 6.7–15.3 GHz, High-Performance Broadband Low-Noise Amplifier With Large Transistor and Two-Stage Broadband Noise Matching. *IEEE Microw. Wirel. Compon. Lett.* 2021, 31, 949–952. [CrossRef]
- Zhang, T.; Shuai, Y. Design of a broadband LNA for a ship receiver system. In Proceedings of the 2018 IEEE International Symposium on Electromagnetic Compatibility and 2018 IEEE Asia-Pacific Symposium on Electromagnetic Compatibility (EMC/APEMC), Suntec City, Singapore, 14–18 May 2018; pp. 631–636.
- Memioglu, O.; Gundel, A. A High Linearity Wide Bandwidth GSM/WCDMA/LTE Base Station LNA MMIC with Ultra Low Noise Figure. In Proceedings of the 2018 18th Mediterranean Microwave Symposium (MMS), Istanbul, Turkey, 31 October–2 November 2018; pp. 198–201.
- Kobayashi, K.W.; Kumar, V.; Xie, A.; Jimenez, J.L.; Beam, E.; Ketterson, A. A baseband-65GHz High Linearity-Bandwidth GaN LNA using a 1.7A/mm High Current Density ScAlN based GaN HEMT Technology. In Proceedings of the 2021 IEEE MTT-S International Microwave Symposium (IMS), Atlanta, GA, USA, 7–25 June 2021; pp. 772–775.
- Bierbuesse, D.; Negra, R. 60 GHz variable Gain & Linearity Enhancement LNA in 65 nm CMOS. In Proceedings of the 2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Los Angeles, CA, USA, 4–6 August 2020; pp. 163–166.
- Xu, X.; Schumann, S.; Ferschischi, A.; Finger, W.; Carta, C.; Ellinger, F. A 28 GHz and 38 GHz High-Gain Dual-Band LNA for 5G Wireless Systems in 22 nm FD-SOI CMOS. In Proceedings of the 2020 15th European Microwave Integrated Circuits Conference (EuMIC), Utrecht, The Netherlands, 10–15 January 2021; pp. 77–80.
- Jang, S.; Nguyen, C. A High-Gain Power-Efficient Wideband V-Band LNA in 0.18-μm SiGe BiCMOS. *IEEE Microw. Wirel. Compon.* Lett. 2016, 26, 276–278. [CrossRef]
- Venkatesh Murthy, B.T.; Singh, N.K.; Jha, R.; Kumar, N.; Kumar, R. Ultra Low Noise Figure, Low Power Consumption Ku-Band LNA with High Gain for Space Application. In Proceedings of the 2020 5th International Conference on Communication and Electronics Systems (ICCES), Coimbatore, India, 10–12 June 2020; pp. 80–83.
- Sawayama, Y.; Morishita, T.; Komoku, K.; Itoh, N. Dual-Band Concurrent LNA with Low Gain Deviation and Low Noise Figure. In Proceedings of the 2020 IEEE Asia-Pacific Microwave Conference (APMC), Hong Kong, China, 8–11 December 2020; pp. 1006–1008.
- Gupta, A.; Kushwaha, A.; Mehra, G. A 2.4 GHz Low Power and High Gain LNA in 0.18μm CMOS for Radio Applications. In Proceedings of the 2021 7th International Conference on Advanced Computing and Communication Systems (ICACCS), Coimbatore, India, 19–20 March 2021; pp. 1390–1393.
- Musenov, R.Y.; Yanakova, E.S. The S- and C- band Low-power CMOS LNA Using the Current-reuse Technique. In Proceedings of the 2021 IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering (ElConRus), Moscow, Russia, 26–29 January 2021; pp. 2714–2717.
- Liu, J.; Shan, W.; Yao, Q. Development of a Low-power Consumption Cryogenic MMIC LNA for Immediate Connection with an SIS Mixer. In Proceedings of the 2019 IEEE MTT-S International Wireless Symposium (IWS), Guangzhou, China, 19–22 May 2019; pp. 1–3.

- 17. Yang, C.; Feng, F. Multi-Step-Ahead Prediction for a CMOS Low Noise Amplifier Aging Due to NBTI and HCI Using Neural Networks. *J. Electron. Test.* **2019**, *35*, 797–808. [CrossRef]
- Borremans, J.; Wambacq, P.; Soens, C.; Rolain, Y.; Kuijk, M. Low-Area Active-Feedback Low-Noise Amplifier Design in Scaled Digital CMOS. *IEEE J. Solid-State Circuits* 2008, 43, 2422–2433. [CrossRef]
- 19. He, Z.; Zhou, S.H.; Nie, M.N. Experimentally investigating the performance degradations of the CMOS PA at different temperatures. *AIP Adv.* **2021**, *11*, 115205. [CrossRef]
- 20. Razavi, B. Design of Analog CMOS Integrated Circuits; McGraw Hill Higher Education: New York, NY, USA, 2003.
- Gray, P.R.; Hurst, P.J.; Lewis, S.H.; Meyer, R.G. *Analysis and Design of Analog Integrated Circuits*; Wiley: New York, NY, USA, 2001.
   Gao, L.; Wagner, E.; Rebeiz, G.M. Design of E- and W-Band Low-Noise Amplifiers in 22-nm CMOS FD-SOI. *IEEE Trans. Microw.*
- *Theory Tech.* **2020**, *68*, 132–143. [CrossRef] 23. Yamauchi, K.; Iyama, Y.; Yamaguchi, M.; Ikeda, Y.; Urasaki, S.; Takagi, T. X-band MMIC power amplifier with an on-chip
- temperature-compensation circuit. IEEE Trans. Microw. Theory Tech. 2001, 49, 2501–2506. [CrossRef]
- 24. Zhou, S.; Wei, S.; Wang, J. On-Chip Temperature Compensation for Small-Signal Gain Variation Reduction. *Micromachines* **2022**, 13, 1101. [CrossRef] [PubMed]