Editorial

Editorial for the Special Issue on Advanced Interconnect and Packaging

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Unlike transistors, the continuous downscaling of feature size in CMOS technology leads to a dramatic rise in interconnect resistivity and concomitant performance degradation. At nanoscale technology nodes, interconnect delay and reliability become the major bottlenecks faced by modern integrated circuits. To resolve these interconnect problems, various emerging technologies, including airgap, nanocarbon, optical, and through-silicon via (TSV), have been proposed and investigated. For example, by virtue of TSV technology, dies can be stacked to increase the integration density. More importantly, 3D integration and packaging also offer the most promising platform to implement "More-than-Moore" technologies, providing heterogenous materials and technologies on a single chip.

This Special Issue seeks to showcase research papers on new developments in advanced interconnect and packaging, i.e., on the design, modeling, fabrication, and reliability assessment of emerging interconnect and packaging technologies. Additionally, there are two interesting papers on carbon nanotube interconnects and interconnect reliability issues.

In particular, Liu et al. successfully realize the thermocompression bonding of Pt–Pt metal electrodes through process exploration and form a packaging interconnection that meets the requirements [1]. Sun et al. achieve low-temperature assembly by reflowing 13.5Sn–37.5Bi–45In–4Pb quaternary eutectic solder paste and a SAC 305 solder ball together at 140 °C for 5 min [2]. Liu et al. investigate the flow process of nano glass powder melted at a high temperature [3]. To reduce the wettability of the glass paste on the Au electrode, they grow a silicon dioxide isolation layer on the surface of golden lead via chemical vapor deposition. Wang et al. investigate the chip-level hermetic package for a high-temperature graphene pressure sensor and demonstrate that the combination of Cu–Sn and Au–Au is extremely suitable for hermetic packaging [4]. Wu et al. provide theoretical support for the application of thin coatings at high temperatures and in harsh environments [5].

Wang et al. study the electrical performance of graphene-based on-chip spiral inductors by virtue of a physics-based equivalent circuit model [6]. Kim et al. propose a novel interposer channel structure with vertical tabbed vias to achieve high-speed signaling in high-bandwidth memory and demonstrate that the proposed channel structure could reduce dynamic power consumption [7]. Kim designs noise suppression structures that generate an electromagnetic bandgap and studies the mechanism of the proposed structure based on dispersion analysis [8]. Zheng et al. study the average power handling capability of corrugated slow-wave transmission lines [9]. Du et al. develop a mathematical degradation model for evaluating the degradation of vacuum packaged MEMS sensors and perform a temperature-accelerated test of MEMS gyroscopes with different vacuums [10]. Zhao et al. introduce recent studies on the physics-based modeling of the electromigration aging of interconnects [11].

Pan et al. present a novel wideband bandpass filter based on the integration of a substrate-integrated waveguide and a spoof surface plasmon polariton [12]. Wei et al. present a new method for the analytical approximation of spatial current/field profiles of frequency-selective surfaces and demonstrate that the transmission line loss has little

Citation: Zhao, W.-S. Editorial for the Special Issue on Advanced Interconnect and Packaging. *Micromachines* **2023**, *14*, 171. https://doi.org/10.3390/mi14010171

Received: 6 January 2023
Accepted: 8 January 2023
Published: 10 January 2023

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influence on the current distribution [13]. Bai et al. propose a broadband frequency-selective rasorber based on spoof surface plasmon polaritons [14]. Tian et al. investigate the deadbeat current controllers for an isolated bidirectional dual-active-bridge dc–dc converter, including in the peak current mode and middle current mode [15]. Kuo et al. develop a flexible blood oxygen sensing system with a 3 × 3 array and use a flip chip package to integrate the sensing chip [16]. Finally, Xu et al. review the advantages, recent developments, and dilemmas of carbon nanotube-based interconnects from the perspective of different interconnect lengths and through-silicon via applications [17].

To conclude, I would like to take this opportunity to thank all the authors for submitting their papers to this Special Issue, as well as the reviewers for the effort and time they expended to improve the quality of the published papers. I also want to recognize Mr. Dikies Zhang from the *Micromachines* publishing office for his endless assistance and help in disseminating this Special Issue.

In view of the success reached in terms of the number and quality of papers published, we plan to open a second Volume where we hope to continue the conversation regarding the latest advances in interconnect and packaging.

Funding: This research was funded by National Natural Science Foundation of China (grant number 62222401) and Zhejiang Provincial Natural Science Foundation (grant number LXR22F040001).

Conflicts of Interest: The authors declare no conflict of interest.

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