Review

Trap Characterization Techniques for GaN-Based HEMTs: A Critical Review

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Abstract: Gallium nitride (GaN) high-electron-mobility transistors (HEMTs) have been considered promising candidates for power devices due to their superior advantages of high current density, high breakdown voltage, high power density, and high-frequency operations. However, the development of GaN HEMTs has been constrained by stability and reliability issues related to traps. In this article, the locations and energy levels of traps in GaN HEMTs are summarized. Moreover, the characterization techniques for bulk traps and interface traps, whose characteristics and scopes are included as well, are reviewed and highlighted. Finally, the challenges in trap characterization techniques for GaN-based HEMTs are discussed to provide insights into the reliability assessment of GaN-based HEMTs.

Keywords: GaN HEMT; trap; characterization methods; DLTS

1. Introduction

Gallium nitride (GaN) high-electron-mobility transistors (HEMTs) possess superior features such as high breakdown voltage, high electron saturation drift velocity, and low ON-resistance, making them highly promising for power device applications [1,2]. Additionally, due to the polarization effect in GaN-based materials, a high-concentration two-dimensional electron gas (2DEG) channel can be formed at the AlGaN/GaN interface of GaN HEMT devices, significantly enhancing carrier mobility. Consequently, the theoretical figure of merit limit of GaN HEMT is higher than that of Si and SiC-based power electronic devices. In recent years, GaN HEMTs have been intensively studied and widely used in RF amplifiers and power electronics systems [3–5].

Despite the many benefits of GaN-based HEMT devices, the presence of traps in the bulk and at the interface can cause stability and reliability issues such as current collapse [6–11], threshold voltage drift [7,12], deterioration of short channel effect [12], and limited microwave power output [8,13], which seriously limit its large-scale applications. Therefore, trap characterization is crucial for achieving better commercial applications of GaN-based HEMT devices, which can provide more insights into the performances of devices as well as more guidelines for the optimization of the device structure and manufacturing processes to improve both the capability and reliability of GaN HEMTs. In recent decades, several techniques such as low-frequency noise (LFN), frequency dispersion properties, and deep-level transient spectroscopy (DLTS) have been developed to characterize the locations, types, concentrations, energy levels, and capture cross-sections of traps in GaN HEMTs, which are also applicable to novel GaN HEMT structures [14] and GaN diodes [15], p-n junctions [16], etc.

2. Types and Impacts of Traps

Various traps found in GaN HEMTs are classified in this chapter. As illustrated in Figure 1, the main traps in GaN HEMTs can be classified into interface traps and bulk traps according to the locations; the former ones are located mainly between the AlGaN/passivation layer, GaN/Substrate, and AlGaN/GaN heterojunction, while the latter ones are located primarily in the GaN buffer layer and AlGaN barrier layer. In addition, for metal-insulator-semiconductor heterojunction field-effect transistors (MIS-HEMT), interface defects also exist at the interface between AlGaN and insulation.
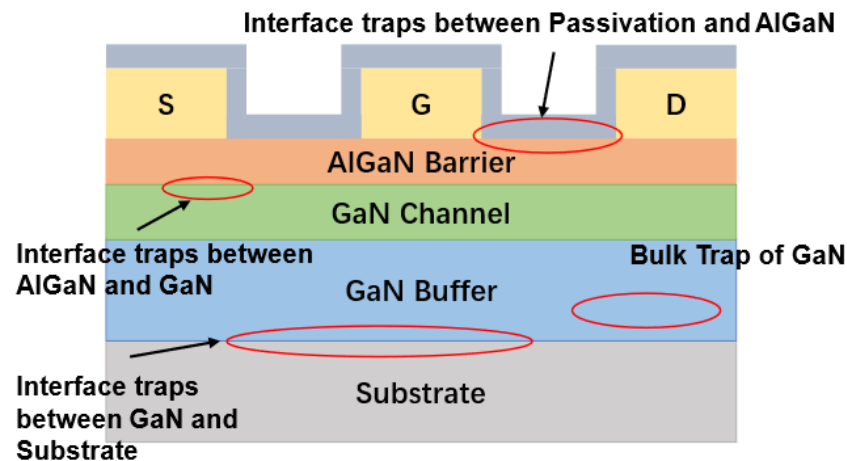

Figure 1. The locations of traps in GaN HEMTs.

The AlGaN/GaN interface and semiconductor/insulator interface traps are mainly caused by dislocations and defects generated during the growth of the material and the manufacturing processes of the device [17,18]. The reasons for the formation of bulk defects in the AlGaN barrier layer and GaN buffer layer are multifaceted. Firstly, buffer traps are introduced because of the high-resistance characteristics exhibited by the GaN buffer layer, which are usually achieved through C or Fe impurity compensation [19–23]. The 2DEG concentration of a device may be affected by the aforementioned traps [24], which, in turn, affects parameters such as current density and threshold voltage [25]. Secondly, V_{Ga}-impurity, V_N-impurity, Mg-H complexes, V_N-Mg complexes, etc., also form point defects in GaN materials, introducing deep-level traps. In addition, although there has been significant development in GaN-on-GaN homoepitaxial growth and device fabrication [26,27], a considerable portion of devices still use heteroepitaxial substrates, in which large amounts of dislocations and defects are caused by lattice mismatch during the epitaxial growth process, forming deep-level trap states in the bandgap.

The energy levels, positions, and corresponding characterization methods of the traps identified in GaN HEMT devices are shown in Figure 2 [28–66]. From this figure, it can be observed that there are traps located near the energy band of 0.6 eV in SI-GaN/UID-GaN/Si-GaN/Mg GaN, which is said to be attributed mainly to the point defects in GaN in some papers, but there are other reports saying that the source of this type of trap may be caused by V_N-impurity, Mg/Si-H complexes, and so on. The 0.7 eV trap near the AlGaN/GaN interface is generally believed to be caused by the spreading defects in the AlGaN/GaN heterostructure. And, beyond that, there are traps located around Ec-0.6 eV at the passivation layer and the semiconductor interface, which may be caused by the high Ga-O components near the passivation layer and semiconductor interface.
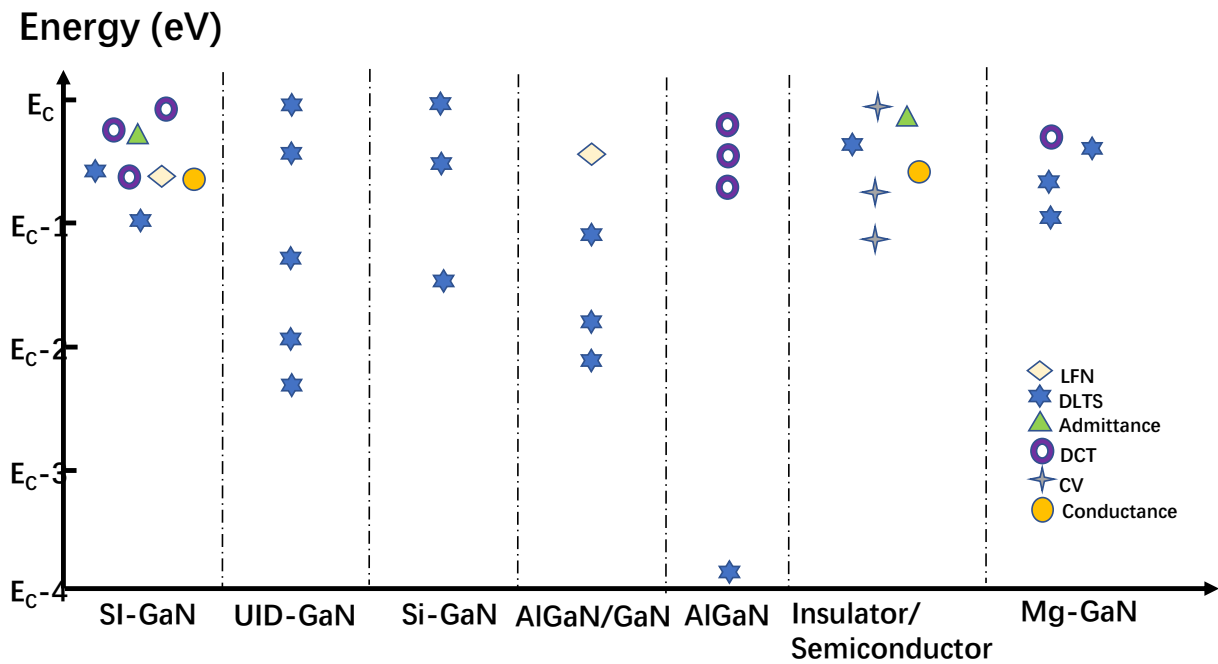
Figure 2. Energy levels and positions of traps in GaN HEMTs.

From the perspective of characterization methods, DCT, LFN, and low-frequency output admittance methods are used more frequently to characterize traps in semiconductor bodies, while other methods such as C-V and dispersion of conductance output are mainly used to characterize the traps at semiconductor interfaces. It is also illustrated that DLTS can characterize traps on the surface and in vivo based on their modes. In addition, it can be observed that DCT is usually used to characterize shallower traps, while DLTS can characterize deeper-level traps. DCT, a method that is used to characterize shallower traps, is different from DLTS since DLTS is usually used to characterize deeper traps.

From the perspective of trap location, DCT, DLTS, and C-V can identify the trap location through different voltage biases, and the conductivity method can measure semiconductor/insulator interface traps in MOS structures. As for LFN and transconductance methods, although they cannot identify trap locations, they can be used together with other characterization methods to comprehensively analyze traps.

3. Characterization Methods of Bulk Traps

3.1. Drain Current Transient

The drain current transient (DCT) test involves applying large positive V_{ds} bias, large negative V_{gs} bias, or both to measure the change in I_{DS} [48–56]. The transient current I_{DS} can be expressed as

$$I_{DS}(t) = \sum \Delta I_i \exp\left(-\frac{t}{\tau_i}\right) + I_\infty,\tag{1}$$

where ΔI_i is the amplitude, τ_i is the time constant of the trap, and I_∞ is the current which is at a steady state [51]. The Bayesian deconvolution method can be used to obtain the time constant of traps (τ_n) and the energy level and cross-section of the trap can be derived from Arrhenius plots:

$$\ln(\tau_n T^2) = -\frac{E_a}{k_B T} + \ln(\sigma_n \gamma_n),\tag{2}$$

where σ_n is the electron capture cross-section, γ_n contains the density and thermal velocity of electrons, E_a is the trap activation energy, and k_B is the Boltzmann constant [51].

The type of trap can be determined by the peak in the derivative spectrum of DCT where a positive peak represents the existence of an electron trap, while a negative peak shows that there exists a hole trap.

The process of extracting trap parameters with a leakage current response is illustrated in Figure 3. The change of I_{DS} at different temperatures during trap launch, the time constant of the trap extracted through the Bayesian convolution method, and the Arrhenius plot extracted from the transient curve are shown in Figure 3a, Figure 3b, and Figure 3c, respectively.
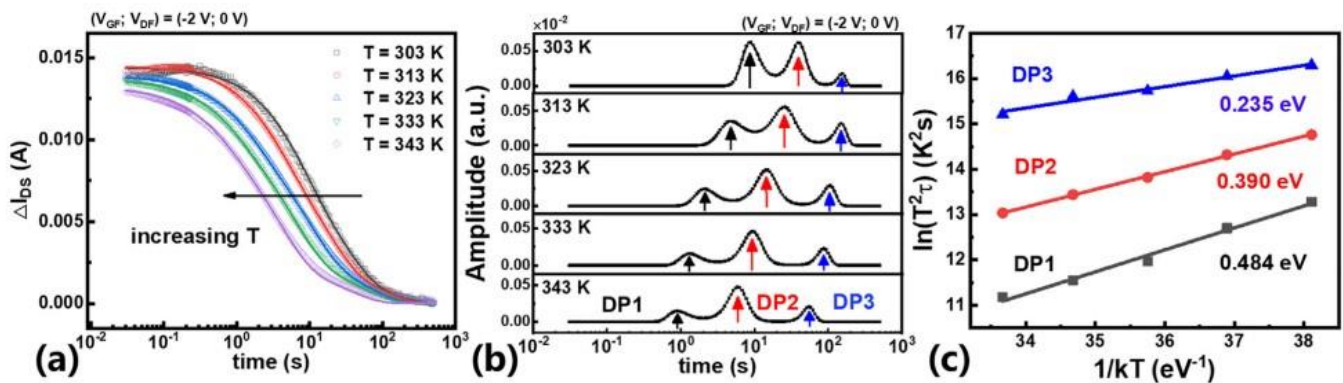

Figure 3. (Color online.) (**a**) The actual detrapping transient curves with different temperatures. (**b**) The time constant spectra at different temperatures. (**c**) The Arrhenius plots and the corresponding energy levels. Reprinted from [51], with the permission of AIP Publishing.

The physical location of the traps can still be determined by other means, although the inherent spatial sensitivity cannot be provided by this method. Different filling pulse conditions with different combinations of the gate-source voltage (V_{gs}) and the gate-source voltage (V_{ds}) stress conditions can be used to fill traps in different areas of GaN HEMTs. For instance, filling pulses with a strong negative $V_{gs} < V_{th}$ can cause electrons to fill surface channel regions located beneath the gate area or defects in both the gate electrode and drain regions [67]. The channel capture can be highlighted by applying a strong positive V_{ds} bias and a strong negative V_{gs} bias due to the increase in the electron tunneling in the drain direction. A strong positive V_{ds} bias with $V_{gs} > V_{th}$ can allow electrons to be captured in the barrier layer or buffer layer between the gate and drain, as large positive V_{gs} can scatter hot electrons out of the channel [68]. Therefore, the physical location of traps can be distinguished through DCT tests on a device performed by stress conditions.

The DCT technique is simple and can locate trap positions, but the trap density cannot be quantitatively measured and traps can only be detected with energy levels below 1 eV. Therefore, other approaches are necessary to characterize deep-level traps.

3.2. Low-Frequency Leakage Noise

Low-frequency leakage noise (LFN) is a noise signal generated in the low-frequency range, usually below a few hundred Hz, which reflects the charge and energy-level distribution inside a device. In GaN HEMT devices, the presence of traps affects the device's leakage current and conductivity [69]. A small current noise is generated by traps when a small signal voltage is applied to the device. This noise can be measured by means of low-frequency leakage noise measurement techniques [39,56,60,61]. By analyzing the noise signals at different frequencies, parameter energy levels and capture cross-sections can be obtained by analyzing the noise signals at different frequencies and extracting the time constants of the G-R. The relationship between output noise and frequency is illustrated in Figure 4a. The measured output drain noise spectral density must be multiplied by the frequency to distinguish G-R noise from other measurement noise sources, as shown in Figure 4b. The cutoff frequency of traps can be extracted at different temperatures and then the trap parameters can be extracted by using the Arrhenius equation in Figure 4c.
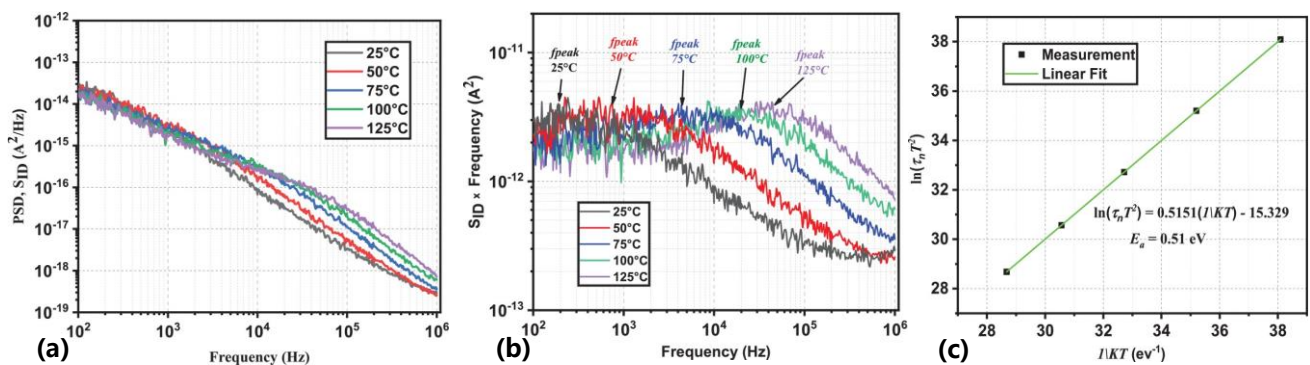
Figure 4. (Color online.) (**a**) Output noise PSD versus frequency. (**b**) Output noise PSD multiplied by frequency measured. (**c**) Extracted Arrhenius plot using LFN measurement [39].

Compared to DLTS and DCT, LFN has more difficulty in locating traps and lacks quantitative measurements of trap density, but it does not require a large reverse bias voltage to be applied to a device to degrade the de-trapping performance, and it is also capable of detecting traps in small area devices.

3.3. Low-Frequency Output Admittance Measurements

The characterization technique for low-frequency output admittance measurements characterizes traps by measuring the characteristics of their S/Y parameters as a function of frequency [39,57–59,65,70]. Then, the measured parameters can be calculated as equivalent Y_{22} parameters. Due to the influence of traps, the Y_{22} parameter obtained will reach its peak at a certain frequency. This peak will shift towards a higher frequency as the temperature increases. The emission time constant of the trap can be extracted from the peak frequency (f_{peak}) using Equation (3). The parameters of the trap can then be obtained using the Arrhenius equation.

$$f_{\text{peak}} = f_{\text{Imag}[Y_{22}]} = \frac{1}{2\pi\tau_n}, \tag{3}$$

The relationship between the imaginary part of the measured Y_{22} parameter and the frequency is demonstrated in Figure 5a, and the Arrhenius plot of this measurement is shown in Figure 5b.
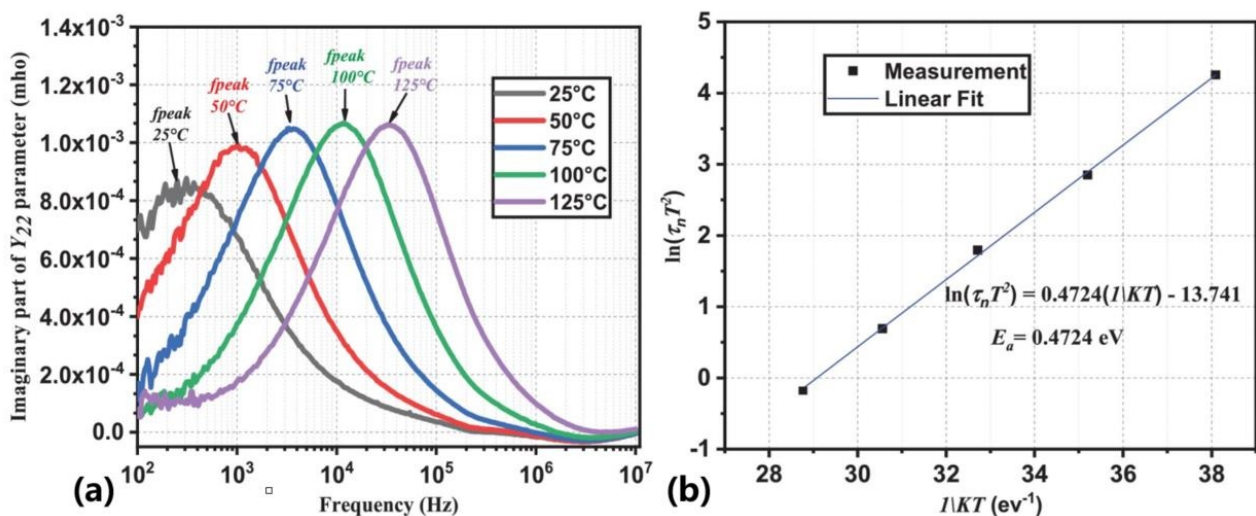

Figure 5. (Color online.) (**a**) Imaginary part of the measured Y_{22}-parameter vs. frequency. (**b**) Extracted Arrhenius plot [39].

In practical applications, the appropriate parameter to represent the dispersion of HEMT traps should be chosen based on specific requirements. Generally, if an analysis of the influence of HEMT traps on the entire system is required, the S parameter should be used as it provides the relative response between input and output ports. On the other hand, if a deeper understanding of the characteristics of HEMT traps is required, the Y parameter may be more suitable as it provides the internal response of the device, including the relationship between voltage and current.

Pulse effects such as voltage stabilization time or unstable temperature are avoided and wide dynamic range and measurement speed are provided in this method [70]. However, only energy levels and capture cross-sections for traps can be obtained through this method.

3.4. DLTS

DLTS has the advantages of being sensitive to measurement, having a wide range of detectable defect energy levels, being able to simultaneously measure both majority and minority carrier traps, and being able to determine trap positions. The processes involved in trap emission and capture during DLTS testing are summarized in Figure 6. In the steady-state condition, as indicated in Figure 6a, the energy level E_T is not occupied by electrons. The Fermi level is forced to shift towards the conduction band when applying a filling pulse bias voltage (V_f), as indicated in Figure 6b, which attracts electrons and consequently weakens the built-in electric field. The trap levels within the depletion region are situated below the Fermi level. Charges captured by traps within the depletion region with energy levels above the Fermi level will be emitted by applying a measurement voltage (V_m) that is more negative than the filling pulse voltage V_f, as shown in Figure 6c. Taking the contribution of thermal emission into account, the trap emission constant can be obtained by measuring the change in capacitance through the DLTS from time t_1 to t_2 after the pulse [71]. As for the determination of the type of trap, the method of identifying the type of peak in the derivative of capacitance versus the time plot can be applied, where a positive peak represents the trap type as an electron and a negative peak represents the trap type as a hole. Taking an n-type semiconductor as an example, the trap density can be calculated from Equation (4).

$$N_T = \frac{\Delta C_{max}}{C_0} \frac{2 N_D r^{\frac{r}{r-1}}}{r-1}, \tag{4}$$

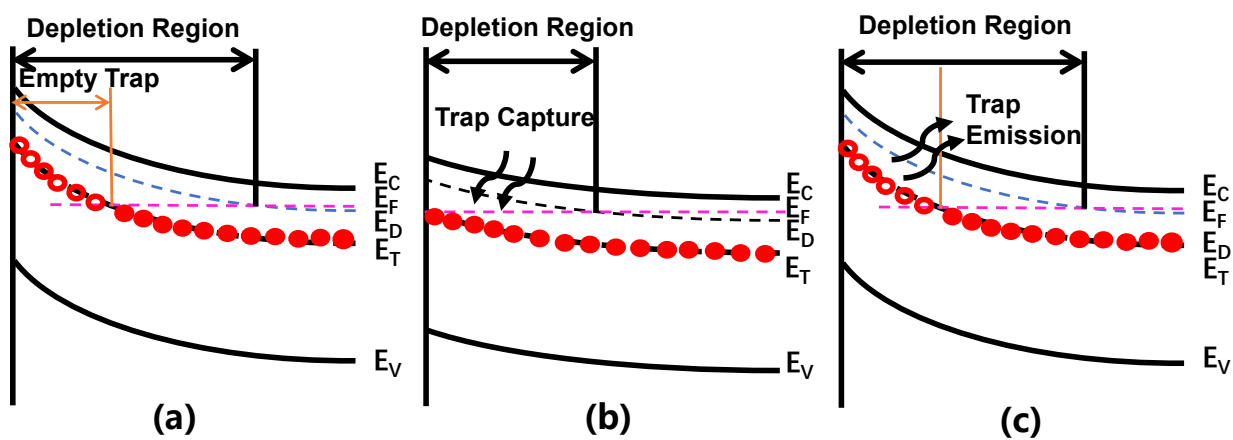where r = t_2/t_1 and C_0 is the steady-state capacitance value.

Figure 6. (Color online.) Schottky diode energy-band diagrams: (**a**) steady-state; (**b**) trap filling state; (**c**) trap emission state.

Capacitor DLTS (C-DLTS) first applies a filling pulse voltage to the device being tested and then measures the change in capacitance after the pulse to characterize the trap [35,72–75]. Traps in the AlGaN barrier layer, GaN channel layer, and buffer layer can be effectively distinguished through C-DLTS. The main principle is based on the state of the 2DEG whereby the gate capacitance primarily comes from the GaN channel layer and buffer layer, while the contribution of the barrier layer to the total capacitance is very small when the 2DEG is depleted, and the depletion region is mainly confined to the AlGaN barrier layer when the 2DEG is accumulated.

It should be noted that the transient values of C-DLTS are usually less than 10% of the total depletion capacitance. Therefore, a sufficient area must be produced to enable experimental resolution ΔC. Furthermore, it is necessary to consider the signal-to-noise ratio of DLTS devices.

Constant drain-current DLTS (CID-DLTS) is applied to obtain specific trap parameters beneath the gate by adjusting the V_{GS} to maintain a constant drain current (I_{DS}), as depicted in Figure 7b. In the gate-controlled mode, the gate voltage is pulsed to V_{fill} in order to populate the deep levels, and the I_{DS} must be kept constant in order to measure the transient response of V_{GS}. The merits of CID-DLTS are that it can detect traps at very low concentrations and capture trap responses with high sensitivity as well as in very short time scales within the device [37,46].
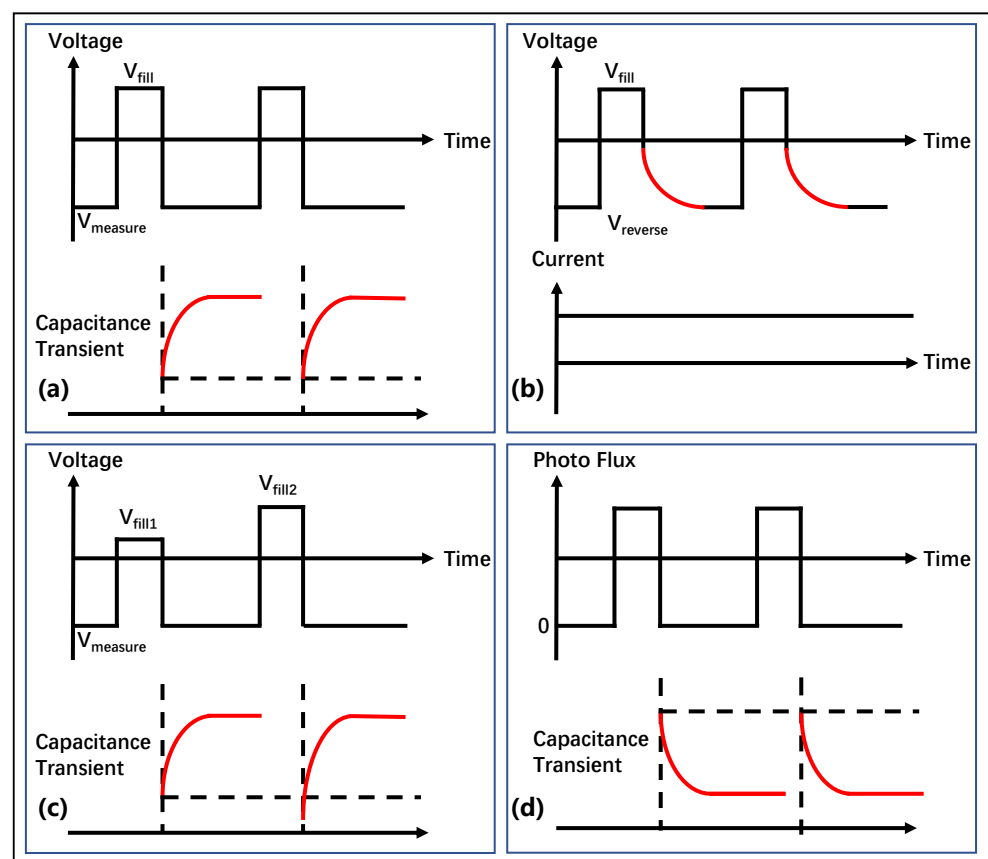
Figure 7. (Color online.) Measurement conditions and curves for (**a**) C-DLTS, (**b**) CID-DLTS, (**c**) D-DLTS, and (**d**) O-DLTS.

Double correlation DLTS (D-DLTS) replaces one amplitude pulse in C-DLTS by using pulses with different amplitudes, as shown in Figure 7c. Although this method makes the experiment and data processing more complex, it facilitates the observation of defect behavior within the space–charge region. Moreover, the variation of defects with depth can be analyzed by changing the pulse amplitude and rate window [76,77].

In DLTS technology, there is also a commonly used drain current DLTS (I-DLTS), whose testing method is highly similar to that of DCT technology, except that DCT observes long-term changes in I_{DS}, while I-DLTS selects a small interval with significant current changes for analysis.

Several of the above DLTS techniques are suitable for detecting majority traps, while the detection of minority traps is difficult. This is due to the very stringent test conditions for minority traps, which require a few traps to be filled and majority traps to be emptied. The optical DLTS (ODLTS) technique has been proposed and validated in order to better characterize minority traps.

ODLTS is a method that uses light pulses as injection pulses to excite electrons and holes, causing carriers to be captured from the trap. Once the light pulse is switched off, the carriers are detrapped so that the capacitance of the device can be measured to obtain the trap parameters. As shown in Figure 7d, photo-generated carriers are generated and captured by traps when a light pulse is applied to a device. After the end of the optical pulse, these captured carriers are de-captured, causing a gradual change in capacitance. Trap parameters can be extracted from capacitance changes at different temperatures after going through the above steps. One of the superiorities of ODLTS is that it overcomes the limitations of DLTS in studying minority traps, with high sensitivity to ultra-deep-level traps [42].

So far, the conventional DLTS method described has the drawback of poor energy resolution. Laplace DLTS (L-DLTS) is an isothermal technique in which the capacitance transients at a fixed temperature are digitized and averaged, and then the defect emission rate is obtained through numerical methods equivalent to the Laplace inverse transform [78]. Compared with traditional DLTS, the main advantage of L-DLTS is a significant improvement in energy resolution, which provides a more precise detection for traps. However, a better signal-to-noise ratio is required in L-DLTS than in conventional DLTS, which makes it less sensitive by a factor of 5.

4. Characterization Methods of Interface Traps

4.1. Constant Capacitance Deep-Level Transient Spectroscopy

Constant capacitance DLTS (CC-DLTS) employs a customized feedback control circuit to maintain a consistent capacitance and regulate voltage to measure voltage transients resulting from trap discharge [66,79,80]. Significant advantages of this method over the traditional DLTS are evident as it ensures a constant depletion of capacitance and SCR width throughout the entire transient process. This feature is particularly beneficial when studying the interface traps in MIS-HEMTs since it keeps the Fermi level constant during the transient response process. Figure 8 illustrates the process and principle of CC-DLTS for measuring MIS HEMT interface traps.
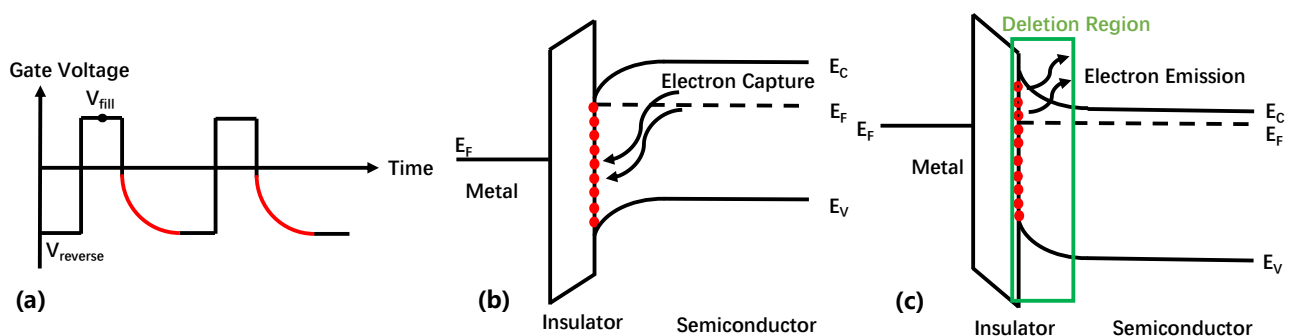

Figure 8. (Color online.) (**a**) The process of CC-DLTS measuring MIS HEMT interface traps. Energy-band diagrams for an MIS HEMT on an n-type semiconductor for (**b**) pulsed accumulation bias and (**c**) nonequilibrium depletion bias.

As shown in Figure 8a, the MIS-HEMT is biased at a negative pressure $V_{reverse}$, and a depletion capacitor is established at $V_{reverse}$. Following that, a pulsed filling voltage referred to as V_{fill} is employed to transition the device into an accumulation state. Throughout this phase, electrons are introduced and occupy the interface/oxide states, as demonstrated in Figure 8b. After the filling pulse, the device returns to the depletion state, and the traps emit electrons. The depletion bias is used to maintain a constant capacitance, which means maintaining an almost-fixed SCR. At this condition, the change in bias voltage is reflected by the release process of interface traps, and the energy and density of the traps can be extracted from $V_{ds}(t)$. Equation (5) allows for the calculation of the interface state density (N_{it}).

$$N_{it} = \int_{E_{FR}}^{E_{FP}} N_{SS}(E) \, (1 - \exp(\frac{-t_P}{\tau_C(E)})) dE,$$ (5)

It involves the density of detected interface states ($N_{SS}(E)$), the Fermi level at the gate bias of UR (E_{FP}), the Fermi level at the gate bias of UP (E_{FR}), and the capture time constants ($\tau_C(E)$) associated with the interface states [79].

Nevertheless, CC-DLTS has a slow response due to the influence of the feedback circuit, but it is still highly sensitive and suitable for measuring interface traps [81–84].

4.2. Quasi-Static C-V Measurement

Quasi-static C-V (QSCV) testing is the process of testing the C-V curve of a device under quasi-static and high-frequency conditions. The C-V curve obtained at high frequencies is generally considered to be the ideal curve without interface traps, whereas the C-V curve changes in response to interface traps at low frequencies. The density of interface traps can be determined by comparing the C-V curves measured at quasi-static and high frequencies (HFCV) using Equation (6) [85,86].

$$D_{it} = \int_{V < V_{th}}^{V_G} (C_{QSCV} - C_{HFCV}) dV / e,$$ (6)

Figure 9 demonstrates the CV testing of MIS diodes, with 10 kHz selected as the high frequency and 1 Hz as the lowest quasi-static state.
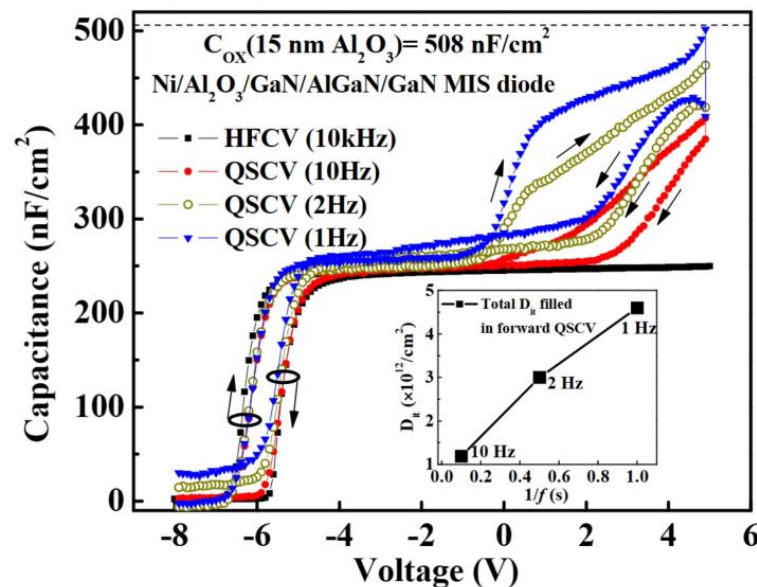

Figure 9. (Color online.) CV characteristics measured at 10, 2, 1, and 10 kHz of Ni/Al₂O₃/GaN/AlGaN/GaN MIS diodes. Reproduced with permission from [85]. Copyright 2012, Wiley.

Quasi-static C-V measurement can provide not only the interface trap charge density but also the determination of the trap energy level and capture cross-section.

4.3. Dispersion of Conductance Output

The dispersion of conductance output is a highly sensitive technique for characterizing interface defect density, which is capable of detecting interface defects on orders of 10^{10} cm^{-2}/eV or lower [63,64,87].

The equivalent circuit for measuring MOS interface traps using the dispersion of conductance output method is shown in Figure 10a, where C_{OX} is the oxide layer capacitance, C_S is the semiconductor capacitance, and C_{it} is the interface trap capacitance. The charge loss caused by the trap capture emission is represented by R_{it}. By circuit transformation, Figure 10b can be obtained, where C_P and G_P are represented by the Equations (7) and (8):

$$C_P = C_S + \frac{C_{it}}{1+(\omega\tau_{it})^2}, \tag{7}$$

$$\frac{G_P}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}}\ln\left[1+(\omega\tau_{it})^2\right], \tag{8}$$

Here, $\tau_{it} = C_{it}R_{it}$. By plotting the G_P/ω-ω curve, the trap density D_{it} and the trap time constant can be extracted from the peak of the curve and the frequency corresponding to the peak, respectively.
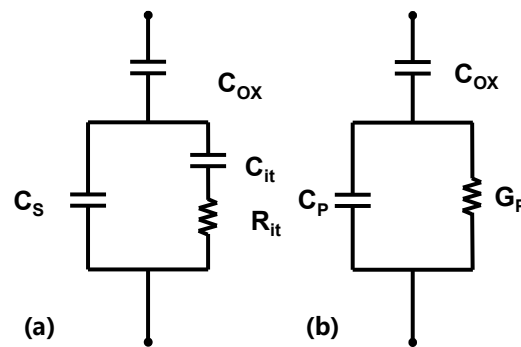

Figure 10. (**a**) The equivalent circuit of MOS. (**b**) Simplified circuit of (**a**).

The conductivity method is highly sensitive, but requires operation over a wide frequency range and is therefore slow to measure [87].

4.4. Single-Pulse Charge Pump

To characterize the interface trap density, a technique known as single-pulse charge pump (SPCP), a method of applying a pulse voltage to gates, can be applied on devices. The SPCP measurement process involves applying a high enough pulse to the gate when the gate voltage is small [88,89]. As the rising edge of the pulse advances, channel electrons begin to accumulate and, subsequently, a portion is captured by the interface trap. At the beginning of the falling edge, the trapped electrons cannot respond quickly due to the long trap time constant. As a result, a difference in current between rise time and fall time occurs, which determines the interface trap density, as shown in Equations (9) and (10):

$$Q_{it} = \int \left(I_{tcp,RISE} - I_{tcp,FALL}\right)dt, \tag{9}$$

$$Q_{it} = qN_{it}, \tag{10}$$

where $I_{tcp,RISE}$ and $I_{tcp,FALL}$ are CP current during rise time and fall time, respectively.

SPCP is less susceptible to interference from gate leakage and well characterized for traps with recovery times within 100 μs [89]. However, except for the value of the interface trap density, other parameters cannot be determined.

5. Conclusions and Outlook

The characterization of GaN HEMT traps is a complex and challenging task that requires advanced experimental techniques and sophisticated theoretical models. Although considerable advancements have been made in this domain, numerous unanswered questions and technical challenges remain, necessitating further exploration to comprehensively understand the characteristics and dynamics of these traps.

A significant obstacle arises from the restrictions imposed by existing measurement techniques. This review focuses on the principles and processes of characterizing traps using electrical, optical, and junction capacitance methods, which have already been widely used to probe traps in GaN HEMTs. However, these techniques have their own drawbacks, such as low sensitivity, poor spatial resolution, and limited frequency range. Furthermore, some of these techniques require special sample preparations or expensive equipment, which can limit their accessibility and practicality. The scope and characteristics of each characterization technique are summarized in Table 1.

Table 1. The range of applications and characteristics of characterization methods.

Methods	Range of Application	Sensitivity	Speed	Non-Destructiveness	Characteristics
DCT	Bulk trap	High	Low	No	Easily interferes with leakage current
LFN	Bulk trap	High	Fast	Yes	Easily interferes with noise
Low-frequency output admittance	Bulk trap	Low	Fast	Yes	Wide range
C-DLTS	Bulk trap	High	Low	No	Wide range
CID-DLTS	Bulk trap	High	Low	No	Complex
D-DLTS	Bulk trap in the SCR	High	Low	No	Complex
ODLTS	Bulk trap	High	Low	No	Measures minority carrier traps
CC-DLTS	Interface trap with high concentrations	High	Low	No	Complex
QSCV	Interface trap with high concentrations	Low	Fast	Yes	Energy levels and capture cross-sections cannot be obtained
Dispersion of conductance	Interface trap	Most high	Low	Yes	Wide frequency range
SPCP	Interface trap	High	Fast	Yes	Energy levels and cross-sections unknown

Another challenge is related to the characterization of interface traps. The characterization of GaN HEMT interface traps is mostly applicable to MIS HEMT, while the interface traps of conventional HEMT structures are difficult to measure due to the presence of MS junctions.

To overcome these challenges, further optimizations and innovations in characterization techniques are needed. The characterization of GaN HEMT traps will continue to be a vibrant field, with many exciting opportunities, such as the new measurement techniques that can provide higher sensitivity and resolution a and wider frequency range while reducing the cost and complexity of further research and developments. Moreover, by integrating multiple measurement techniques and theoretical models, complementary and consistent information about traps can be obtained.

In conclusion, the characterization of GaN HEMT traps is a challenging and rewarding task that is critical for improving device performance and reliability. With continuous advancements in measurement techniques and theoretical models, it can be anticipated that profound understandings of the characteristics and dynamics of these traps can be further unlocked so that the full potential of traps for future applications can be realized. This

knowledge will enable us to enhance the stability and reliability of GaN HEMTs, broaden their range of applications, and unleash their complete potential for future utilization.

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Ikeda, N.; Niiyama, Y.; Kambayashi, H.; Sato, Y.; Nomura, T.; Kato, S.; Yoshida, S. GaN Power Transistors on Si Substrates for Switching Applications. *Proc. IEEE* **2010**, *98*, 1151–1161. [CrossRef]
2. Lee, F.C.; Li, Q. High-Frequency Integrated Point-of-Load Converters: Overview. *IEEE Trans. Power Electron.* **2013**, *28*, 4127–4136. [CrossRef]
3. Kumar, V.; Lu, W.; Khan, F.A.; Schwindt, R.; Kuliev, A.; Simin, G.; Yang, J.; Khan, M.A.; Adesida, I. High performance 0.25 μm gate-length AlGaN/GaN HEMTs on sapphire with transconductance of over 400 mS/mm. *Electron. Lett.* **2002**, *38*, 252–253. [CrossRef]
4. Li, C.; Li, Z.; Peng, D.; Ni, J.; Pan, L.; Zhang, D.; Dong, X.; Kong, Y. Improvement of breakdown and current collapse characteristics of GaN HEMT with a polarization-graded AlGaN buffer. *Semicond. Sci. Technol.* **2015**, *30*, 035007. [CrossRef]
5. Kang, M.; Lee, M.; Choi, G.; Hwang, I.; Cha, H.; Seo, K. High-performance normally off AlGaN/GaN-on-Si HEMTs with partially recessed SiNx MIS structure. In Proceedings of the 9th International Workshop on Nitride Semiconductors, Orlando, FL, USA, 1 August 2017.
6. Klein, P.B.; Freitas, J.J.; Binari, S.C.; Wickenden, A.E. Observation of deep traps responsible for current collapse in GaN metal–semiconductor field-effect transistors. *Appl. Phys. Lett.* **1999**, *75*, 4016–4018. [CrossRef]
7. Meneghesso, G.; Chini, A.; Zanoni, E.; Manfredi, M.; Pavesi, M.; Pavesi, B.; Pavesi, C. Diagnosis of trapping phenomena in GaN MESFETs. In Proceedings of the Electron Devices Meeting, 2000. IEDM Technical Digest. International, San Francisco, CA, USA, 10–13 December 2000.
8. Binari, S.C.; Ikossi, K.; Roussos, J.A.; Kruppa, W.; Park, D.; Dietrich, H.B.; Koleske, D.D.; Wickenden, A.E.; Henry, R.L. Trapping effects and microwave power performance in AlGaN/GaN HEMTs. *IEEE Trans. Electron Devices* **2001**, *48*, 465–471. [CrossRef]
9. Klein, P.B.; Binari, S.C.; Ikossi, K.; Wickenden, A.E.; Koleske, D.D.; Henry, R.L.; Katzer, D.S. Investigation of traps producing current collapse in AlGaN/GaN high electron mobility transistors. *Electron. Lett.* **2001**, *37*, 661. [CrossRef]
10. Klein, P.B.; Binari, S.C.; Ikossi, K.; Wickenden, A.E.; Koleske, D.D.; Henry, R.L.; Katzer, D.S. Current collapse and the role of carbon in AlGaN/GaN high electron mobility transistors grown by metalorganic vapor-phase epitaxy. *Appl. Phys. Lett.* **2001**, *79*, 3527–3529. [CrossRef]
11. Vetury, R.; Zhang, N.Q.; Keller, S.; Mishra, U.K. The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs. *IEEE Trans. Electron Devices* **2001**, *48*, 560–566. [CrossRef]
12. Hasumi, Y.; Kodera, K. Simulation of the surface trap effect on the gate lag in GaAs MESFETs. *Electron. Commun. Jpn.* **2002**, *85*, 18–26. [CrossRef]
13. Binari, S.C.; Klein, P.B.; Kazior, T.E. Trapping effects in GaN and SiC microwave FETs. *Proc. IEEE* **2002**, *90*, 1048–1058. [CrossRef]
14. Wang, Z.; Zhang, Z.; Wang, S.; Chen, C.; Wang, Z.; Yao, Y. Design and Optimization on a Novel High-Performance Ultra-Thin Barrier AlGaN/GaN Power HEMT With Local Charge Compensation Trench. *Appl. Sci.* **2019**, *9*, 3054. [CrossRef]
15. Wang, Z.; Li, L. Two-dimensional polarization doping of GaN heterojunction and its potential for realizing lateral p–n junction devices. *Appl. Phys. A* **2022**, *8*, 672. [CrossRef]
16. Wang, Z.; Yang, D.; Cao, J.; Wang, F.; Yao, Y. A novel technology for turn-on voltage reduction of high-performance lateral heterojunction diode with source-gate shorted anode. *Superlattices Microstruct.* **2019**, *125*, 144–150. [CrossRef]
17. Meneghini, M.; Rossetto, I.; Bisi, D.; Stocco, A.; Pantellini, A.; Lanzieri, C.; Nanni, A.; Meneghesso, G.; Zanoni, E. Buffer Traps in Fe-Doped AlGaN/GaN HEMTs: Investigation of the Physical Properties Based on Pulsed and Transient Measurements. *IEEE Trans. Electron Devices* **2014**, *61*, 4070–4077. [CrossRef]
18. Guo, W.L.; Chen, Y.F.; Li, S.Y.; Lei, L.B.; Chang, Q. Defect studies of GaN-based HEMT devices: A review. *Chin. J. Luminesc.* **2017**, *38*, 760–767.
19. Bergsten, J.; Thorsell, M.; Adolph, D.; Chen, J.; Kordina, O.; Sveinbjörnsson, E.; Rorsman, N. Electron trapping in extended defects in microwave AlGaN/GaN HEMTs with carbon-doped buffers. *IEEE Trans. Electron Devices* **2018**, *65*, 2446–2453. [CrossRef]
20. Villamin, M.E.; Kondo, T.; Iwata, N. Effect of C- and Fe-doped GaN buffer on AlGaN/GaN high electron mobility transistor performance on GaN substrate using side-gate modulation. *Jpn. J. Appl. Phys.* **2021**, *60*, SBBF01. [CrossRef]

21. Bisi, D.; Stocco, A.; Rossetto, I.; Meneghini, M.; Rampazzo, F.; Chini, A.; Soci, F.; Pantellini, A.; Lanzieri, C.; Gamarra, P.; et al. Effects of buffer compensation strategies on the electrical performance and RF reliability of AlGaN/GaN HEMTs. *Microelectron. Reliab.* **2015**, *55*, 1662–1666. [CrossRef]

22. Meneghini, M.; Bisi, D.; Rossetto, I.; Santi, C.D.; Stocco, A.; Hilt, O.; Bahat-Treidel, E.; Wuerfl, J.; Rampazzo, F.; Meneghesso, G.; et al. Trapping processes related to iron and carbon doping in AlGaN/GaN power HEMTs. *Proc. SPIE* **2015**, *9363*, 93632O.

23. Joshi, V.; Gupta, S.D.; Chaudhuri, R.R.; Shrivastava, M. Interplay between surface and buffer traps in governing breakdown characteristics of AlGaN/GaN HEMTs-Part II. *IEEE Trans. Electron Devices* **2020**, *68*, 80–87. [CrossRef]

24. Wang, F.Z.; Chen, W.J.; Wang, Y.; Sun, R.Z.; Ding, G.J.; Yu, P.; Wang, X.H.; Feng, Q.; Xu, W.J.; Xu, X.R.; et al. Analytically Modeling the Effect of Buffer Charge on the 2DEG Density in AlGaN/GaN HEMT. *IEEE Trans. Electron Devices* **2023**, 1–8. [CrossRef]

25. Wang, F.; Chen, W.; Sun, R.; Wang, Z.; Zhang, B. An analytical model on the gate control capability in p-gan gate algan/gan high-electron-mobility transistors considering buffer acceptor traps. *J. Phys. D Appl. Phys.* **2020**, *54*, 095107. [CrossRef]

26. Wu, M.; Zhang, M.; Yang, L.; Hou, B.; Yu, Q.; Li, S.M.; Shi, C.Z.; Zhao, W.; Lu, H.; Chen, W.W.; et al. First Demonstration of State-of-the-art GaN HEMTs for Power and RF Applications on A Unified Platform with Free-standing GaN Substrate and Fe/C Co-doped Buffer. In Proceedings of the 2022 International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 3–7 December 2022.

27. Nomoto, K.; Hu, Z.; Song, B.; Zhu, M.; Qi, M.; Yan, R.; Protasenko, V.; Imhoff, E.; Kuo, J.; Kaneda, T.; et al. GaN-on-GaN p-n power diodes with 3.48 kV and 0.95 mΩ·cm^2: A record high figure-of-merit of 12.8 GW/cm^2. In Proceedings of the 2015 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 7–9 December 2015.

28. Lee, W.I.; Huang, T.C.; Guo, J.D.; Feng, M.S. Effects of column III alkyl sources on deep levels in GaN grown by organometallic vapor phase epitaxy. *Appl. Phys. Lett.* **1995**, *67*, 1721–1723. [CrossRef]

29. Soh, C.B.; Chua, S.J.; Lim, H.F.; Chi, D.; Liu, W.; Tripathy, S. Identification of deep levels in GaN associated with dislocations. *J. Phys. Condens. Matter* **2004**, *16*, 6305–6315. [CrossRef]

30. Yutaka, T.; Yujiro, Y.; Shibata, T.; Yamaguchi, S.; Ueda, H.; Uesugi, T.; Kachi, T. Hole traps in n-GaN detected by minority carrier transient spectroscopy. *Phys. Status Solidi* **2011**, *8*, 433–436.

31. Hacke, P.; Nakayama, H.; Detchprohm, T.; Hiramatsu, K.; Sawaki, N. Deep levels in the upper band-gap region of lightly Mg-doped GaN. *Appl. Phys. Lett.* **1996**, *68*, 1362–1364. [CrossRef]

32. Chung, H.M.; Chuang, W.C.; Pan, Y.C.; Tsai, M.C.; Lee, M.C.; Chen, W.K.; Chiang, C.I.; Lin, C.H.; Chang, H. Electrical characterization of isoelectronic in-doping effects in GaN films grown by metalorganic vapor phase epitaxy. *Appl. Phys. Lett.* **2000**, *76*, 897–899. [CrossRef]

33. Umana-Membreno, G.A.; Dell, J.M.; Hessler, T.P.; Nener, B.D.; Parish, G.; Faraone, L.; Mishra, U.K. 60Co gamma-irradiation-induced defects in n-GaN. *Appl. Phys. Lett.* **2002**, *80*, 4354–4356. [CrossRef]

34. Cho, H.K.; Kim, C.S.; Hong, C.H. Electron capture behaviors of deep level traps in unintentionally doped and intentionally doped n-type GaN. *J. Appl. Phys.* **2003**, *94*, 1485–1489. [CrossRef]

35. Hacke, P.; Detchprohm, T.; Hiramatsu, K.; Speck, J.S.; Mishra, U.K.; DenBaars, S.P. Analysis of deep levels in n-type GaN by transient capacitance methods. *J. Appl. Phys.* **1994**, *76*, 304–309. [CrossRef]

36. Hierro, A.; Ringel, S.A.; Hansen, M.; Speck, J.S.; Mishra, U.K.; DenBaars, S.P. Hydrogen passivation of deep levels in n-GaN. *Appl. Phys. Lett.* **2000**, *77*, 1499–1501. [CrossRef]

37. Sasikumar, A.; Arehart, A.R.; Cardwell, D.W.; Jackson, C.M.; Sun, W.; Zhang, Z.; Ringel, S.A. Deep trap-induced dynamic on-resistance degradation in GaN-on-Si power MISHEMTs. *Microelectron. Reliab.* **2016**, *61*, 39–44. [CrossRef]

38. Calleja, E.; Sanchez, F.J.; Basak, D.; Sánchez-García, M.A.; Muñoz, E.; Izpura, I.; Calle, F.; Tijero, J.M.G.; Sánchez-Rojas, J.L.; Beaumont, B.; et al. Yellow luminescence and related deep states in undoped GaN. *Phys. Rev. B* **1997**, *55*, 4689–4694. [CrossRef]

39. Bouslama, M.; Gillet, V.; Chang, C.; Nallatamby, J.C.; Sommet, R.; Prigent, M.; Quéré, R.; Lambert, B. Dynamic Performance and Characterization of Traps Using Different Measurements Techniques for the New AlGaN/GaN HEMT of 0.15-μm Ultrashort Gate Length. *IEEE Trans. Microw. Theory Tech.* **2019**, *67*, 2475–2482. [CrossRef]

40. Benvegnu, A.; Bisi, D.; Laurent, S.; Meneghini, M.; Meneghesso, G.; Muraro, J.L.; Barataud, D.; Zanoni, E.; Quere, R. Trap Investigation under Class AB Operation in AlGaN/GaN HEMTs Based on Output-Admittance Frequency Dispersion, Pulsed and Transient Measurements. In Proceedings of the IEEE Microwave Integrated Circuits Conference, Paris, France, 7–8 September 2015.

41. Hernandez, C.; López-López, M.; Casallas-Moreno, Y.L.; Rangel-Kuoppa, V.; Cardona, D.; Hu, Y.; Kudriatsev, Y.; Zambrano-Serrano, M.A.; Gallardo-Hernandez, S. Study of the Heavily p-Type Doping of Cubic GaN with Mg. *Sci. Rep.* **2020**, *10*, 16858.

42. Chen, J.; Huang, W.; Qu, H.; Zhang, Y.; Zhou, J.; Zou, X. Study of Minority Carrier Traps in p-GaN Gate HEMT by Optical Deep Level Transient Spectroscopy. *Appl. Phys. Lett.* **2022**, *120*, 211105. [CrossRef]

43. Armstrong, A.; Chakraborty, A.; Speck, J.S.; DenBaars, S.P.; Mishra, U.K.; Ringel, S.A. Characterization and Discrimination of AlGaN- and GaN-Related Deep Levels in AlGaN/GaN Heterostructures. *AIP Conf. Proc.* **2007**, *893*, 223–224.

44. Fang, Z.Q.; Look, D.C.; Kim, D.H.; Adesida, I. Traps in AlGaN/GaN/SiC heterostructures studied by deep level transient spectroscopy. *Appl. Phys. Lett.* **2005**, *87*, 182103. [CrossRef]

45. Nakano, Y.; Irokawa, Y.; Takeguchi, M. Deep-Level Optical Spectroscopy Investigation of Band Gap States in AlGaN/GaN Hetero-Interfaces. *Appl. Phys. Express* **2008**, *1*, 091101. [CrossRef]

46. Arehart, A.R.; Sasikumar, A.; Via, G.D.; Winningham, B.; Poling, B.; Heller, E.; Ringel, S.A. Spatially-discriminating trap characterization methods for HEMTs and their application to RF-stressed AlGaN/GaN HEMTs. In Proceedings of the IEEE Microwave Symposium Digest, San Francisco, CA, USA, 6–8 December 2010; pp. 394–397.

47. Cho, H.K.; Khan, F.A.; Adesida, I.; Fang, Z.Q.; Look, D.C. Deep level characteristics in n-GaN with inductively coupled plasma damage. *J. Phys. D Appl. Phys.* **2008**, *41*, 155314. [CrossRef]

48. Dupouy, E.; Raja, P.V.; Gaillard, F.; Sommet, R.; Nallatamby, J.C. Trap Characterization in InAlN/GaN and AlN/GaN based HEMTs with Fe- and C-doped Buffers. In Proceedings of the 2021 16th European Microwave Integrated Circuits Conference (EuMIC), London, UK, 3–4 April 2022.

49. Bouslama, M.; Raja, P.V.; Gaillard, F.; Sommet, R.; Nallatamby, J.C. Investigation of Electron Trapping in AlGaN/GaN HEMT with Fe-doped Buffer through DCT Characterization and TCAD Device Simulations. *AIP Adv.* **2021**, *11*, 025018. [CrossRef]

50. Raja, P.V.; Dupouy, E.; Bouslama, M.; Sommet, R.; Nallatamby, J.C. Estimation of Trapping Induced Dynamic Reduction in 2DEG Density of GaN-Based HEMTs by Gate-Lag DCT Technique. *IEEE Trans. Electron Devices* **2022**, *69*, 4864–4869. [CrossRef]

51. Pan, S.; Feng, S.; Li, X.; Bai, K.; Lu, X.; Li, Y.; Zhang, J.; Zhou, L. Characterization of Hole Traps in Reverse-Biased Schottky-type p-GaN Gate HEMTs by Current-Transient Method. *Appl. Phys. Lett.* **2022**, *121*, 153501. [CrossRef]

52. Pan, S.; Feng, S.; Li, X.; Bai, K.; Lu, X.; Zhu, J.; Zhang, J.; Zhou, L. Identification of Traps in p-GaN Gate HEMTs During OFF-State Stress by Current Transient Method. *IEEE Trans. Electron Devices* **2022**, *69*, 4877–4882. [CrossRef]

53. Ťapajna, M.; Simms, R.J.T.; Faqir, M.; Kuball, M.; Pei, Y.; Mishra, U.K. Identification of Electronic Traps in AlGaN/GaN HEMTs Using UV Light-Assisted Trapping Analysis. In Proceedings of the 010 IEEE International Reliability Physics Symposium, Anaheim, CA, USA, 2–6 May 2010.

54. Meneghesso, G.; Verzellesi, G.; Pierobon, R.; Rampazzo, F.; Chini, A.; Mishra, U.K.; Canali, C.; Zanoni, E. Surface-Related Drain Current Dispersion Effects in AlGaN-GaN HEMTs. *IEEE Trans. Electron Devices* **2004**, *51*, 1554–1561. [CrossRef]

55. Joh, J.; Alamo, J. A Current-Transient Methodology for Trap Analysis for GaN High Electron Mobility Transistors. *IEEE Trans. Electron Devices* **2011**, *58*, 132–140. [CrossRef]

56. Tartarin, J.G.; Karboyan, S.; Olivie, F.; Astre, G.; Bary, L.; Lambert, B. I-DLTS, Electrical Lag and Low Frequency Noise Measurements of Trapping Effects in AlGaN/GaN HEMT for Reliability Studies. In Proceedings of the 2011 6th European Microwave Integrated Circuit Conference, Manchester, UK, 10–11 October 2011.

57. Subramani, N.K.; Couvidat, J.; Hajjar, A.A.; Nallatamby, J.; Sommet, R.; Quéré, R. Identification of GaN Buffer Traps in Microwave Power AlGaN/GaN HEMTs Through Low Frequency S-Parameters Measurements and TCAD-Based Physical Device Simulations. *IEEE J. Electron Devices Soc.* **2017**, *5*, 175–181. [CrossRef]

58. Gustafsson, S.; Chen, J.; Forsberg, U.; Thorsell, N.; Janzén, E.; Rorsman, N. Dispersive Effects in Microwave AlGaN/AlN/GaN HEMTs with Carbon-Doped Buffer. *IEEE Trans. Electron Devices* **2015**, *62*, 2162–2169. [CrossRef]

59. Raja, P.V.; Subramani, N.K.; Gaillard, F.; Bouslama, M.; Sommet, R.; Nallatamby, J.C. Identification of Buffer and Surface Traps in Fe-Doped AlGaN/GaN HEMTs Using Y21 Frequency Dispersion Properties. *Electronics* **2021**, *10*, 3096. [CrossRef]

60. Bouslama, M.; Hajjar, A.A.; Laurent, S.; Subramani, N.K.; Nallatamby, J.C.; Prigent, M. Low Frequency Drain Noise Characterization of Different Technologies of GaN HEMTs: Investigation of Trapping Mechanism. In Proceedings of the International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMIC), Brive La Gaillarde, France, 10–11 December 2018.

61. Tartarin, J.G.; Soubercaze-Pun, G.; Grondin, J.J.; Bary, L.; Mimila-Arroyo, J.; Chevallier, J. Generation-Recombination Defects In AlGaN/GaN HEMT on SiC Substrate, Evidenced By Low Frequency Noise Measurements and SIMS Characterization. *AIP Conf. Proc.* **2007**, *922*, 163–166.

62. Polyakov, A.Y.; Smirnov, N.B.; Govorkov, A.V.; Shlensky, A.A.; Pearton, S.J. Influence of high-temperature annealing on the properties of Fe doped semi-insulating GaN structures. *J. Appl. Phys.* **2004**, *95*, 5591–5596. [CrossRef]

63. Silvestri, M.; Uren, M.J.; Kuball, M. Iron-induced deep-level acceptor center in GaN/AlGaN high electron mobility transistors: Energy level and cross section. *Appl. Phys. Lett.* **2013**, *102*, 073501. [CrossRef]

64. Ma, X.H.; Zhu, J.J.; Liao, X.Y.; Yue, T.; Chen, W.W.; Hao, Y. Quantitative characterization of interface traps in Al_2O_3/AlGaN/GaN metal-oxide-semiconductor high-electron-mobility transistors by dynamic capacitance dispersion technique. *Appl. Phys. Lett.* **2013**, *103*, 033510. [CrossRef]

65. Potier, C.; Martin, A.; Campovecchio, M.; Laurent, S.; Quere, R.; Jacquet, J.C.; Jardel, O.; Piotrowicz, S.; Delage, S. Trap characterization of microwave GaN HEMTs based on frequency dispersion of the output-admittance. In Proceedings of the European Microwave Integrated Circuit Conference, Rome, Italy, 6–9 October 2014; pp. 464–467.

66. Huang, S.; Wang, X.; Liu, X.; Kang, X.W.; Fan, J.; Yang, S.; Yin, H.; Wei, K.; Zheng, Y.; Wang, X.; et al. Revealing the Positive Bias Temperature Instability in Normally-OFF AlGaN/GaN MIS-HFETs by Constant-Capacitance DLTS. In Proceedings of the 2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD), Shanghai, China, 19–23 May 2019.

67. Meneghesso, G.; Meneghini, M.; Bisi, D.; Rossetto, I.; Cester, A.; Mishra, U.K.; Zanoni, E. Trapping phenomena in AlGaN/GaN HEMTs: A study based on pulsed and transient measurements. *Semicond. Sci. Technol.* **2013**, *28*, 014005. [CrossRef]

68. Meneghini, M.; Bisi, D.; Marcon, D.; Stoffels, S.; Hove, M.V.; Wu, T.L.; Decoutere, S.; Meneghesso, G.; Zanoni, E. Trapping in GaN-based metal-insulator-semiconductor transistors: Role of high drain bias and hot electrons. *Appl. Phys. Lett.* **2014**, *104*, 143505. [CrossRef]

69. Subramani, N.K.; Couvidat, J.; Hajjar, A.A.; Nallatamby, J.; Floriot, D.; Prigent, M.; Quéré, R. Low-Frequency Noise Characterization in GaN HEMTs: Investigation of Deep Levels and Their Physical Properties. *IEEE Electron Device Lett.* **2017**, *38*, 1109–1112. [CrossRef]

70. Potier, C.; Jacquet, J.; Dua, C.; Martin, A.; Campovecchio, M.; Oualli, M.; Jardel, O.; Piotrowicz, S.; Laurent, S.; Aubry, R.; et al. Highlighting trapping phenomena in microwave GaN HEMTs by low-frequency S-parameters. *Int. J. Microw. Wirel. Technol.* **2015**, *7*, 287–296. [CrossRef]

71. Matteo, M.; Carlo, D.S.; Idriss, A.; Matteo, B.; Marcello, C.; Riyaz, A.K.; Luca, N.; Nicolò, Z.; Alessandro, C.; Farid, M.; et al. GaN-based power devices: Physics, reliability, and perspectives. *J. Appl. Phys.* **2021**, *130*, 181101.

72. Yang, S.; Huang, S.; Wei, J.; Zheng, Z.; Wang, Y.; He, J.; Chen, K.V. Identification of Trap States in p-GaN Layer of a p-GaN/AlGaN/GaN Power HEMT Structure by Deep-Level Transient Spectroscopy. *IEEE Electron Device Lett.* **2020**, *41*, 685–688. [CrossRef]

73. Gassoumi, M.; Bluet, J.M.; Guillot, G.; Gaquiere, C.; Maaref, H. Characterization of deep levels in high electron mobility transistor by conductance deep level transient spectroscopy. *Mater. Sci. Eng. C* **2008**, *28*, 787–790. [CrossRef]

74. Salah, S.; Saadaoui, M.; Gassoumi, M.; Maaref, H.; Christophe, G. Anomaly and defects characterization by I-V and current deep level transient spectroscopy of $Al_{0.25}Ga_{0.75}N/GaN/SiC$ high electron-mobility transistors. *J. Appl. Phys.* **2012**, *111*, 073713.

75. Lang, D.V. Deep-level transient spectroscopy: A new method to characterize traps in semiconductors. *J. Appl. Phys.* **1974**, *45*, 3023–3032. [CrossRef]

76. Lefèvre, H.; Schulz, M. Double correlation technique (DDLTS) for the analysis of deep level profiles in semiconductors. *Appl. Phys. A* **1977**, *12*, 45–53. [CrossRef]

77. Kosai, K. External generation of gate delays in a boxcar integrator—Application to deep level transient spectroscopy. *Rev. Sci. Instrum.* **1982**, *53*, 210–213. [CrossRef]

78. Auret, F.D.; Meyer, W.E.; Diale, M.; Rensburg, P.; Song, S.F.; Temst, K. Electrical Characterization of Metastable Defects Introduced in GaN by Eu-Ion Implantation. *Mater. Sci. Forum* **2011**, *804*, 679–680. [CrossRef]

79. Huang, S.; Wang, X.; Liu, X.; Zhao, R.; Shi, W.; Zhang, Y.; Fan, J.; Yin, H.; Wei, K.; Zheng, Y.; et al. Capture and emission mechanisms of defect states at interface between nitride semiconductor and gate oxides in GaN-based metal-oxide-semiconductor power transistors. *J. Appl. Phys.* **2019**, *126*, 164505. [CrossRef]

80. Johnson, N.M. Measurement of semiconductor–insulator interface states by constant-capacitance deep-level transient spectroscopy. *J. Vac. Sci. Technol.* **1982**, *21*, 303–314. [CrossRef]

81. Li, M.F.; Sah, C.T. New techniques of capacitance-voltage measurements of semiconductor junctions. *Solid-State Electron.* **1982**, *25*, 95–99. [CrossRef]

82. Dejule, R.Y.; Haase, M.A.; Ruby, D.S.; Stillman, G.E. Constant capacitance DLTS circuit for measuring high purity semiconductors. *Solid State Electron.* **1985**, *28*, 639–641. [CrossRef]

83. Kolev, P. An improved feedback circuit for constant-capacitance voltage transient measurements. *Solid-State Electron.* **1992**, *35*, 387–389. [CrossRef]

84. Li, M.F.; Sah, C.T. A new method for the determination of dopant and trap concentration profiles in semiconductors. *IEEE Trans. Electron Devices* **1982**, *29*, 306–315.

85. Huang, S.; Shu, Y.; Roberts, J.; Chen, K.V. Characterization of Vth-instability in Al_2O_3/GaN/AlGaN/GaN MIS-HEMTs by quasi-static C-V measurement. *Phys. Status Solid* **2012**, *9*, 923–926. [CrossRef]

86. Gray, P.V.; Brown, D.M. Density of SiO_2–Si interface states. *Appl. Phys. Lett.* **1966**, *8*, 31–33. [CrossRef]

87. Nicollian, E.H.; Goetzberger, A. The Si-SiO_2 interface-electrical properties as determined by the metal-insulator-silicon conductance technique. *Bell Syst. Tech. J.* **1967**, *46*, 1055–1133. [CrossRef]

88. Alghamdi, S.; Si, M.; Bae, H.; Zhou, H.; Ye, P.D. Single Pulse Charge Pumping Measurements on GaN MOS-HEMTs: Fast and Reliable Extraction of Interface Traps Density. *IEEE Trans. Electron Devices* **2020**, *67*, 444–448. [CrossRef]

89. Lin, L.; Ji, Z.; Zhang, J.F.; Zhang, W.D.; Kaczer, B.; Gendt, S.D.; Groeseneken, G. A Single Pulse Charge Pumping Technique for Fast Measurements of Interface States. *IEEE Trans. Electron Devices* **2011**, *58*, 1490–1498. [CrossRef]