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Comprehensive Comparison of MOCVD- and LPCVD-SiN_x Surface Passivation for AlGaN/GaN HEMTs for 5G RF Applications

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Abstract: Passivation is commonly used to suppress current collapse in AlGaN/GaN HEMTs. However, the conventional PECV-fabricated SiN_x passivation layer is incompatible with the latest process, like the "passivation-prior-to-ohmic" method. Research attention has therefore turned to high-temperature passivation schemes. In this paper, we systematically investigated the differences between the SiN_x/GaN interface of two high-temperature passivation schemes, MOCVD-SiN_x and LPCVD-SiN_x, and investigated their effects on the ohmic contact mechanism. By characterizing the device interface using TEM, we reveal that during the process of MOCVD-SiN_x, etching damage and Si diffuses into the semiconductor to form a leakage path and reduce the breakdown voltage of the AlGaN/GaN HEMTs. Moreover, N enrichment at the edge of the ohmic region of the LPCVD-SiN_x device indicates that the device is more favorable for TiN formation, thus reducing the ohmic contact resistance, which is beneficial to improving the PAE of the device. Through the CW load-pull test with drain voltage V_{DS} = 20V, LPCVD-SiN_x devices obtain a high PAE of 66.35%, which is about 6% higher than MOCVD-SiN_x devices. This excellent result indicates that the prospect of LPCVD-SiN_x passivation devices used in 5G small terminals will be attractive.

Keywords: AlGaN/GaN; high electron mobility transistors (HEMTs); SiN_x passivation; low-pressure chemical vapor deposition (LPCVD); ohmic contact; SiN_x/GaN interface

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1. Introduction

With the rapid growth of mobile data volume, traditional 4G networks are no longer able to meet the demands for higher speeds, lower latency, and more reliable connections. As a result, the development of 5G as the next generation of mobile communication technology aims to provide more efficient, flexible, and innovative communication solutions to support various novel applications and the expanding needs of the digital society. In 5G applications, GaN semiconductors offer unique advantages including wide bandgap and high operation frequency compared to Si and group III-V material [1]. Devices based on GaN materials exhibit higher output power density and energy conversion efficiency, enabling system miniaturization and lightweight design. Today, GaN devices have been widely used in radio frequency (RF) applications [2–4] and power electronics [5–7]. However, during the process of GaN HEMT epitaxial growth, surface states like dangling bonds or defects will exist on the interrupted surfaces [8,9]. These surface states will lead to some adverse phenomena such as current collapse, thereby significantly impacting the RF output performance of GaN HEMT devices [10,11]. There are currently various methods available for suppressing surface states, such as growth-controlling conditions [12,13] or surface passivation [14]. Surface passivation has become an effective and common method

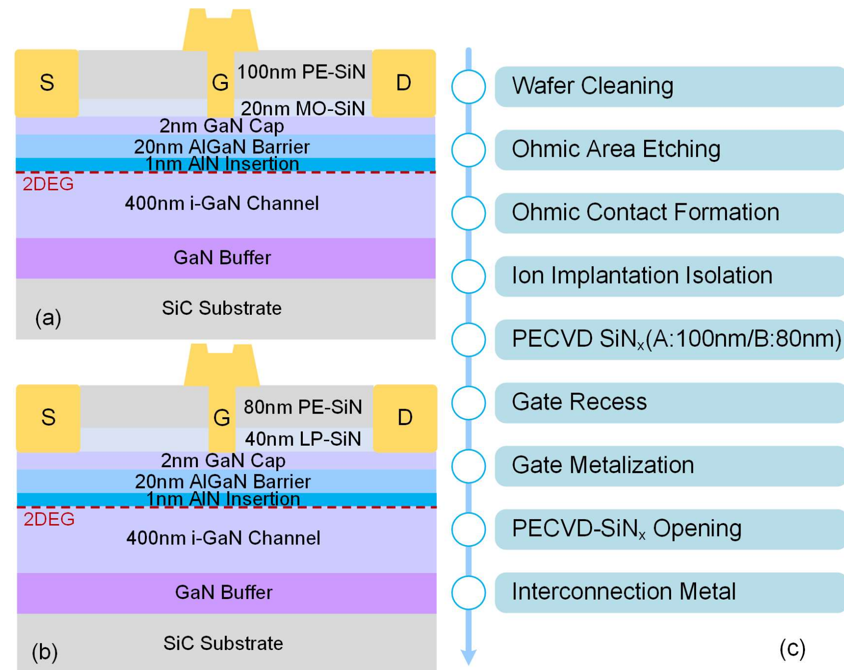
due to its simplicity. It has a relatively simple process and can reduce the possibility of chemical contamination or mechanical damage to the surface during subsequent packaging processes. The passivation material mostly used on GaN HEMTs is SiN_x [15] and the most commonly used deposition method for it is plasma-enhanced chemical vapor deposition (PECVD) with a growth temperature below 350 °C [16]. However, due to its tendency to crack under high-temperature conditions [17], it is not possible to carry out the "passivation-prior-to-ohmic" process [18]. In addition, SiN_x growth using PECVD has lower film compactness compared to the SiN_x deposited by metal organic chemical vapor deposition (MOCVD) and low-pressure chemical vapor deposition (LPCVD) [18,19]. The active plasma sources in PECVD can also potentially cause damage to the surface of AlGaN or GaN and further degrade the quality of the deposited SiN_x itself [20]. Therefore, improved high-temperature solutions, including MOCVD (over 900 °C) and LPCVD (over 750 °C), are used for depositing the passivation layer [21–23]. MOCVD, an in-situ SiNx passivation technique, is employed in which an epitaxial layer is deposited using MOCVD, followed by the deposition of an additional SiNx passivation layer within the same chamber. This in-situ growth approach helps to prevent some negative impacts during the process chamber transfer, such as oxidation reactions. During the LPCVD process for SiNx deposition, the pressure is typically maintained at around 200 mTorr. At a specific temperature, the lower operating pressure results in an increased mean free path of gas molecules within the chamber, leading to a significant reduction in diffusion rate. Consequently, the reaction time is prolonged, thereby achieving the objective of enhancing thin film quality and density. The research above has revealed that SiN_x passivation layers deposited at high temperatures exhibit higher thermal stability and better growth quality, which can significantly suppress surface state density and enhance the output characteristics of devices.

However, it is noted that a high-temperature deposited SiN_x layer is often used in power electronic devices to form MIS gate structures [23,24], while there are limited evaluations in the field of RF applications [25] and there has been little research on the interface under SiN_x layers and the mechanism of ohmic contact, which are important concerns for enhancing the RF performance of AlGaN/GaN HEMTs. The impact of the passivation layer on ohmic alloying is not yet clear, and there is no relevant research on the interface quality of the passivation layer and its interdiffusion with the barrier layer. Therefore, this work systematically compares MOCVD-SiN_x and LPCVD-SiN_x, which are known for their high-temperature processes to evaluate interface quality and the impact on ohmic contact. Finally, this study will assess the performance between the two passivation layer approaches in RF applications.

2. Device Structure and Fabrication

The structures of sample A and sample B used in this work are shown in Figure 1a,b. The AlGaN/GaN heterostructure of both samples was grown on a three-inch SiC substrate using MOCVD. The epilayer, from the bottom to the top, included a GaN buffer (a 400 nm unintentionally doped GaN channel layer). On top of the GaN channel layer, there was a 1 nm AlN insertion layer, facilitating the growth of a 20 nm AlGaN layer with 25% Al composition. A 2 nm GaN cap layer was deposited on the barrier layer. Considering the growth quality of the passivation layer and the stress management, the difference between sample A and sample B is that there was a 20 nm in situ SiN_x passivation layer utilized using MOCVD and a 40 nm ex situ SiN_x passivation layer utilized by LPCVD. The device fabrication process followed the "passivation-prior-to-ohmic" strategy. The fabrication process flow is shown in Figure 1c. The SiN_x passivation layer above the ohmic region was first etched away by F-based etching. The F-based etching gas mixture consists of CF4/O2 = 25/5 sccm, and the etching pressure is set to 5 mTorr. Then, another ohmic photolithography process was performed followed by ohmic contact formation. The ohmic contact metal stack was Ti/Al/Ni/Au = 20/160/45/55 nm, with annealing performed at 860 °C/60 s under ambient N_2 conditions. The electrical isolation of the devices was

achieved using nitrogen ion implantation. To form the T-gate structure, on sample A, the 20 nm SiN_x passivation layer was supplemented with 100 nm SiN_x grown by PECVD, and the 40 nm SiN_x layer was supplemented with an additional 80 nm SiN_x grown by PECVD on sample B. The T-gate electrode was formed by Ni/Au = 45/400 nm stacks with a 0.5 µm foot length and a 1 µm cap length, while the gate width was 100 µm. Finally, interconnection metal fabrication was completed by evaporating Ti/Au = 20/400 nm.



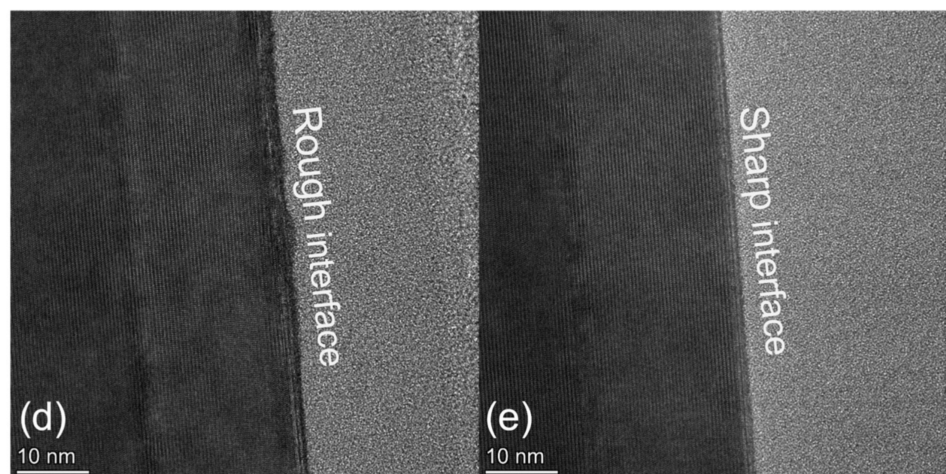


Figure 1. The device structure diagram of (**a**) sample A and (**b**) sample B. (**c**) The fabrication process flow of the samples. The TEM image of the interface quality of SiN_x/GaN in (**d**) sample A and (**e**) sample B.

3. Results and Discussion

After the fabrication, the samples were tested using a Keysight B1500A semiconductor parameter analyzer to obtain the result of the transmission line model (TLM) and the DC characteristics. The pulse I-V characteristics were tested using a Keithley 4200A-SCS parameter analyzer.

A. The Epitaxial Growth of Device

Figure 1d,e compare the epitaxial growth quality of sample A and sample B after ohmic annealing. It can be observed from the transmission electron microscopy (TEM) that Si was significantly diffused at the interface of sample A, resulting in a rough SiN_x/GaN boundary. In contrast, in sample B, there was a clear boundary between the LPCVD-SiN_x and the semiconductor interface, indicating the good suppression of Si diffusion. This is because, during the process of depositing the SiN_x film using MOCVD, SiH_4 had an etching effect on the semiconductor layer, allowing Si to diffuse into the semiconductor as an impurity. According to the results, we suppose that LPCVD can effectively prevent the diffusion of Si. Zhu et al. have demonstrated that the surface diffusion of Si is insufficient to compensate for the electron concentration and enhance performance [26]. On the contrary, etching damage accompanied by the diffusion of Si into the semiconductor will generate a leakage current path through the gate, affecting the reverse characteristics of the device [27].

B. Formation Mechanism of Ohmic Contact

Figures 2 and 3 compare the morphology of ohmic regions in samples A and B. The formation of TiN in high-temperature annealing can promote ohmic metal formation by ensuring direct contact with 2DEG or by forming N vacancies reported by many reports [28–31]. There was no apparent low-work function TiN alloy incorporation in the edge of the ohmic region of sample A, while there was large TiN alloy incorporation in sample B. Since there was sidewall contact between the ohmic metal stack and the passivation layer in the "passivation-prior-to-ohmic" scheme, some different alloy reactions occurred under the same annealing conditions. Based on an analysis of the distribution of Ti and N elements at the edge of the ohmic region for sample A (shown in the red box in Figure 2g,j) and sample B (shown in the red box in Figure 3g,j), we infer that this is because the deposition temperature of MOCVD-SiN_x was above 900 °C while the annealing temperature of sample A was lower than 900 °C, resulting in N being difficult to participate in the alloy reaction in order to form TiN from the side walls during the annealing alloying process. In contrast, the deposition temperature of LPCVD-SiN_x was 780 °C, which is less than the annealing temperature of 860 °C. This may make it easier for N to combine with Ti to form TiN in sample B. This enrichment of TiN at the edge of the ohmic region, which is also compared in Figures 2k and 3k, effectively reduced the ohmic contact resistance.

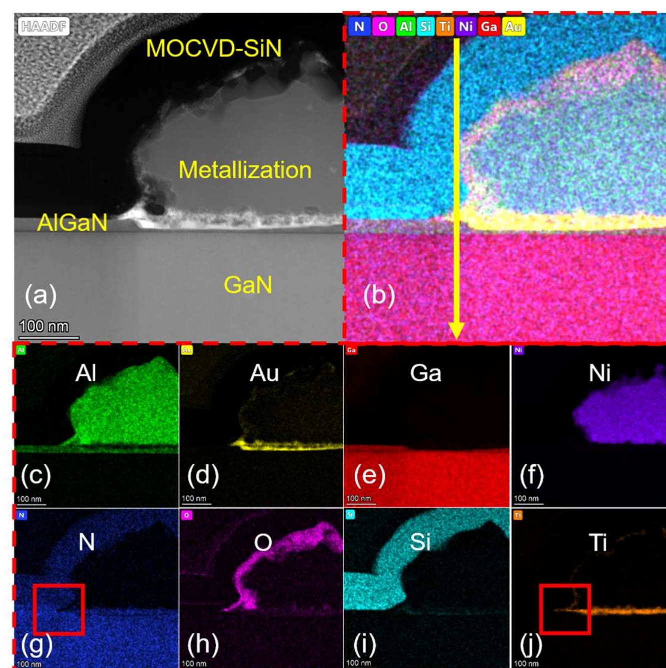


Figure 2. *Cont.*

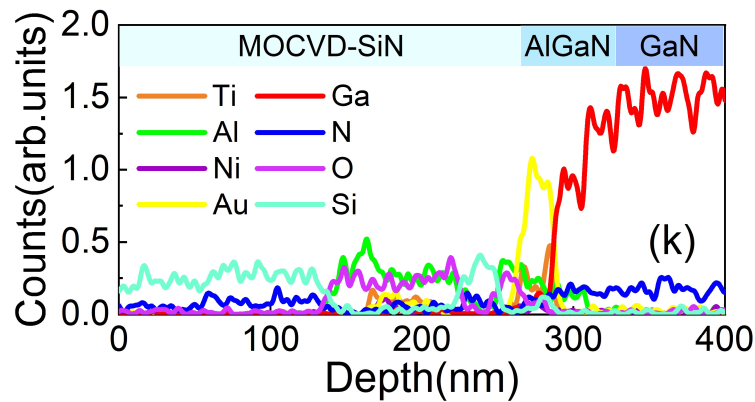


Figure 2. (**a**) The HAADF-STEM micrograph of the sidewall ohmic region for sample A. (**b**) EDX mapping of all elements. (**c**–**j**) EDX mapping of Al, Au, Ga, Ni, N, O, Si, and Ti. (**k**) EDS line scan profile of yellow arrow presented in (**b**).

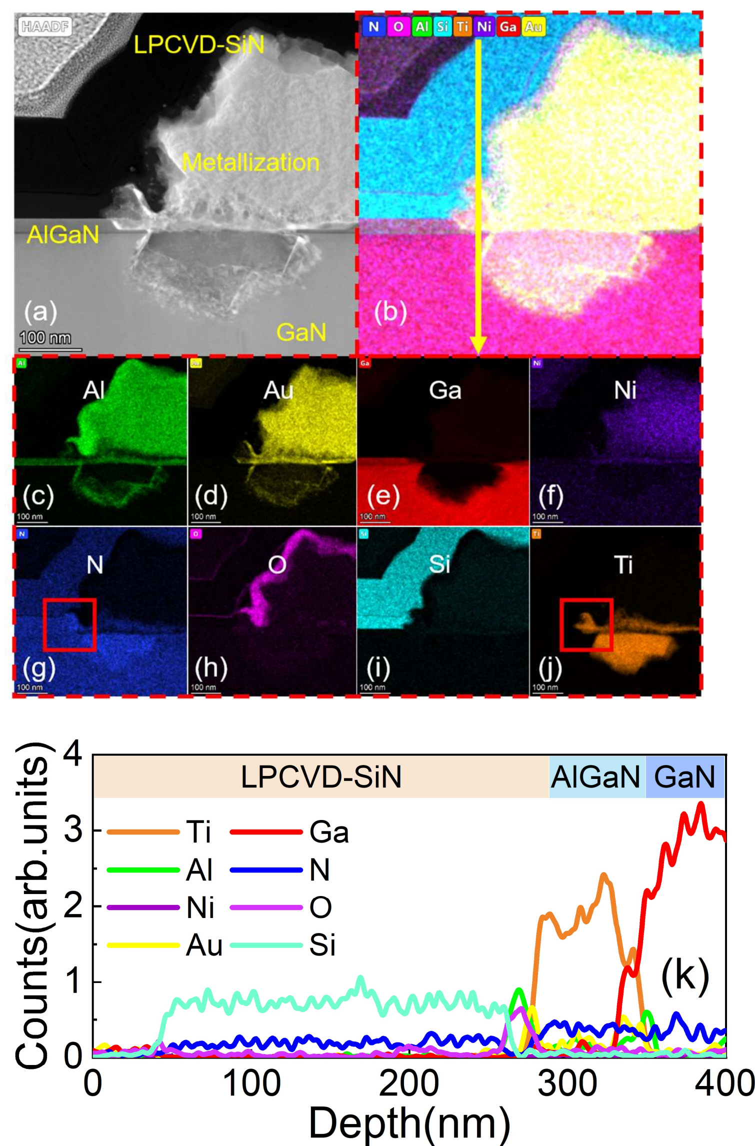


Figure 3. (**a**) The HAADF-STEM micrograph of the sidewall ohmic region for sample B. (**b**) EDX mapping of all elements. (**c**–**j**) EDX mapping of Al, Au, Ga, Ni, N, O, Si, and Ti. (**k**) EDS line scan profile of yellow arrow presented in (**b**).

C. Ohmic Contact Resistance and DC I-V Characteristics

The ohmic contact results obtained by the transmission line model (TLM) test are shown in Figure 4a. The ohmic contact resistance (R_c) for sample B with apparent side wall effect was 0.32 ± 0.05 Ω·mm and the sheet resistance (R_{sh}) was 291 Ω/sq, whereas the R_c for sample A was 0.39 ± 0.05 Ω·mm, with an R_{sh} of 302 Ω/sq. Figure 4b displays the DC characteristic curves of samples A and B. From the transfer I–V curves, it can be observed that the threshold voltage for sample A was −3.7 V with a maximum transconductance ($g_{m,max}$) of 294 mS/mm, while sample B had a threshold voltage of −3.8 V and $g_{m,max}$ of 346 mS/mm, which was 50 mS/mm higher than sample A.

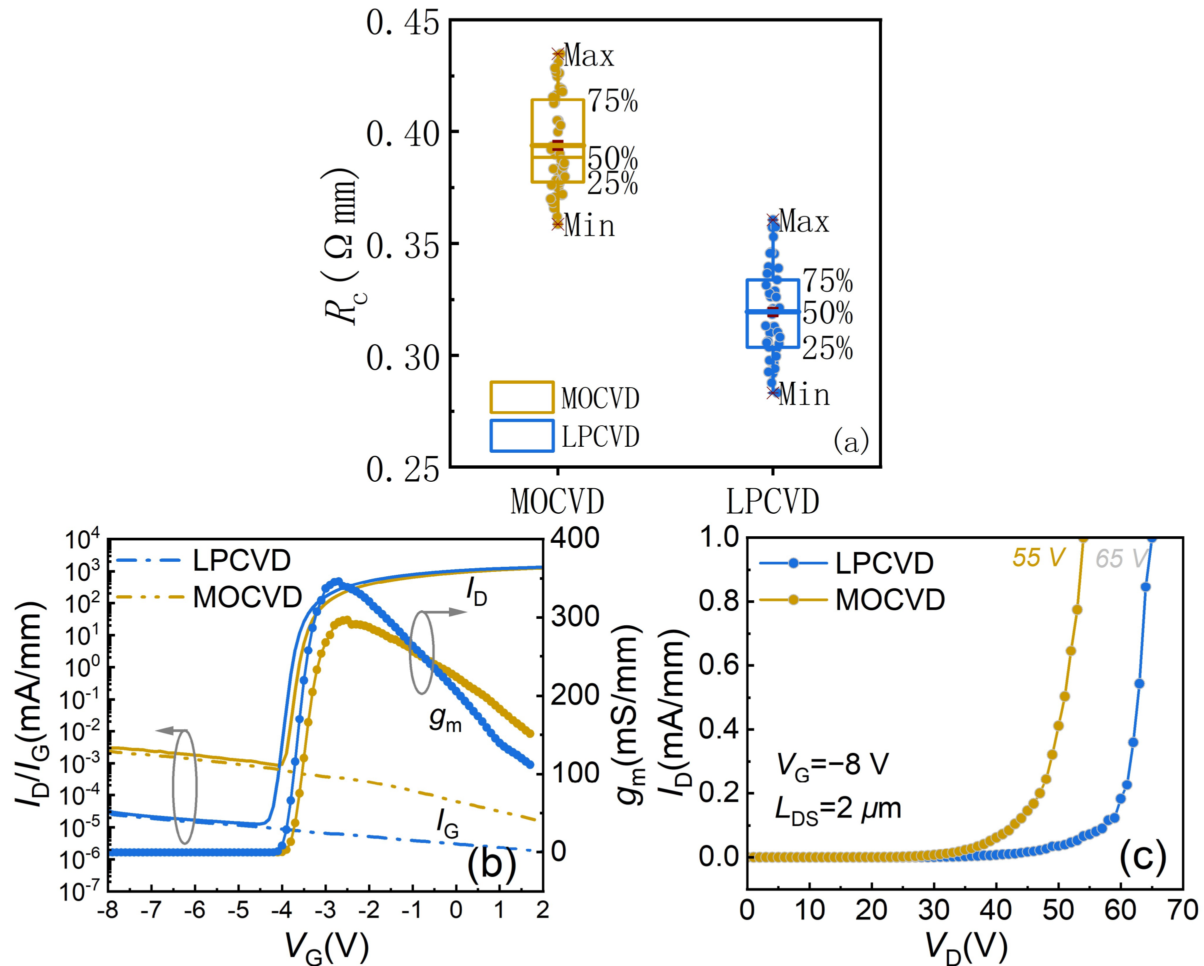


Figure 4. (**a**) TLM result of the MOCVD-SiN$_x$ and LPCVD-SiN$_x$ device. (**b**) Transfer I–V characteristics in semi-log scale of the MOCVD-SiN$_x$ and LPCVD-SiN$_x$ device. (**c**) Breakdown characteristics of the MOCVD-SiN$_x$ and LPCVD-SiN$_x$ devices.

Under the conditions of gate voltage (V_{gs}) = 2 V and drain voltage (V_{ds}) = 10 V, the maximum output currents were 1.28 A/mm and 1.34 A/mm for samples A and B, respectively. To minimize the influence of thermal resistance on on-resistance (R_{on}), the pulse test at a quiescent voltage of (0 V, 0 V) was performed with a 2 μm drain source spacing (L_{DS}) device. The measured R_{on} value for sample A was 1.75 Ω·mm and that for sample B was 1.54 Ω·mm. It can be seen that sample B had a lower R_{on}, which is consistent with the superior TLM results on sample B. Moreover, sample B, which lacks the diffusion of Si and etching damage, did not form an additional leakage path in passivation layers, resulting in relatively lower gate leakage current by 1–2 orders of magnitude below 10^{-5} mA/mm compared to sample A.

Figure 4c depicts the breakdown characteristics for the samples. At V_{gs} = −8 V, the breakdown voltage of sample A was measured to be 55 V for a 2 µm L_{DS} device, while the breakdown voltage of sample B was 65 V. This indicates that the excellent growth interface of LPCVD-SiN_x can generate a smoother electric field, thereby enhancing the breakdown characteristics of the device.

D. Pulsed I-V Characteristics

In RF applications, especially for an RF power output, the temperature of the working environment usually increases due to device heat dissipation. Therefore, to characterize the stability of the passivation layer, pulse I-V measurements were performed at room temperature of 25 °C and high temperature of 85 °C with a pulse width and a duty cycle of 500 ns and 0.05%, respectively. The voltage range of gate voltage (V_{GS}) was −4 to 2 V with a step of 3 V. The gate and drain quiescent bias (V_{GQ} and V_{DQ}) used for the pulse test is shown in Figure 5, ranging from (V_{GQ}, V_{DQ}) = (0 V, 0 V)~(−8 V, 20 V). Under room temperature conditions, the current collapse shown in Figure 5a of sample A was 7.8% for the high reverse gate voltage and high drain voltage condition of (−8 V, 20 V), while that of sample B shown in Figure 5b was 5.9%. At 85 °C, the current collapse of sample A was 7.4% (Figure 5c), while that of sample B was 6% (Figure 5d). Comparing the passivation effects between high and low temperatures, the variations observed were relatively insignificant and we thought that the discrepancy was a consequence of different surface trapping states at the interface to the SiN layer. The different growth methods and recipes for the passivation layer had a significant impact on the introduction of traps [32,33], and, in the future, we will focus on more accurate trap testing, like deep-level transient spectroscopy (DLTS), to demonstrate the differences in traps related to the two passivation layers. Nevertheless, both samples show excellent thermal stability and also show that sample B has a better passivation effect at either room temperature or at high temperatures. These results prove that the high-temperature process of SiN_x deposition is beneficial to improving the thermal stability of the passivation.

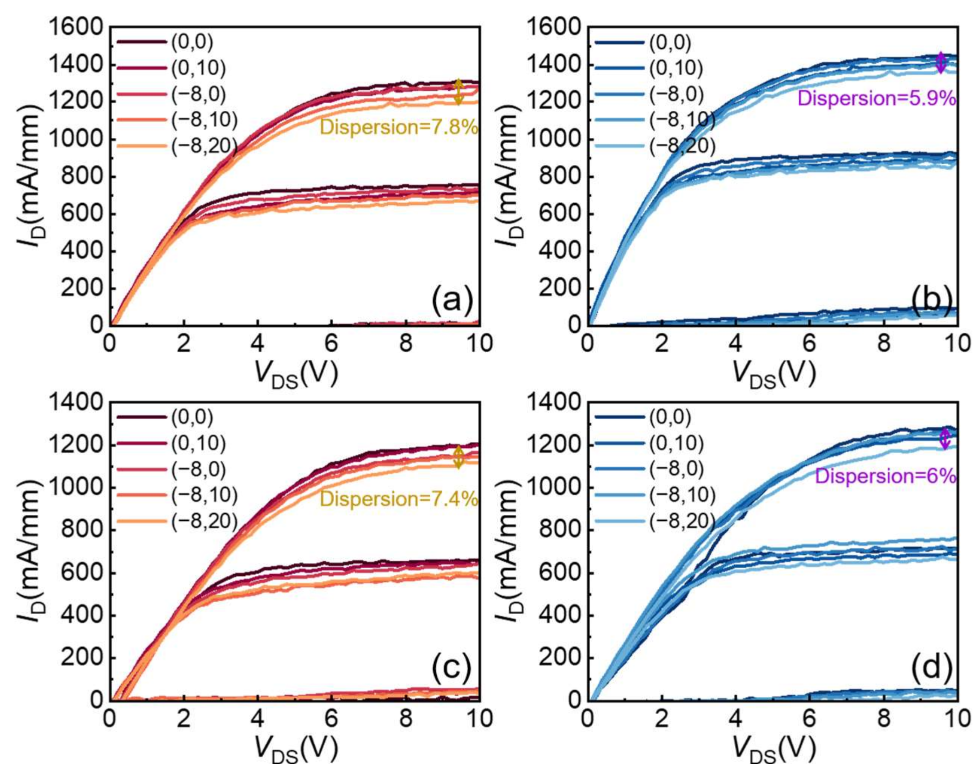


Figure 5. Pulsed output characteristic of (**a**) sample A and (**b**) sample B at 25 °C. Pulsed output characteristics of (**c**) sample A and (**d**) sample B at 85 °C.

E. Small- and Large Signal Power Characteristic

Small-signal measurements of the two samples are shown in Figure 6a,b. S-parameters were measured from 0.1 GHz to 40 GHz using a Keysight network analyzer. The current gain cutoff frequency f_T for sample A at V_{ds} = 20 V was 22 GHz, while that of sample B was 24 GHz. The maximum oscillation frequency f_{max} was 64 GHz in sample A and 72 GHz in sample B. The improvement of f_{max} may be ascribed to the better transconductance and reduced parasitic resistance deriving from low R_c in sample B [34].

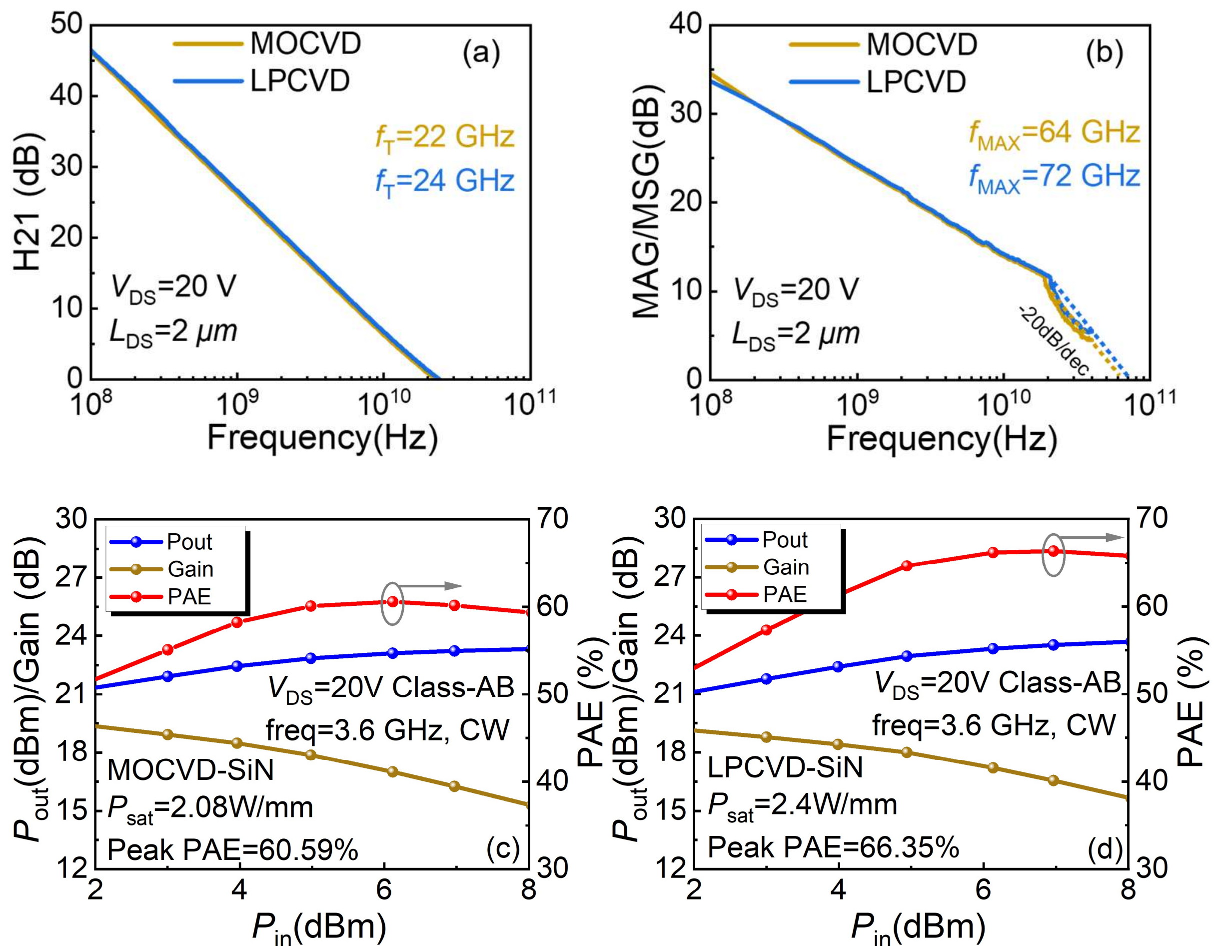


Figure 6. Small signal comparison between MOCVD- and LPCVD-SiN_x of (**a**) f_T and (**b**) f_{max}. Large-signal results of (**c**) the MOCVD-SiN_x device and (**d**) the LPCVD-SiN_x device.

CW load–pull measurements were measured at 3.6 GHz using a Focus load–pull system with class-AB bias. The impedance matching in the load-pull test is PAE optimum tuning. These results are shown in Figure 6c,d. It can be seen that sample B has better output power density and power-added efficiency (PAE). This is attributed to lower leakage current [35] and lower parasitic resistance [34] in sample B. According to the large-signal test, sample B exhibited a PAE of 66.35% under a drain voltage bias of 20 V, which is 6% higher than 60.59% of sample A. The sample B fabricated in this study exhibited significant efficiency advantages in low-voltage power output compared to other state-of-the-art LPCVD-SiN_x AlGaN/GaN HEMTs measured at a sub-6G condition, as shown in Figure 7 [18,25,36–38].

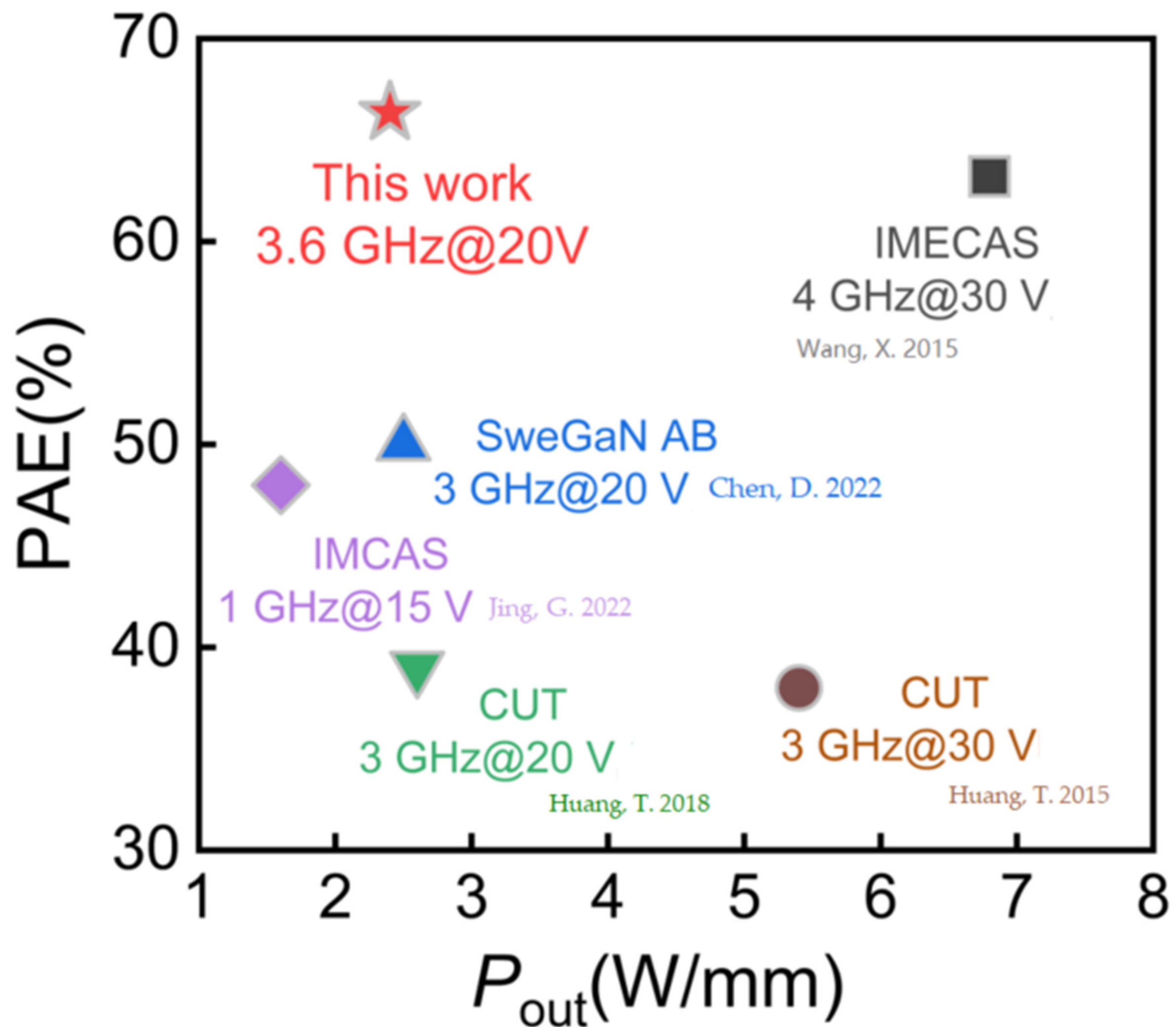


Figure 7. Benchmark of sub-6G high-signal power characteristics for state-of-the-art AlGaN/GaN HEMTs [18,25,36–38].

4. Conclusions

Due to the low-temperature characteristics of PECVD-SiNx, it cannot meet the requirements of an advanced "passivation-prior-to-ohmic" process. This study investigates SiNx passivation fabricated using two high-temperature deposition methods. In this paper, we compared the differences between MOCVD-SiN_x and LPCVD-SiN_x in terms of ohmic contact and related interface. We discovered that the growth interface of LPCVD-SiN_x was smoother than that of MOCVD-SiN_x, resulting in better leakage suppression. Additionally, LPCVD-SiN_x devices achieved improved RF output performance by forming lower Ohmic contact resistance. The maximum current of the LPCVD-SiN_x device exceeded 1.3 A/mm at V_{gs} = 2 V, with gate leakage below 10^{-5} mA/mm. The f_{max} of the 2 μm L_{DS} device reached 72 GHz. Under a drain voltage of 20 V, the output power exceeded 2.4 W/mm with PAE greater than 66.35%. The results presented in this study demonstrates significant efficiency advantages in low-voltage power output compared to other state-of-the-art LPCVD-SiNx AlGaN/GaN HEMT operated at 5G frequency spectrum. These results demonstrate the excellent performance of LPCVD-SiN_x devices in small-sized modules working in low-voltage applications and highlight its prospects in 5G small terminals.

Author Contributions: L.D.: investigation (equal); methodology (equal); writing—original draft (equal); and formal analysis (equal). L.Z.: investigation (equal); data curation; visualization (equal); and writing—review and editing (equal). H.L.: writing—review and editing (supporting). L.Y.: methodology (equal). Q.Y.: investigation (equal). M.Z.: methodology (equal). M.W.: validation (supporting). B.H.: methodology (equal). X.M.: funding acquisition (lead); project administration (lead); and supervision (lead). Y.H.: funding acquisition (lead) and supervision (lead). All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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