

## Article

# Electrically Doped PNP Tunnel Field-Effect Transistor Using Dual-Material Polarity Gate with Improved DC and Analog/RF Performance

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**Abstract:** A new structure for PNP tunnel field-effect transistors (TFETs) has been designed and simulated in this work. The proposed structure incorporates the polarity bias concept and the gate work function engineering to improve the DC and analog/RF figures of merit. The proposed device consists of a control gate (CG) and a polarity gate (PG), where the PG uses a dual-material gate (DMG) structure and is biased at  $-0.7$  V to induce a  $P^+$  region in the source. The PNP structure introduces a local minimum on the conduction band edge curve at the tunneling junction, which dramatically reduces the tunneling width. Furthermore, we show that incorporating the DMG architecture further enhances the drive current and improves the subthreshold slope (SS) characteristics by introducing an additional electric field peak. The numerical simulation reveals that the electrically doped PNP TFET using DMG improves the DC and analog/RF performances in comparison to a conventional single-material gate (SMG) device.

**Keywords:** tunnel FETs (TFETs); electrically doped; dual-material gate (DMG); band-to-band tunneling (BTBT); analog/RF performance



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## 1. Introduction

It has become increasingly difficult for the industry to continuously scale traditional Complementary Metal Oxide Semiconductor (CMOS) devices at the nanoscale level. At room temperature, the 60 mV/dec subthreshold slope acts as a limit on transistor scaling in Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs). One such candidate is the Tunnel Field-Effect Transistor (TFET), whose subthreshold slope value at room temperature is less than 60 mV/decade [1]. In addition to these advantages, TFETs have two major disadvantages, namely low on-state current ( $I_{ON}$ ) and ambipolarity during switching [2]. In order to overcome  $I_{ON}$  and the ambipolar issue, we have recently proposed an in-built  $N^+$  pocket electrically doped TFET (ED-TFET) with and without an electrically doped drain, using the concept of polarity bias [3,4]. An in-built  $N^+$  pocket ED-TFET structure is very similar to a PNP TFET structure, except that it does not require additional chemical doping for the narrow  $N^+$  pocket [5,6]. By applying a bias voltage at both the polarity gate and control gate, the principle of the polarity bias concept induces charge carriers that modulate tunneling barriers [7,8]. Consequently, no additional doping processes are required to build a narrow  $N^+$  pocket, thereby simplifying the manufacturing process [9].

In previous works, simulation studies have demonstrated that by replacing the single-material control gate structure in the double-gate TFET with a dual-material control gate structure, both the ON-current and subthreshold slope (SS) characteristics of the TFETs

could be significantly improved [10,11]. For example, a new structure of Schottky tunneling MOSFET has been designed and simulated using floating gates and dual-material main gates to counter short-channel effects and improve analog/RF performances [12]. In addition, a dual-material control gate with dual-oxide TFET has been investigated with reduced ambipolar behavior and subthreshold swing [13]. Furthermore, an analytical model of a dual-material single-gate doping-less TFET with gate underlap regions has been proposed [14]. A dual-material gate GaAs/InAs/Ge junctionless TFET has been proposed based on intraband tunneling and interband tunneling with improved SS and  $I_{ON}$  [15]. A dual-material gate-oxide-stack double-gate TEFT has also been investigated as a biosensing element, and the underlying device sensitivity has been estimated [16]. However, the effect of dual-material polarity gates on TFET devices has not yet been investigated.

We present the application of a dual-material polarity gate (DMPG) to an in-built  $N^+$  pocket ED-TFET in this paper. In 2D device simulations, we demonstrate that engineering the dual-polarity gates' work functions enables the optimization of the ON-current  $I_{ON}$ , the OFF-current  $I_{OFF}$ , and the average subthreshold slope and analog/RF performance by simultaneously optimizing the work functions of the dual-polarity gates.

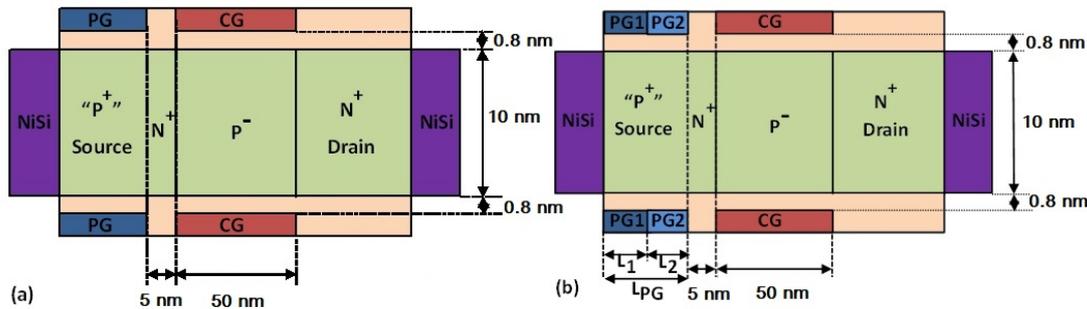
In this work, we investigate the device design and DC and analog/RF performances of the proposed DMPG ED-TFET with regard to several key parameters. A description of the physical structure used in the simulation is presented in Section 2. In Section 3, comparative results and analyses are presented. Finally, Section 4 summarizes the paper.

## 2. Device Structure and Simulation Model

Figure 1a,b illustrate the cross-sectional views of the conventional single-material polarity gate (SMPG) ED-TFET and the proposed dual-material polarity gate (DMPG) ED-TFET. In both types of devices, there are two sets of gate electrodes: control gates (CG) and polarity gates (PG). For comparison, an SMPG ED-TFET with the same channel length is used. The proposed DMPG ED-TFET has two polarity gates with different work functions, denoted by PG1 and PG2, which are set to 4.97 and 4.5 eV, respectively, corresponding to the values of some common metals, as shown in Figure 1b. Initially,  $L_1$  and  $L_2$  are set to 20 nm, and the total length of the polarity gate is fixed at 40 nm. In Table 1, we show the detailed design parameters we used in our simulation. During the simulation, the lengths and work functions of the two polarity gates can be varied. As shown in Table 1, both devices have the same doping concentration at the source, channel, and drain, with a starting NPN structure. A PNP TFET structure is achieved by setting up polarity gates on the source side of the device based on the polarity bias concept. The narrow  $N^+$  pocket is, therefore, built into the device without the need for additional doping processes, thereby simplifying manufacturing. In general, the proposed DMPG ED-TFETs have the same working mechanism as the conventional SMPG ED-TFETs, except for the dual-material polarity gate configuration. In Figure 2, the energy band diagrams for the proposed DMPG and conventional SMPG ED-TFET at 1 nm below the Si-oxide interface are shown. It appears that the conduction energy band edge ( $E_C$ ) at  $V_{CG} = 0$  V has a local minimum point. By aligning the local minimum with the valence energy band edge ( $E_V$ ) at the source, the introduction of the  $N^+$  pocket results in a decrease in the  $E_C$  curve and a rapid decrease in the tunneling barrier width. However, the incorporation of the DMPG leads to a reduction in the local  $E_C$  minimum, as shown in Figure 2, and the tunneling barrier width can be further reduced due to the work function modulation of the DMPG.

In this paper, we used the Silvaco Atlas device simulation software (version 5.19.20.R) [17] to perform all the simulations. Based on [18], we validated our simulation model using a non-local band-to-band tunneling (BTBT) model. Based on the analysis of the energy band diagrams, a non-local BTBT model was used to calculate the tunneling probability along the lateral direction of the device. A fine mesh was used across the region of tunneling in the simulations to perform non-local BTBT. Approximating the evanescent wavevector was performed by Atlas using the Wentzel–Kramers–Brillouin method. To include the effect of the electric field on mobility degradation, we used the Lombardi mobility model. In

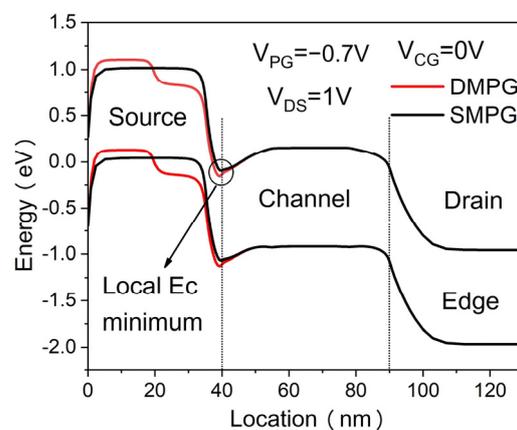
addition, Fermi Dirac and the Shockley–Read–Hall (SRH) recombination models were used. In order to account for the high concentration of doping in the devices, a band-gap narrowing (BGN) model was used. Because the thickness of the silicon film exceeded 7 nm, quantum mechanical effects were not taken into account [19,20].



**Figure 1.** Cross-sectional views of (a) the conventional SMPG ED-TFET and (b) the proposed DMPG ED-TFET.

**Table 1.** Parameters used for device simulation.

Parameter	Conventional SMPG ED-TFET [3]	Proposed DMPG ED-TFET
Source Doping	$4 \times 10^{19} \text{ cm}^{-3} (\text{N}^+)$	$4 \times 10^{19} \text{ cm}^{-3} (\text{N}^+)$
Channel Doping	$1 \times 10^{17} \text{ cm}^{-3} (\text{P}^-)$	$1 \times 10^{17} \text{ cm}^{-3} (\text{P}^-)$
Drain Doping	$5 \times 10^{18} \text{ cm}^{-3} (\text{N}^+)$	$5 \times 10^{18} \text{ cm}^{-3} (\text{N}^+)$
CG Work function	4.74 eV	4.74 eV
PG Work function	4.33 eV	-
PG1 Work function	-	4.97 eV
PG2 Work function	-	4.5 eV



**Figure 2.** Energy band diagrams of DMPG and SMPG ED-TFET at 1 nm below the Si/oxide interface.

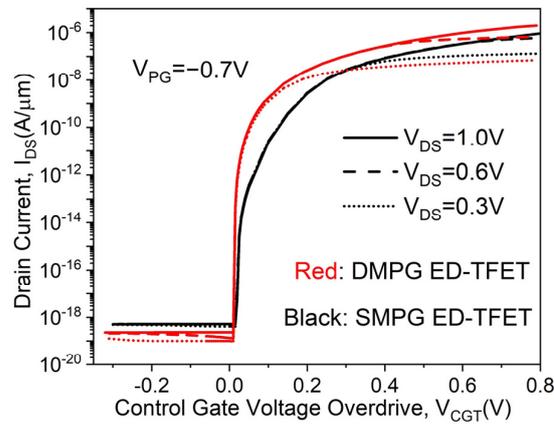
### 3. Simulation Results and Discussion

The DC and analog/RF characteristics of the proposed DMPG ED-TFET are investigated and compared with those of a corresponding compatible SMPG ED-TFET. The influences of the key parameters are further analyzed in this section.

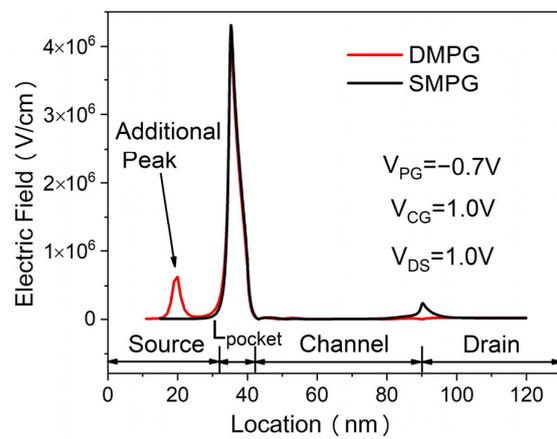
#### 3.1. DC Characteristics

The transfer characteristics of the proposed DMPG ED-TFET and conventional SMPG ED-TFET for various drain voltages are shown in Figure 3. The control gate voltage overdrive  $V_{CGT}$  is defined as  $V_{CGT} = V_{CG} - V_{TH}$ , where  $V_{CG}$  is the control gate voltage and  $V_{TH}$  is the threshold voltage referring to the control gate voltage when the device is turned on. It is clearly seen from Figure 3 that the SS is significantly improved in the proposed device and  $I_{ON}$  (calculated at  $V_{CG} = V_{DS} = 1.0 \text{ V}$ ,  $V_{PG} = -0.7 \text{ V}$ ) is also higher.

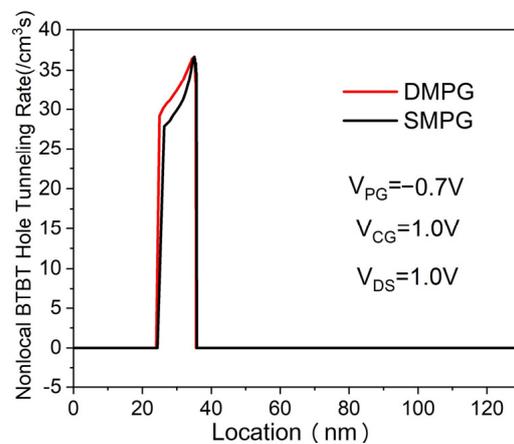
This can be explained using the electric field distributions, which are shown in Figure 4. By using the dual-material polarity gates of work functions 4.97 eV and 4.5 eV in the proposed device, an additional peak electric field is created in the source region, which provides more acceleration to the tunneling carrier and enhances the non-local BTBT hole tunneling rate near the  $N^+$  pocket, as shown in Figure 5.



**Figure 3.** Transfer characteristics of the proposed DMPG ED-TFET and conventional SMPG ED-TFET for various  $V_{DS}$ .



**Figure 4.** Electric field distributions of DMPG and SMPG ED-TFET at 1 nm below the Si/oxide interface.



**Figure 5.** Non-local BTBT hole tunneling rate of DMPG and SMPG ED-TFET at 1 nm below the Si/oxide interface.

### 3.2. Device Optimizations

The transfer characteristics of the proposed DMPG ED-TFET for various PG2 work functions ( $\Phi_{PG2}$ ) are shown in Figure 6. The PG1 work function is fixed at 4.97 eV. The  $\Phi_{PG2} = 4.97$  eV corresponds to that of the SMPG ED-TFET. As shown in Figure 6, both  $I_{ON}$  and SS increase and the devices turn on at a lower control gate voltage with increasing  $\Phi_{PG2}$ . We show the energy band diagrams of the proposed DMPG ED-TFET for various PG2 work functions at 1 nm below the Si/oxide interface in the OFF-state in Figure 7. For clarity, the band diagram near the local  $E_C$  minimum is enlarged. From Figure 7, it can be seen that increasing the PG2 work function leads to a reduced depth of the  $E_C$  well where the local minimum point is located, which results in band-to-band tunneling difficulties. Thus, SS degrades considerably when  $\Phi_{PG2}$  reaches 4.97 eV. Considering  $I_{ON}$  and SS, the optimal work function of PG2 is 4.5 eV when keeping the work function of PG1 fixed at 4.97 eV.

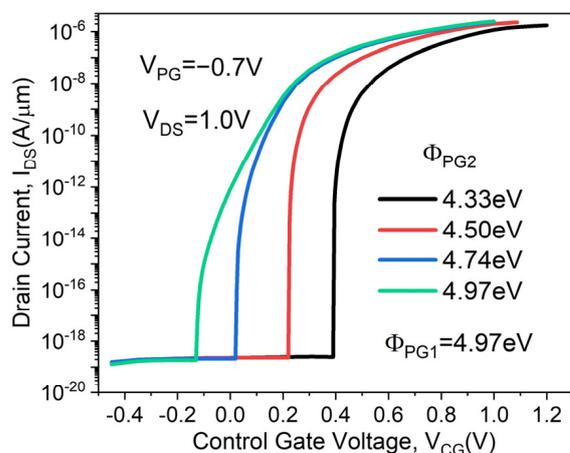


Figure 6. Transfer characteristics of the proposed DMPG ED-TFET for various PG2 work functions.

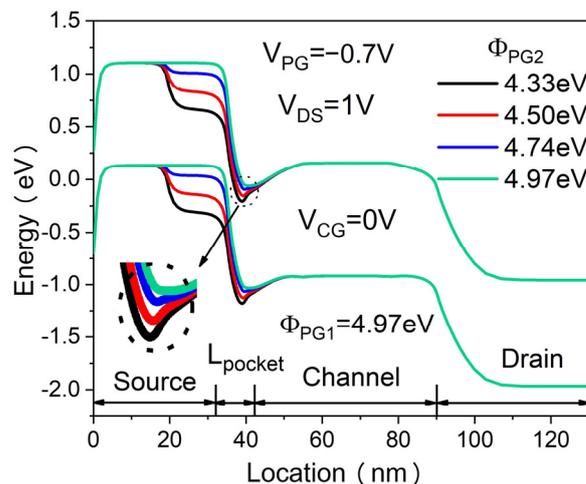


Figure 7. Energy band diagrams of the proposed DMPG ED-TFET for various PG2 work functions at 1 nm below the Si/oxide interface.

Figure 8 shows the transfer characteristics of the proposed DMPG ED-TFET for various PG1 work functions ( $\Phi_{PG1}$ ) while keeping  $\Phi_{PG2}$  fixed at 4.5 eV. The  $\Phi_{PG1} = 4.5$  eV corresponds to that of the SMPG ED-TFET. In general, the OFF-state current  $I_{OFF}$  (calculated at  $V_{CG} = 0$  V,  $V_{DS} = 1.0$  V,  $V_{PG} = -0.7$  V) decreases with increasing  $\Phi_{PG1}$ , as shown in Figure 8. However, SS,  $V_{TH}$ , and  $I_{ON}$  are virtually unchanged since  $\Phi_{PG2}$  is fixed. This can be explained by the fact that in the ON-state, the band-to-band tunneling occurs at the junction between the source region and pocket. Thus, an increase in  $\Phi_{PG1}$  does not change

the band diagram near tunneling significantly. The device with  $\Phi_{PG1}$  of 4.97 eV has the lowest  $I_{OFF}$ , as shown in Figure 8. This can be understood from the electron concentration distribution for different PG1 work functions in the OFF-state. In the case of the proposed device with  $\Phi_{PG1} = 4.97$  eV, the electron concentration in the channel shows the lowest value, as illustrated in Figure 9. This reduced electron concentration affects the conduction band profile in the OFF-state. As a result, the conduction band well becomes wider, resulting in a lower  $I_{OFF}$ . When the PG2 work function is fixed at 4.5 eV, the optimal PG1 work function is 4.97 eV.

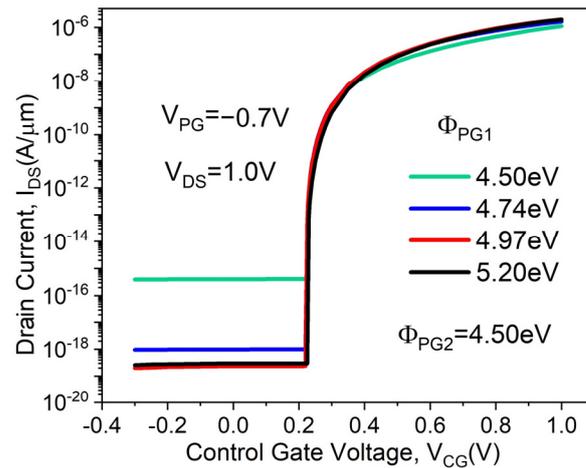


Figure 8. Transfer characteristics of the proposed DMPG ED-TFET for various PG1 work functions.

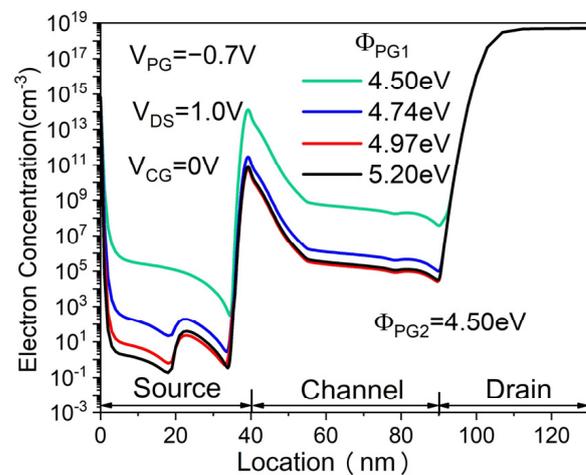


Figure 9. Electron concentration of the proposed DMPG ED-TFET for various PG1 work functions.

The transfer characteristics of the proposed DMPG ED-TFET are studied when the  $L_2/L_{PG}$  ratio is varied from 0.25 to 0.875 by changing  $L_2$  from 10 to 35 nm with a fixed polarity gate length of  $L_{PG} = L_1 + L_2 = 40$  nm, as shown in Figure 10. It is evident that SS degradation occurs when the  $L_2/L_{PG}$  ratio is 0.25 and 0.375. The SS is almost consistent when the  $L_2/L_{PG}$  ratio exceeds 0.5; however, as the ratio increases,  $I_{OFF}$  increases as well. For all  $L_2/L_{PG}$  ratios,  $I_{ON}$  is essentially the same. In Figure 11, the characteristics of the SS and ON/OFF current ratios ( $I_{ON}/I_{OFF}$ ) for the DMPG ED-TFET devices are shown. It can be observed that the lowest SS and the highest  $I_{ON}/I_{OFF}$  occur at  $L_2/L_{PG} = 0.5$ . Considering the SS and  $I_{ON}/I_{OFF}$ , as well as the actual photolithography conditions,  $L_2/L_{PG} = 0.5$  seems to be a reasonable optimal value for the proposed DMPG ED-TFET.

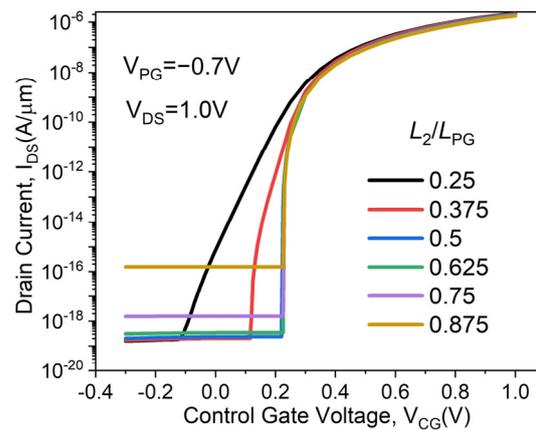


Figure 10. Transfer characteristics of the proposed DMPG ED-TFET for various  $L_2/L_{PG}$  ratios.

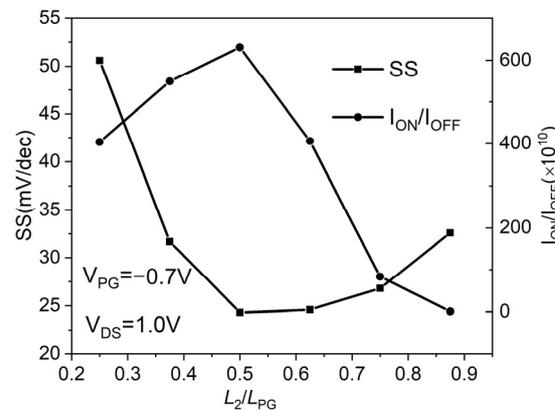
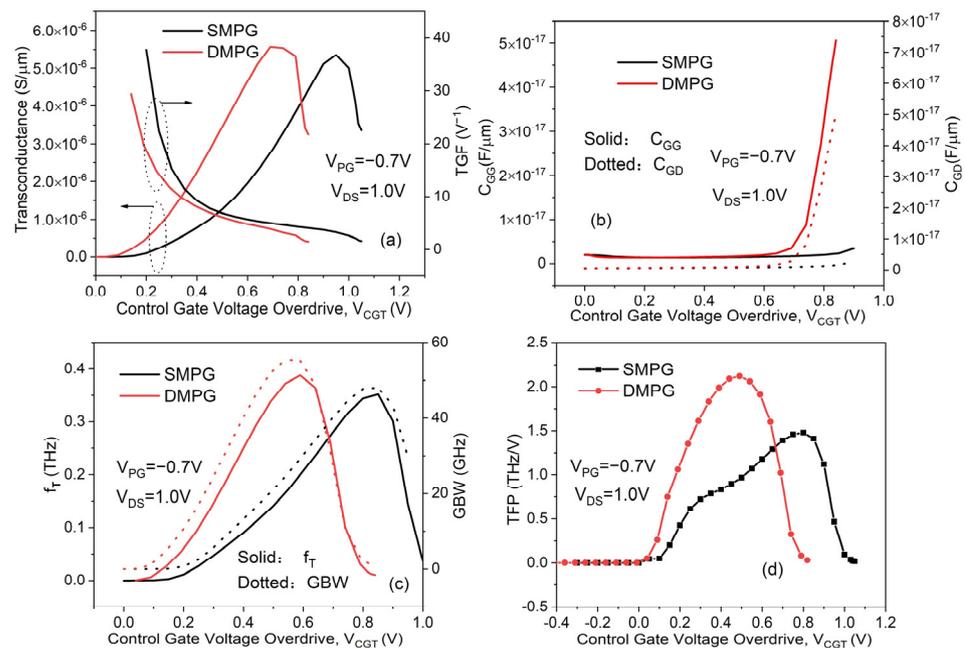


Figure 11. SS and  $I_{ON}/I_{OFF}$  of the proposed DMPG ED-TFET for various  $L_2/L_{PG}$  ratios.

### 3.3. Analog/RF Performance

We simulate and compare the analog/RF performance of the proposed DMPG ED-TFETs with that of the conventional SMPG ED-TFETs with identical dimensions, as shown in Figure 12. An analog/RF figure of merit (FoM) consists of the following: transconductance ( $G_m$ ), transconductance generation factor (TGF), gate capacitance ( $C_{GG}$ ), gate–drain capacitance ( $C_{GD}$ ), cutoff frequency ( $f_T$ ), gain bandwidth product (GBW), and transconductance frequency product (TFP). For fair comparisons, the same  $V_{CGT}$  is used to subtract the effect of the threshold voltage.

This can be expressed as  $G_m = dI_{DS}/dV_{CG}$ , where  $G_m$  is the slope of the  $\log(I_{DS})-V_{CG}$  curve when  $V_{DS}$  remains at 1.0 V. In analog circuits, transconductance is crucial for achieving high gains and  $f_T$ . As shown in Figure 12a, the  $G_m$  of the DMPG ED-TFET is larger than that of the SMPG device. The improved SS of the DMPG structure results in a significant change in  $I_{DS}$  with  $V_{CG}$ , whereas  $I_{ON}$  maintains a high value, resulting in a greater  $G_m$ . Furthermore,  $G_m$  increases as  $V_{CGT}$  is increased until saturation occurs. The maximum  $G_m$  of the proposed DMPG and conventional SMPG ED-TFETs are 5.57 and 5.35  $\mu\text{S}/\mu\text{m}$ , respectively. Both devices' transconductance drops rapidly when they enter the saturation region ( $V_{CGT}$  of 0.69 V for DMPG, 0.95 V for SMPG). A device's efficiency can also be quantified by TGF, which represents  $G_m$  divided by the  $I_{DS}$ . Figure 12a also shows TGF with varying  $V_{CGT}$  for the DMPG and SMPG devices. We can see that the proposed DMPG device has a lower TGF because  $G_m$  is less dominant than the drain current. Therefore, in spite of the higher  $G_m$  of DMPG, TGF remains relatively small. As  $V_{CGT}$  increases, the drain current increases rapidly, and the TGF decreases accordingly.



**Figure 12.** Variation in (a) transconductance and TGF, (b)  $C_{GG}$  and  $C_{GD}$ , (c)  $f_T$  and GBW, and (d) TFP versus  $V_{CGT}$  of the conventional SMPG and proposed DMPG ED-TFET.

As we know, capacitance is an important parameter closely related to the power consumption and switching speed characteristics of transistors. Therefore, variations in  $C_{GG}$  and  $C_{GD}$  with respect to  $V_{CGT}$  of both the proposed DMPG and conventional SMPG ED-TFETs are shown in Figure 12b. It has been observed that  $C_{GG}$  and  $C_{GD}$  in the proposed DMPG device are higher than those in the conventional SMPG device. When  $V_{CGT}$  exceeds 0.6 V, both capacitances of the DMPG device increase rapidly as  $V_{CGT}$  increases. For the SMPG devices, the capacitances increase slowly. Other important parameters for RF applications are the cutoff frequency ( $f_T$ ) and the gain bandwidth product (GBW). At the cutoff frequency, the short-circuit current gain reaches unity and is represented by  $f_T = Gm/2\pi C_{GG}$ . For high-frequency circuits, it is generally beneficial to have a high  $f_T$  to ensure that the device can be used widely. The GBW can be expressed as a ratio of  $Gm$  to  $C_{GD}$  for a DC gain value equal to 10, and it is represented by  $GBW = Gm/2\pi 10 C_{GD}$ . It can be inferred from Figure 12c that both  $f_T$  and GBW are improved in the DMPG ED-TFET, which is similar to the trends in Figure 12a. Based on the formulas listed above, the values of  $f_T$  and GBW are both proportional to  $Gm$ , so the changing trends are also similar. As  $V_{CGT}$  further increases,  $Gm$  drops sharply and the capacitance increases, resulting in a decrease in  $f_T$  and GBW. The proposed DMPG and conventional SMPG ED-TFETs achieve a maximum  $f_T$  of 0.388 and 0.352 THz, and a maximum GBW of 55.52 and 48.01 GHz at  $V_{CGT}$  of 0.59 V and 0.85 V, respectively.

Another important FoM for high-frequency circuits is the TFP, which is essentially calculated by multiplying the TGF by the  $f_T$ , or  $TFP = (Gm/I_{DS}) \times f_T$ . As shown in Figure 12d, the proposed DMPG ED-TFET exhibits higher TFP values than the conventional SMPG ED-TFET due to its higher  $f_T$ . The DMPG and SMPG devices achieve a maximum TFP of 2.12 and 1.48 THz/V at  $V_{CGT}$  of 0.49 V and 0.8 V, respectively. Compared to conventional SMPG ED-TFETs for low-voltage circuits, the proposed DMPG ED-TFETs appear to be more suitable for RF applications.

#### 4. Conclusions

In this paper, we presented a device structure that incorporates a dual-material gate in a PNP ED-TFET based on the polarity bias concept. The dual-material gate was used on the polarity gate, which was biased at  $-0.7$  V to induce a  $P^+$  region in the source. By introducing an additional electric field peak, we demonstrated that the DMPG architecture

further improves the drive current and SS characteristics. Furthermore, the device design was optimized by modulating the work functions of PG1 and PG2 and the  $L_2/L_{PG}$  ratio. In general,  $L_2/L_{PG} = 0.5$ , PG1 work function  $\Phi_{PG1} = 4.97$  eV, and PG2 work function  $\Phi_{PG2} = 4.5$  eV are recommended for DMPG ED-TFET. Two-dimensional simulations were used to evaluate DC and analog/RF performance. The simulated performance of the DMPG ED-TFET performed better than that of the conventional SMPG ED-TFET at the optimized dimensions of SS,  $I_{ON}$ ,  $Gm$ , TGF,  $f_T$ , GBW, and TFP in low-voltage situations. Based on this, we anticipate that the circuit performance would be better with the DMPG architecture.

**Author Contributions:** Conceptualization and methodology, C.S.; software, Y.L.; validation, L.S.; investigation, C.S.; writing—review and editing, Y.W.; data curation, R.C. All authors have read and agreed to the published version of the manuscript.

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**Data Availability Statement:** The data presented in this study are available on request from the corresponding author. The data are not publicly available due to privacy.

**Conflicts of Interest:** The authors declare no conflict of interest.

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