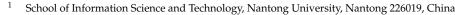


Article A Balanced Substrate Integrated Waveguide Phase Shifter with Wideband Common-Mode Suppression

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Abstract: In this paper, a slotted substrate integrated waveguide (SIW) is used to create a balanced phase shifter with wideband common-mode (CM) suppression. Differential-mode (DM) impedance matching and CM suppression are achieved by utilizing the fact that TE_{20} mode and TE_{10} (TE_{30}) mode can only transmit DM signals and CM signals, respectively, and by increasing the bandwidth for CM suppression via slots. Furthermore, a wideband phase shift with low phase deviation can be obtained due to the phase slop counteract between the slot and the delay line. Compared with the state-of-the-art, the proposed one has the advantages of wideband CM suppression, wide phase shift range, and a simple and easy-to-make structure. Five prototypes covering the frequency of 3.5 GHz are designed with the relative operating bandwidth for $45^{\circ} \pm 2^{\circ}$ ($90^{\circ} \pm 4.5^{\circ}$, $135^{\circ} \pm 6^{\circ}$, and $180^{\circ} \pm 8^{\circ}$) phase shifter of 20% (20%, 20%, and 20%), with the minimum insertion loss of 0.41 dB (0.5 dB, 0.58 dB, and 0.59 dB), with the minimum return loss greater than 15 dB, and with the relative bandwidth for 15-dB CM suppression of 59% (59%, 58%, and 57%).

Keywords: balanced phase shifter; common-mode suppression; substrate integrated waveguide; wideband

1. Introduction

Phase shifters play crucial roles in wireless communication systems, such as radar, phase modulators, beamforming networks, and phased array antenna systems, because they can provide the required phase shifts [1–3]. The increasing popularity of balanced phase shifters is due to their high immunity to electromagnetic interference and their simple connection to other balanced circuits or antennas. In addition to the advantages of the balanced microstrip phase shifter, the balanced substrate integrated waveguide (SIW) phase shifter has high-quality factors, a high power handling capacity, and low loss. Consequently, the balanced SIW phase shifter will be in high demand in modern communication systems. Balanced SIW phase shifter design challenges include wideband CM suppression while preserving wideband DM phase shift, low in-band phase deviation, and low insertion loss.

Currently, a few balanced phase shifters have been reported [4–11], and all of them are microstrip designs. Several approaches have been used to design microstrip balanced phase shifters, including coupled lines with loaded transmission lines [4–6], two-stage branch line structure [7], cascaded three microstrip lines and two coupled lines [8], T-shaped multi-mode resonator with intermediate cascaded stubs [9], two three-end folded coupled lines with three half-wavelength microstrip lines [10], LC-based microstrip differential line with periodic T-shaped stubs [11], etc. Among them, different features have been achieved, such as compact size in [4,6], wideband CM suppression in [8], large phase shift range in [7,9], fusing filtering function in [5,10], and tunable phase shift in [11].



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Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). To our knowledge, no balanced SIW phase shifter has been reported till now. Various single-ended SIW phase shifters have been reported [12–24], and their design methods can be categorized as inserted metallic posts [12–14], buried PIN diodes [15], embedded omega particles [16], CSRR-loaded SIW [17], air-filled SIW loaded with dielectric slab [18], loaded rod-shaped artificial dielectric slabs [19], slow-wave structures [20], slotted SIW [21,22], varactor-loaded slotted SIW [23], transverse slot coupling [24], and so on. Among the aforementioned SIW phase shifters, some designs pursue equal lengths of the reference and main lines ([12,13,15,17]), some designs obtain wide operating bandwidths ([14,16,19–21]), some designs attain low insertion loss ([18,22]), and some designs realize tunable phase shift ([23,24]).

This paper constructs a balanced SIW phase shifter with wideband CM suppression by combining slotted SIW and microstrip delay lines. It is possible to simultaneously achieve wideband DM impedance matching, wideband phase shift with low in-band phase deviation, and wideband CM suppression. The equivalent circuit of the centred slot on the SIW and the surface current distributions of the SIW with/without slots are analysed to introduce the functions of the slots on the top surface of the SIW. The parametric study and the design procedure are provided to guide the practical design. Five prototypes are fabricated to verify the theoretical prediction.

2. Proposed Balanced SIW Phase Shifter

2.1. Structure

The proposed balanced SIW phase shifter is constructed by etching two symmetrical transverse slots into the top surface of SIW, as shown in Figure 1. Two pairs of symmetric microstrip lines form the two balanced ports, namely 1+ and 1-, 2+ and 2-, and the microstrip feed lines, which serve as delay lines. The reference and main lines employ the same circuit model on the RO4003C substrate (the dielectric constant of 3.38, thickness of 0.813 mm, and loss tangent of 0.0027). The lengths of the delay lines and the slot parameters distinguish the reference line from the main line.

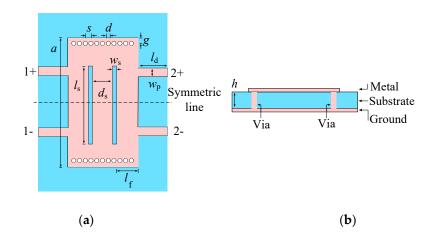


Figure 1. Structure of the proposed balanced SIW phase shifter. (a) Top view. (b) Cross-sectional view.

An SIW is equivalent to a conventional dielectric-filled metallic rectangular waveguide, and the equivalent relationship can be described as [25]:

$$w_{\rm eff} = a - \frac{d}{0.95s} \tag{1}$$

where w_{eff} is the equivalent width of the SIW compared with its conventional rectangular counterpart, *a* is the SIW width, and *d* and *s* are the diameter of metallic vias and the space between adjacent metallic vias, respectively. The dimensions of *a*, *d*, and *s* should follow the rules given in [26].

To achieve the transmission of DM signals and the suppression of CM signals at the centre frequency (f_0), the distance between ports 1+(2+) and 1-(2-) is set to half the equivalent width of the SIW. In addition, the relationship between f_0 and the cut-off frequencies of TE₂₀ mode and TE₃₀ mode must be satisfied as:

$$f_{c(TE_{20})} < f_0 < f_{c(TE_{30})}$$
 (2)

Thus, $w_{\rm eff}$ can also be expressed as:

$$\frac{c_0}{f_0\sqrt{\varepsilon_r}} < w_{\rm eff} < \frac{3c_0}{2f_0\sqrt{\varepsilon_r}} \tag{3}$$

Therefore, $w_{\rm eff}$ can be obtained according to f_0 . Conversely, f_0 can be controlled by $w_{\rm eff}$.

2.2. DM Analysis

Figures 2 and 3 illustrate the uniform amplitude distributions and vector distributions of the surface current on the SIW with/without slots for DM operating at f_0 to determine the effects of slots on DM properties. Figures 2 and 3 demonstrate that the TE₂₀ mode will be excited when the proposed design is operating at the DM. In addition, Figure 2 reveals that the surface current on the SIW without slots is distributed uniformly in the transmission direction, whereas the surface current on the SIW with two slots in Figure 3 is disturbed by the slots. It can be observed from Figure 3 that the transmission paths of the surface current on the upper and lower edges of the SIW are changed, and the surface current avoids the slots when transmitting forward. In addition, the surface current in the middle position of the SIW is transmitted through the slots' coupling. Therefore, the slots will change the transmission mechanism and the distributions of the surface current on the SIW; this is because a centred slot on the top surface of SIW can be equivalent to a circuit with a susceptance (*B*) and a conductance (*G*) in parallel [27], as shown in Figure 4, where *B* and *G* can be written as Equations (4)–(13).

$$G = Y_0 \frac{32\lambda_g w_{\text{eff}} b}{3\lambda^3 \pi} [1 - 0.374 (\frac{l_s}{\lambda})^2 + 0.13 (\frac{l_s}{\lambda})^4] [\frac{\pi}{4} \frac{1 - (l_s / w_{\text{eff}})^2}{\cos(\pi l_s / 2w_{\text{eff}})}]^2$$
(4)

$$B = Y_0 \left\{ \frac{1}{2} \frac{B_t}{Y_0} + \frac{B_{rj}}{Y_0} \frac{1}{n_j^2} + \frac{2b}{\lambda_g} \left[\ln 2 + \frac{\pi w_s}{6b} + \frac{3}{2} (\frac{b}{\lambda_g})^2 \right] \right\}$$
(5)

where *b* is the thickness of the substrate, and

$$B_{t} = Y_{0} \left\{ \frac{4b}{\lambda_{g}} \left[\ln \csc \frac{\pi w_{s}}{2b} + \frac{1}{2} (\frac{b}{\lambda_{g}})^{2} \cos^{4}(\frac{\pi w_{s}}{2b}) \right] - \frac{4b}{\lambda_{g}} (\frac{\lambda_{g}}{\lambda_{g3}})^{2} \left[1 + (\frac{\pi w_{s}}{2\lambda_{g3}})^{2} \right] \left[\frac{(1 - (\frac{l_{s}}{w_{\text{eff}}})^{2}) \cos(\frac{3\pi l_{s}}{2w_{\text{eff}}})}{(1 - 9(\frac{l_{s}}{w_{\text{eff}}})^{2}) \cos(\frac{\pi l_{s}}{2w_{\text{eff}}})} \right]^{2} \ln(\frac{4\lambda_{g3}}{1.781\pi w_{s}}) \right\}$$
(6)

$$\lambda_{g3} = \frac{\lambda}{\sqrt{1 - \left(\frac{3\lambda}{2w_{\text{eff}}}\right)^2}} \tag{7}$$

$$B_{rj} = Y_0 \frac{2w_s \lambda_g}{\lambda^2} \left\{ \left(\frac{\kappa'}{k}\right)^2 [C + 1.5 - \ln\frac{\gamma |\kappa'| w_s}{2}] + \frac{\sin(kl_s)}{kl_s} + \left[1 + \left(\frac{\lambda}{2l_s}\right)^2\right] (S_-) - \frac{2w_s}{3l_s} \left(\frac{\lambda}{2l_s}\right)^2 \right\}$$
(8)

$$C = \frac{C_i(kl_s + \pi) + C_i|kl_s - \pi|}{2}$$
(9)

$$S_{-} = \frac{S_i(kl_s + \pi) - S_i(kl_s - \pi)}{2\pi}$$
(10)

$$S_i(x) = \int_0^x \frac{\sin t}{t} dt \tag{11}$$

$$C_i(x) = \int_0^x \frac{\cos t}{t} dt \tag{12}$$

$$\frac{1}{n_j^2} = \frac{w_{\rm eff}b}{l_{\rm s}w_{\rm s}} \left[\frac{\pi}{4} \frac{1 - (l_{\rm s}/w_{\rm eff})^2}{(\pi l_{\rm s}/2w_{\rm eff})^2}\right]^2 \tag{13}$$

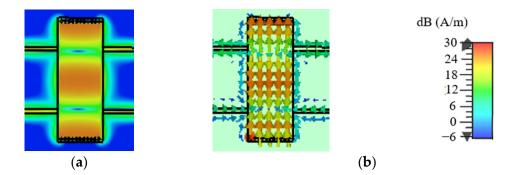


Figure 2. The surface current distributions on the SIW without slots for DM operating at f_0 . (a) The uniform amplitude distributions. (b) The vector distributions.

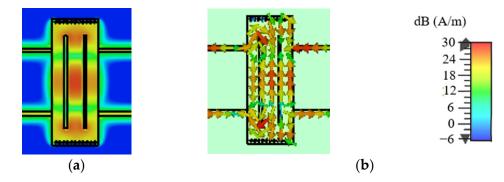


Figure 3. The surface current distributions on the SIW with two slots for DM operating at f_0 . (a) The uniform amplitude distributions. (b) The vector distributions.

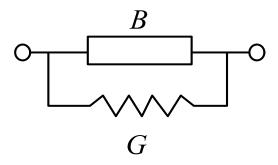


Figure 4. The equivalent circuit of the centred slot on the top surface of SIW.

According to Equations (4)–(13), the values of *B* and *G* are mainly determined by the parameters of the SIW and the slots. Thus, to further study how the parameters of slots on the SIW affect the properties of DM impedance matching and DM phase shift of the proposed balanced SIW phase shifter, Figure 5 provides the variations of the simulated bandwidth for the 15-dB DM impedance matching with different w_s , d_s , l_s , and l_f . Figure 6 shows the variations of the simulated bandwidth for the DM phase shift with $\pm 5\%$ phase deviation for different Δd_s ($d_{sr} - d_{sm}$), Δw_s ($w_{sr} - w_{sm}$), and Δl_s ($l_{sr} - l_{sm}$), where the subscripts *r* and *m* of d_{sr} , d_{sm} , w_{sr} , w_{sm} , l_{sr} , and l_{sm} indicate the reference and main lines, respectively.

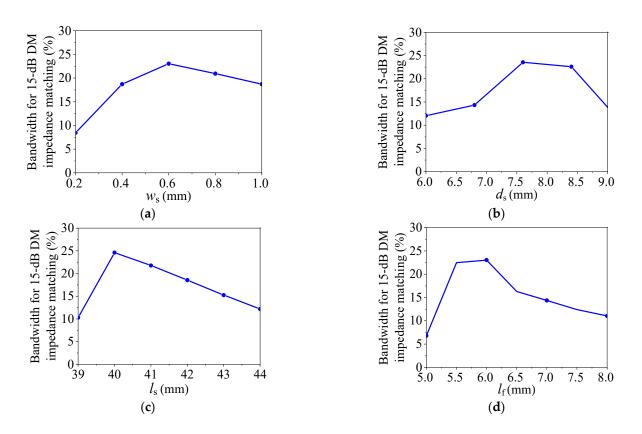


Figure 5. The simulated bandwidth for 15-dB DM impedance matching of the proposed balanced SIW phase shifter with different w_s , d_s , l_s , and l_f . (a) With different w_s . (b) With different d_s . (c) With different l_s . (d) With different l_f .

It can be observed from Figure 5 that the bandwidth for 15-dB DM impedance matching increases first and then decreases when increasing w_s , d_s , l_s , or l_f . Therefore, the wideband DM impedance matching can be achieved by selecting the proper parameters of w_s , d_s , l_s , or l_f . Figure 6a,c show that the bandwidth of DM phase shift with $\pm 5\%$ phase deviation increases at first and then decreases as increasing Δw_s or Δl_s . Figure 6b demonstrates that Δd_s has a negligible effect on the bandwidth of the DM phase shift with $\pm 5\%$ phase deviation. Thus, the wideband DM phase shift with $\pm 5\%$ phase deviation can be obtained by selecting the parameters of Δw_s or Δl_s appropriately.

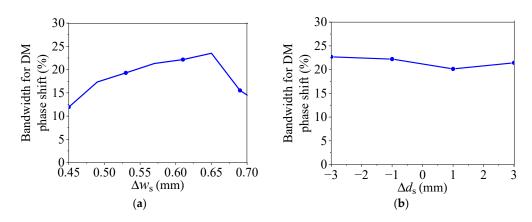


Figure 6. Cont.

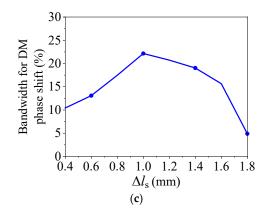


Figure 6. The simulated bandwidth for DM phase shift with $\pm 5\%$ phase deviation of the proposed balanced SIW phase shifter with different Δd_s , Δw_s , and Δl_s . (a) With different Δd_s . (b) With different Δw_s . (c) With different Δl_s .

2.3. CM Analysis

Similarly, Figures 7 and 8 depict the uniform amplitude and vector distributions of the surface current on the SIW with/without slots for CM operating at f_0 . It can be observed from Figure 7 that a small portion of the surface current on the SIW without slots can be transmitted, while the remainder will be substantially suppressed. Figure 8 demonstrates that on an SIW with two slots, almost no surface current can be transmitted, indicating the current is effectively prevented by the slots. Therefore, the CM suppression will be further enhanced by the slots.

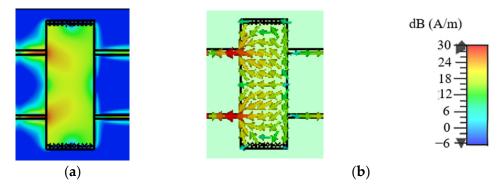


Figure 7. The surface current distributions on the SIW without slots for CM operating at f_0 . (a) The uniform amplitude distributions. (b) The vector distributions.

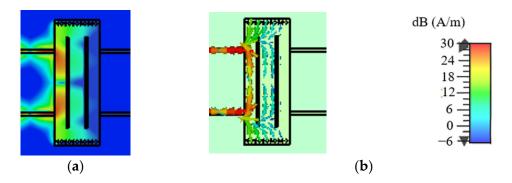


Figure 8. The surface current distributions on the SIW with two slots for CM operating at f_0 . (a) The uniform amplitude distributions. (b) The vector distributions.

Moreover, according to Equation (2), the frequency space between TE_{10} and TE_{30} modes would be wider than the DM operating frequency range if f_0 were fixed. Therefore, it is possible to achieve CM suppression with a bandwidth that completely encompasses the DM operating bandwidth.

Figure 9 displays the simulated bandwidth for 15-dB CM suppression with varying w_s , d_s , l_s , and l_f to illustrate how the slot parameters influence the CM suppression of the proposed balanced SIW phase shifter. It can be observed from Figure 9a,d that the bandwidth for CM suppression increases slightly with increasing w_s or l_f . Figure 9b shows that the bandwidth for CM suppression is nearly unchanged with varying d_s , and Figure 9c illustrates that the bandwidth for CM suppression is primarily determined by the equivalent width of the SIW and the slot lengths.

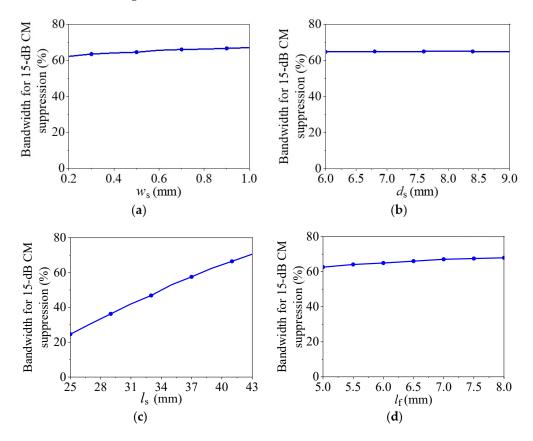


Figure 9. The simulated bandwidth for 15-dB CM suppression of the proposed balanced SIW phase shifter with different w_s , d_s , l_s , and l_f . (a) With different w_s . (b) With different d_s . (c) With different l_s . (d) With different l_f .

According to Figures 5, 6 and 9, the bandwidth for CM suppression is usually wider than that for DM impedance matching and DM phase shift. Therefore, the operating bandwidth will be determined by the bandwidths for DM impedance matching and DM phase shift. In addition, we can find that d_s and l_f have obvious effects on the bandwidth for DM impedance matching but not on the bandwidths for DM phase shift and CM suppression. Therefore, the bandwidth for DM impedance matching can be controlled by d_s and l_f . Furthermore, Δw_s and Δl_s have large effects on the bandwidth for DM phase shift. Thus, the bandwidth for DM phase shift can be primarily controlled by Δw_s and Δl_s .

2.4. Design Procedure

The design procedure for the proposed balanced SIW phase shifter can be described as follows:

- (1) Determine *a* according to the relationship of a, f_0 , and w_{eff} in Equations (1)–(3) to make the proposed design achieve the DM impedance matching and CM suppression at f_0 simultaneously.
- (2) Determine the initial values of w_s , d_s , l_s , and l_f for the reference line according to the variation rules of the bandwidths for 15-dB DM impedance matching and 15-dB CM suppression in Figures 5 and 9, respectively.
- (3) Determine the initial values of l_d for different main lines according to the required phase shifts, and determine the initial values of w_s , d_s , l_s , and l_f for different main lines according to the variation rules of the bandwidths for 15-dB DM impedance matching, DM phase shift, and 15-dB CM suppression in Figures 5, 6 and 9, respectively.
- (4) Fine-tune the parameters in computer simulation technology (CST) to optimize the performance.

3. Results

Five prototypes of one reference line and four main lines are designed and fabricated at $f_0 = 3.5$ GHz. According to the design procedure, the final dimensions are listed in Table 1. A four-port Agilent N5230C vector network analyser is used to test the proposed balanced SIW phase shifter.

Table 1. Dimensions of the	proposed balanced SIW	phase shifter (Unit: mm).
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	Reference Line	45° Main Line	90 $^{\circ}$ Main Line	135° Main Line	180° Main Line
а	59.1	59.1	59.1	59.1	59.1
$l_{\rm f}$	8.16	8.15	8.14	7.8	7.51
S	1.8	1.8	1.8	1.8	1.8
d	1.3	1.3	1.3	1.3	1.3
8	1.65	1.65	1.65	1.65	1.65
\tilde{d}_s	8.36	8.2	8.2	7.8	7.56
w_s	0.5	0.55	0.56	1	1.35
l_s	41.6	41	40.4	38.9	38
l_d	8	11.6	15.31	19.04	22.67
w_p	1.83	1.83	1.83	1.83	1.83

The photograph and results of the five prototypes are shown in Figures 10 and 11, respectively. For the proposed balanced SIW phase shifter, DM and CM *S*-parameters can be expressed as S_{ij}^{dd} and S_{ij}^{cc} , respectively, where *i* and *j* are the port number, and *d* and *c* denote DM and CM, respectively.

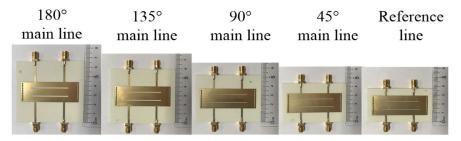
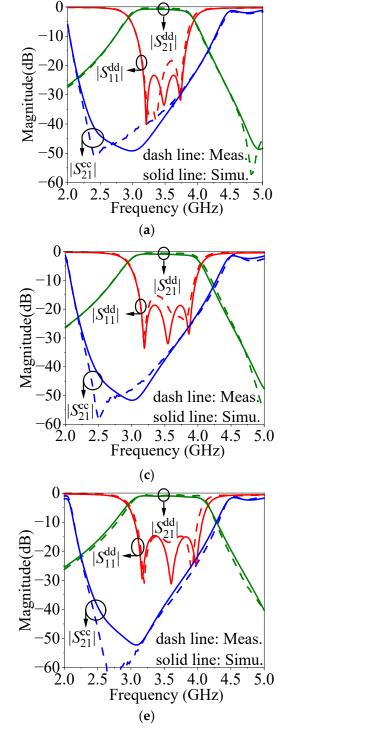


Figure 10. The photograph of the proposed balanced SIW phase shifter.

It can be seen from Figure 11a–e that the reference line and main lines of 45° , 90° , 135° , and 180° phase shifters have the measured bandwidths for 15-dB DM return loss of 3.12 GHz to 3.82 GHz (20%), 3.12 GHz to 3.82 GHz (20%), 3.11 GHz to 3.91 GHz (22.9%), 3.12 GHz to 3.94 GHz (23.4%), and 3.12 GHz to 3.96 GHz (24%), with the bandwidth for 15-dB CM suppression of 2.07 GHz to 4.17 GHz (60%), 2.09 GHz to 4.16 GHz (59.1%), 2.12 GHz to 4.18 GHz (58.9%), 2.16 GHz to 4.22 GHz (58.9%), and 2.18 GHz to 4.22 GHz (58.3%), with the circuit size of λ_g^2 , $1.2\lambda_g^2$, $1.4\lambda_g^2$, $1.6\lambda_g^2$, and $1.8\lambda_g^2$, with the minimum insertion losses of 0.38 dB, 0.41 dB, 0.5 dB, 0.58 dB, and 0.59 dB, respectively. It can be observed from Figure 11f that the bandwidths for the phase shifts of $45^{\circ} \pm 2^{\circ}$, $90^{\circ} \pm 4.5^{\circ}$,

 $135^{\circ} \pm 6^{\circ}$, and $180^{\circ} \pm 8^{\circ}$ are 2.95 GHz to 4.07 GHz (32%), 2.9 GHz to 4.02 GHz (32%), 3.12 GHz to 3.88 GHz (21.7%), and 3.1 GHz to 3.85 GHz (21.4%), respectively. Therefore, the operating bandwidths for 45°, 90°, 135°, and 180° phase shifters are 20%, 20%, 20%, and 20%, respectively, which cover the 15-dB DM return loss, 15-dB CM suppression, and \pm 5% phase deviation simultaneously.



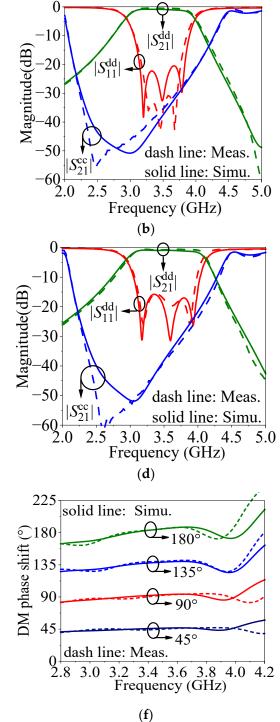


Figure 11. The simulated (Simu.) and measured (Meas.) results of the five prototypes. (a) *S*-parameters for the reference line. (b) *S*-parameters for the main line of 45° phase shifter. (c) *S*-parameters for the main line of 90° phase shifter. (d) *S*-parameters for the main line of 135° phase shifter. (e) *S*-parameters for the main line of 180° phase shifter. (f) DM phase shift.

Table 2 lists the demonstrated performances of the proposed design and other reported microstrip and SIW phase shifters. Compared to previously reported microstrip balanced phase shifters ([6,7,9]), the proposed SIW design has narrower bandwidth, but it would be more suitable for millimetre wave application. Compared to previously reported SIW phase shifters ([13–16,18,20,22]), the proposed design features a balanced topology with wideband CM suppression. In addition, compared to single-ended designs with equal lengths of the reference line and main lines from [13,15], the proposed design has a wider operating bandwidth. Compared to the wideband designs from [14,16], and the low insertion loss designs from [18,22], the size of the proposed design is more compact. Compared to the compact size design from [20], the proposed design has a larger phase shift range.

	f ₀ (GHz)	Phase Shift	FBW (%)	RL _{min} (dB)	IL _{max} (dB)	Size (λ_g^2)	15-dB CMS FBW (%)	n	Туре
[6]	3.5	$45^{\circ} \pm 2.3^{\circ} \ 90^{\circ} \pm 4.7^{\circ}$	81 82	15	0.64 0.78	0.27 0.35	86	1	Microstrip, Balanced
[7]	3	$180^\circ\pm 4.2^\circ$	73.8	14.87	0.96	0.8	75.2	1	Microstrip, Balanced
[9]	4	$\begin{array}{c} 30.14^{\circ}\pm2.2^{\circ}\\ 90.75^{\circ}\pm4.1^{\circ}\\ 180.1^{\circ}\pm5.5^{\circ} \end{array}$	73 68.5 66.8	16 15 15	0.76 0.9 0.9	0.86 0.93 1.19	93.8 92.5 76	1	Microstrip, Balanced
[13]	24	$egin{array}{c} 15^\circ \pm 5^\circ \ 30^\circ \pm 5^\circ \ 60^\circ \pm 5^\circ \end{array}$	10	10	1.5	4.51	N/A	1	SIW, Single-end
[14]	32	$45^{\circ} \pm 3.5^{\circ} \\ 90^{\circ} \pm 2.5^{\circ}$	49 49	10.8 13	0.5 0.75	2.78 4.66	N/A	1	SIW, Single-end
[15]	10	11.25° 45°	9.6 6.9	10 10	0.88 2.32	0.73 0.73	N/A	1	SIW, Single-end
[16]	6	$45^{\circ} \pm 2.5^{\circ} \\ 90^{\circ} \pm 3^{\circ}$	60 55	10	2.5	2.77 2.86	N/A	3	SIW, Single-end
[18]	33 34.4	$\begin{array}{c} 43^\circ\pm6^\circ\\ 90^\circ\pm5^\circ\end{array}$	42.4 12	12.5 10	0.52 0.52	5.43 15.2	N/A	3	SIW, Single-end
[20]	4.5	$90^\circ\pm 3.5^\circ$	43	12	1.6	0.44	N/A	1	SIW, Single-end
[22]	41	$90^\circ\pm 6^\circ$	39	25	0.2	3	N/A	1	SIW, Single-end
This work	3.5	$\begin{array}{c} 45^{\circ}\pm2^{\circ}\\ 90^{\circ}\pm4.5^{\circ}\\ 135^{\circ}\pm6^{\circ}\\ 180^{\circ}\pm8^{\circ} \end{array}$	20 20 20 20 20	15	0.8 0.82 0.93 1	1.2 1.4 1.6 1.8	59 59 58 57	1	SIW, Single-end

Table 2. Performances comparison with previous works.

FBW: Fractional operating bandwidth; RL: Return loss; IL: Insertion loss; CMS: CM suppression; n: Number of layers.

4. Conclusions

In this paper, a balanced phase shifter utilizing SIW with two slots is proposed, which has the features of wideband CM suppression, broad phase shift range, and an easily fabricated structure. DM and CM analysis, performance variation, and design procedure are performed to guide the practical design. The measurements of the final 45°, 90°, 135°, and 180° prototypes agree well with the theoretical prediction. The proposed balanced SIW phase shifter is believed to be capable of promoting the development of balanced microwave systems.

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Data Availability Statement: The data presented in this study are available on request from the corresponding author.

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