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Multi-Phase Interleaved AC–DC Step-Down Converter with Power Factor Improvement

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Abstract: This paper presents the converter design of a single-phase non-isolated step-down controlled rectifier for power factor improvement and output voltage regulation. The converter consists of a full-bridge diode rectifier and a DC–DC interleaved buck converter of two or more switching cells that has an LC filter in its input. It is proposed that the interleaved switching cells operate in discontinuous conduction mode and the current through the input LC filter be continuous, avoiding switching frequency components to be injected into the grid. The controller, which has a simple structure and a small number of sensors, allows the system to achieve a high power factor. It also regulates the output voltage to a constant reference. An experimental prototype is built and tested to validate the analysis and proposed design. The closed-loop converter is evaluated both in a steady state and in transient conditions. At steady state, the converter achieves a power factor above 0.9 with a maximum of 45.4% THD at 110.1 W. The main contributions of this paper are guidelines for the design of the converter, open-loop analysis, and converter control.

Keywords: PFC; rectifier; interleaved buck converter; AC–DC; LC filter

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1. Introduction

Power Factor Correction (PFC) rectifiers are essential in the AC–DC conversion required to supply power to different loads. They are preferred in industrial applications for reducing the harmonic distortion of the AC current and achieving a power factor (PF) close to unity which maximizes the active power transferred from the AC grid [1]. PFC rectifiers must have sinusoidal waveform AC current, regulated DC output current or regulated DC output voltage, simple control and modulation schemes, and high efficiency [2]. They can be composed of two stages, where the first stage is responsible for the PFC, and the second is for voltage or current regulation. Single-stage PFC rectifiers can reduce the number of components and increase efficiency.

PFC rectifiers can be galvanically isolated or not, and can operate in Continuous Conduction Mode (CCM) or in Discontinuous Conduction Mode (DCM) [3], and are required in different applications and in a wide power range. For example, in domestic applications, there is a need for motor drivers that are used in ventilation, air conditioning, and dryer applications [4]. In lighting applications, they are required in LED lighting [5–7] and in high-pressure sodium lamps [8]. In particular, LED drivers require unidirectional rectifiers that achieve near unity PF, low switching ripple [9], and long lifetime [10]. Other applications are in drivers for induction motors or permanent magnet motors for elevators that normally use a rectifier system followed by a DC–AC conversion stage [11,12]. PFC rectifiers have applications in charging low-capacity lithium-ion batteries, such as those used in electronic devices, including mobile phones, which require high power density designs but are also needed for charging electric vehicle (EV) battery banks. Those converters used as on-board or off-board EV chargers can be unidirectional or bidirectional [13–16].

A review of single-phase unidirectional non-isolated PFC converters for onboard battery chargers can be found in [16]. Other applications are in uninterruptible power supplies for data centers [17], and wireless power transfer systems [18].

The boost converter-based PFC rectifier has been widely adopted due to its simplicity and high efficiency [19–23]. The converter DC output voltage in such systems is typically higher than the peak of the AC supply voltage, and for step-down applications, a second stage is required to regulate to a lower voltage level [21] which may degrade the efficiency of the system. PFC rectifiers based on conventional converters such as buck-boost [24], SEPIC [21,25], Cuk [12,25,26], flyback [27], Luo [28], and Zeta [29] converters can improve PF as well as have step-down conversion capability. Very few works have focused on the conventional buck converter since, without modification, it has a discontinuous AC input current and, consequently, high harmonic distortion [30]. However, step-down PFC rectifiers are increasingly being used to achieve a wider control range for the output voltage and to reduce the step-down requirement in the DC–DC conversion stage, for example, in EV charging systems [31]. Their use results in DC–DC converters being built with low-voltage switches, leading to higher efficiency [15]. Step-down PFC rectifier systems are expected to provide an option for supplying DC distribution grids or also for charging EV batteries [2].

In [32], a PFC AC–DC system is presented for applications of less than 100 W. The system uses a full-bridge diode rectifier, a charge pump circuit, and a class-DE resonant circuit. The class-DE topology is similar to the class-D topology but with switching conditions like the class-E circuit [33]. However, the topology in [32] suffers from increased electrical stress as a result of the addition of the charge pump circuit, which results in additional losses in the resonant tank. In [4], the control of a switched reluctance motor with a converter consisting of two Cuk converters with a common switch, in DCM and with AC supply voltage is presented. The converter includes PFC and operates in DCM, which reduces its size and cost. However, a controller is required to keep the voltage across the two capacitors of the dual converter balanced. In [26], a converter based on the switched inductor Cuk converter in CCM is presented for battery charging applications with a nominal power of 500 W. The topology has a high step-down gain and a relatively small number of components. However, the topology has relatively large inductors due to CCM operation and complex control. In [5], a driver for LEDs is proposed that consists of a first stage of a PFC rectifier and a second stage based on a bidirectional buck-boost converter. The bidirectional buck-boost converter is connected in parallel with the output of the PFC converter and serves to absorb the second harmonic component of the output current. However, control of the parallel converter can be complex, and generally, the topology has a relatively large inductor leading to large core and winding losses. In addition, the passive and active components of the parallel converter may suffer from high voltage stress. In [34], a non-linear control for a two-switch buck-boost PFC rectifier is proposed, with an active power decoupling function that can avoid the use of large electrolytic capacitors. Elements in the added circuit suffer from high voltage stress, and the converter controller is complex. A PFC rectifier without electrolytic capacitors based on the flying capacitor buck-boost converter is presented in [35]. The topology incorporates additional components, and due to the converter's nonlinear dynamics, control design is difficult. In addition, the output voltage must be greater than half of the peak AC voltage.

This paper presents the design of a single-phase step-down PFC rectifier together with its control. The converter consists of a full-bridge diode rectifier and a DC–DC interleaved buck converter of two or more switching cells that has an LC filter at its input. The proposed control is conventional and is based on a two-loop average control that assumes decoupled voltage and current dynamics. However, in this case, the decoupling occurs naturally due to the design by proposing that the LC input filter has a continuous current in the inductor and a continuous voltage across the capacitor and that the interleaved switching cells operate in DCM. With these assumptions, the control can be configured with a simple structure with only the feedback of three variables from the converter, namely

the AC grid current, the voltage across the DC output capacitor, and the grid AC voltage. In DCM operation, switching frequency harmonic components can be conducted, and active switches can withstand high voltage spikes. However, the noise conducted into the electrical grid is mitigated by the input LC filter avoiding large switching frequency components being injected into the AC grid. Additionally, the interleaved switching cells allow current and voltage ratings to be shared between each switching cell and then reduce element sizes. The main contributions of this paper are the guidelines for the design of the converter, open-loop analysis and modeling, and the proposal of the converter control.

2. Multi-Phase Interleaved AC–DC Step-Down Converter Description

The electric simplified circuit of the converter is shown in Figure 1 and consists of a full-bridge diode rectifier, and a DC–DC interleaved buck converter, which has an LC filter at its input, formed by the inductor L_i and capacitor C_i, which is connected to a buck converter of n interleaved switching cells, with $n \geq 2$. It is proposed that the interleaved switching cells operate in DCM and also that the current through the input filter be continuous, avoiding large switching frequency components being injected into the AC grid.

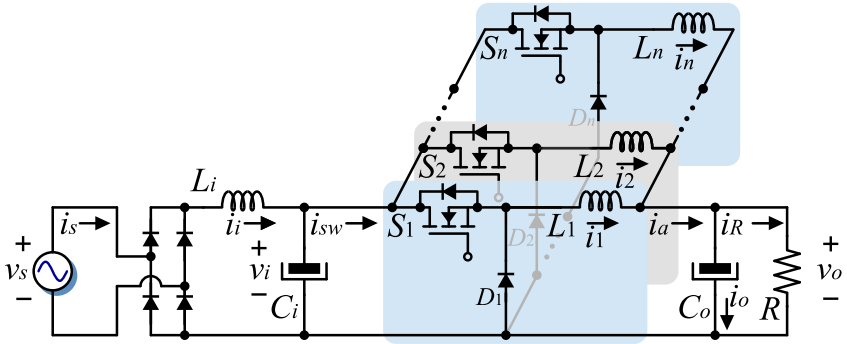

Figure 1. Diagram of the converter topology.

The buck converter has n active switches $S_1, \ldots, S_n$, n diodes $D_1, \ldots, D_n$, an output DC capacitor C_o, and n inductors $L_1, \ldots, L_n$ for the interleaved switching cells. The load is represented by the resistive element R, and the AC electrical grid is represented by a voltage source. The converter operation in steady state is set such that the currents through the inductors $L_1, \ldots, L_n$ are in DCM, and the current through L_i, i_i, and the voltage across C_i, v_i, are in CCM. The switches S_l, with $l = 1, \ldots, n$, are switched at a frequency $f = 1/T$ where T is the switching period in seconds. The activation and deactivation pattern of each S_l, $l = 1, \ldots, n$ is equal but is displaced T/n s, consecutively and cumulatively. Let $k := t_{\text{on}}/T$ denote the duty cycle where t_{on} is the time when the active switches remain in conduction. Compared to the converter with only one single switching cell in DCM, the incorporation of n interleaved switching cells $\{S_l, L_l, D_l\}$, with $l = 1, \ldots, n > 1$, reduces the electrical stress on the switching devices, leading to the use of smaller size elements as well as reducing current ripple in the load. The input filter performs a low-pass filter function that mitigates the switching harmonic components injected into the AC grid. This input filter can be designed to ensure a continuous grid current and continuous capacitor voltage v_i, both with reduced ripple. Under this condition, and in steady state, v_i can be assumed constant except for the voltage ripple, and therefore the input filter dynamics can be supposed to be decoupled from the output DC dynamics with the objective to simplify the output voltage regulation control design.

3. Converter Steady-State Analysis

In this section, the analysis of the open-loop steady-state operation of the converter is presented. The assumptions considered in the analysis are the following.

1. All elements, passive and active, are ideal. In particular, parasitic series resistances of inductors are not considered.

2. Inductors $L_1 = \cdots = L_n = L_o$ are equal.
3. Duty cycles and phase-shift angles are equal for each interleaved switching cell $\{S_l, L_l, D_l\}$, $l = 1, \ldots, n$.

The analysis of the converter with a DC voltage source in the next subsection establishes design guidelines so that the current in each of the interleaved inductors is discontinuous and input current i_i and voltage v_i are continuous. Therefore, this analysis yields rules for the selection of:

1. The inductor value L_o to assure DCM in terms of load and switching frequency,
2. the values of L_i and C_i to assure a constant positive current i_i and constant positive voltage v_i with small ripple, and,
3. the output capacitor value C_o to assure a given output voltage ripple in terms of the load.

In the analysis of the converter connected to an AC voltage source through a full-bridge diode rectifier is supposed that conditions of the operation previously described are preserved.

3.1. Steady-State Analysis with a DC Input Voltage Source

The full-bridge diode rectifier and the AC voltage source in Figure 1 are replaced by a constant DC voltage source with value V_{DC}, as shown in the circuit of Figure 2.

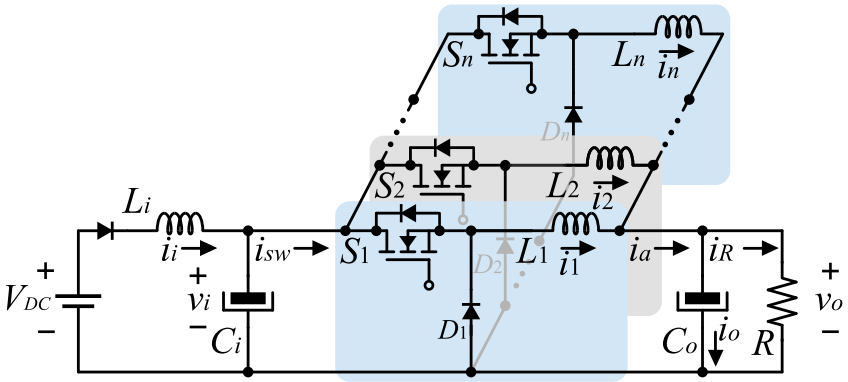

Figure 2. Converter topology with a constant DC power supply.

The notation of the variables is as follows. Let i_l with $l = 1, \ldots, n$ be the instantaneous current through the inductor L_l, let i_R be the instantaneous current through the load, and let v_i and v_o denote the instantaneous voltages through the capacitors C_i and C_o, respectively.

In Figure 3, the waveforms of the converter with $n = 4$ interleaved cells are depicted for three different duty cycles. The general case for n interleaved switching cells is analogous. In Figure 3a, $k = 0.15$, in Figure 3b, $k = 0.4$, and in Figure 3c, $k = 0.7$. The upper plots depict the currents i_l, $l = 1, \ldots, n$ of the interleaved inductors, the middle plot depicts the sum of the switch currents i_{sw} and the sum of inductor currents $i_a = i_1 + \cdots + i_n$. The plot at the bottom depicts the voltage of capacitors v_i and v_o. With duty cycles less than $1/n$, the currents i_l, $l = 1, \ldots, n$ do not overlap and are zero before any other rises.

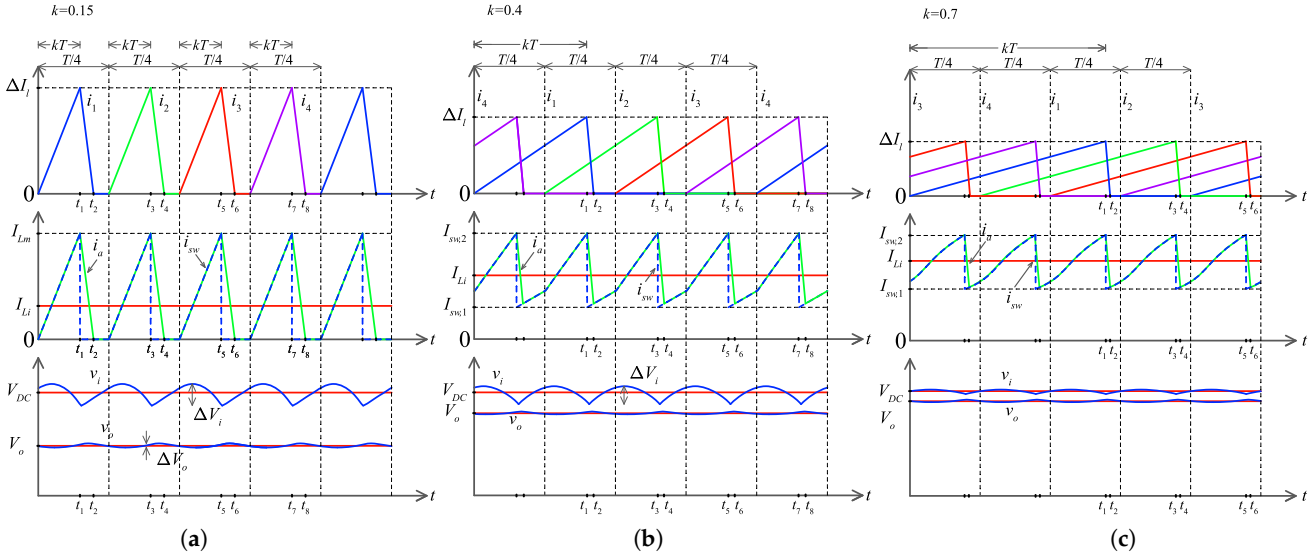

Figure 3. Converter steady-state waveforms under different duty cycles k, (**a**) 0.15, (**b**) 0.4, (**c**) 0.7.

3.1.1. Selection of L_o

By assuming that v_i is positive and continuous, then its averaged value is $V_i = V_{DC}$ in the steady state. Therefore, the converter can be simplified as an interleaved buck of n switching cells connected to a constant voltage source. From the circuit $i_a = \sum_{l=1}^{n} i_l = i_o + i_R$ and then $I_a = I_R = V_o/R$, where uppercase denotes DC component. Therefore $I_l = V_o/(nR)$, and the current peak of interleaved inductors is given by

$$\Delta I_l = \frac{(V_{DC} - V_o)k}{L_l f},\ l = 1, \ldots, n. \tag{1}$$

Then the critical inductor for DCM is given by $2I_l = \Delta I_l$, and the critical inductor for the interleaved inductors to achieve DCM is given by the following expression

$$L_{o,c} = \frac{(V_{DC} - V_o)knR}{2fV_o} = \frac{(1-k)nR}{2f}. \tag{2}$$

Then, the inductor $L_l < L_{o,c}$ to assure DCM of the switching cells, which implies that the current i_l, $l = 1, \ldots, n$ is zero from a given time on during a switching period. Additionally, the static output voltage is given by,

$$V_o = \frac{2V_{DC}}{1 + \sqrt{1 + \frac{8L_e f}{Rk^2}}} = \frac{2V_{DC}}{1 + \sqrt{1 + \frac{8L_o f}{nRk^2}}}, \tag{3}$$

where the equivalent inductor $L_e = L_o/n$ is given by the parallel connection of $L_1, \ldots, L_n$.

3.1.2. Selection of L_i and C_i

The passive elements L_i and C_i are selected to assure a constant positive current i_i and constant positive voltage v_i with a small ripple. The objective of this input filter is to reduce the switching frequency harmonics in i_i. Its cutoff frequency is selected relatively low, and the current i_{sw} can be treated as an input that excites, in steady state, the current i_i as depicted in Figure 4. The largest amplitude component of i_i has the natural frequency of the input filter $1/\sqrt{L_i C_i}$ rad/s. This frequency has to be selected large enough to avoid resonance problems with grid frequency harmonics, but less than the switching frequency to filter effectively.

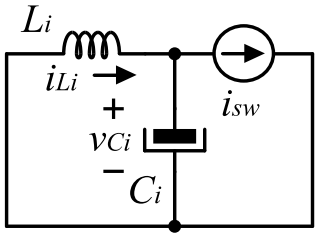

Figure 4. Simplification of the input filter circuit.

The analysis proceeds by obtaining the steady-state expression of i_i excited by i_{sw}, by discarding the DC component. In the steady state, and for duty-cycle $k < 1/n$ the current i_{sw} has the larger ripple amplitude, is periodic with period T/n, and can be described by

$$i_{sw}(t) = \begin{cases} \frac{I_m t}{kT}, & 0 < t \leq kT, \\ 0, & kT < t \leq T/n, \end{cases} \tag{4}$$

where I_m is the peak amplitude of any of the inductor currents i_l, $l = 1, \ldots, n$, and can be obtained by (1). Hence, the average is given by $I_{sw} = nkI_m/2$, and the zero average form of i_{sw}, $i_{sw,ac}$ is

$$i_{sw,ac}(t) = \begin{cases} \frac{I_m t}{kT} - \frac{nkI_m}{2}, & 0 \leq t \leq kT, \\ -\frac{nkI_m}{2}, & kT \leq t \leq T/n. \end{cases} \tag{5}$$

For analysis, current $i_{sw,ac}$ can be approximated by a sinusoidal of period T/n, with the same RMS value than $i_{sw,ac}(t)$

$$i_{sw,ac,\mathrm{RMS}} = \frac{I_m}{6}\sqrt{3nk(4-3kn)}. \tag{6}$$

Then

$$i_{sw,ac}(t) \approx i_{\sin}(t) = \frac{I_m}{6}\sqrt{6nk(4-3kn)}\ \sin(2\pi nt/T). \tag{7}$$

The equations of the circuit in the Figure 4 are given by

$$L_i\, di_i/dt = -v_i, \tag{8}$$

$$C_i\, dv_i/dt = i_i - i_{\sin}(t). \tag{9}$$

The solution is periodic and has two frequency components, one at n times the switching frequency and the other at the resonance frequency of the input filter $1/\sqrt{L_iC_i}$. The latter has the larger amplitude, and by ignoring the switching frequency component, a solution is given by

$$i_i(t) \approx \frac{n\pi T I_m\sqrt{6nkL_iC_i(4-3nk)}}{3(4n^2\pi^2L_iC_i - T^2)}\sin\left(t/\sqrt{L_iC_i}\right), \tag{10}$$

$$v_i(t) \approx \frac{-n\pi L_i T I_m\sqrt{6nk(4-3nk)}}{3(4\pi^2L_iC_in^2 - T^2)}\cos\left(t/\sqrt{L_iC_i}\right). \tag{11}$$

Therefore an approximation for the current ripple can be given by

$$\Delta I_i \approx \frac{2n\pi T I_m\sqrt{6nkL_iC_i(4-3nk)}}{3(4n^2\pi^2L_iC_i - T^2)} \tag{12}$$

$$\Delta V_i \approx \frac{2n\pi L_i T I_m\sqrt{6nk(4-3nk)}}{3(4\pi^2L_iC_in^2 - T^2)} \tag{13}$$

The averaged values of the inductor current and capacitor voltage are given by $I_i = knI_m/2$ and $V_i = V_{DC}$, then the selection of passive elements, for assuring continuous current and voltage, must follow

$$\Delta I_i < 2I_i = knI_m, \qquad \Delta V_i < 2V_i = 2V_{DC}. \tag{14}$$

However, in practice, and to reinforce the decoupling between input and output dynamics, ΔV_i must be selected small. By design, current i_i and voltage v_i in steady-state are continuous, and their ripples have a fundamental frequency of $1/\sqrt{L_I C_I}$, which is much less than the switching frequency. The input filter's natural frequency must be larger than any of the expected harmonic components in the AC voltage source.

3.1.3. Selection of C_o

The output capacitor C_o must filter the sum of currents of the interleaved inductors i_a to obtain a continuous voltage in the load. In the worst case scenario, for $kT \leq T/n$, i_a is discontinuous and C_o can be computed by requiring a given ΔV_o per [36],

$$C_o = \frac{T(nk + d_2)(I_m - I_o)^2}{2nI_m \Delta V_o}, \tag{15}$$

and where d_2 is the fraction of T/n where the i_l drops to zero whenever $k \leq T/n$ and is given by,

$$d_2 = \frac{-nk + \sqrt{n^2k^2 + \frac{8nL_o}{RT}}}{2}. \tag{16}$$

4. Controller Design for the Converter with a Full-Bridge Rectified Sinusoidal Power Supply

In this subsection, the controller design and arguments for the performance of the closed-loop system are presented. The converter of the previous subsection is considered, but by replacing the DC voltage source with a full-bridge diode rectified AC voltage source.The following assumptions are made.

1. The AC grid is considered without harmonic distortion and is represented by $v_s(t) = V_m \sin(\omega_s t)$, where V_m is the peak voltage in Volts (V) and ω_s is the constant grid angular frequency in rad/s.
2. Switching frequency $2\pi f_{sw}$ is much higher than the grid angular frequency ω_s so that the input voltage can be considered constant during one switching period.
3. Inductor currents i_l, $l = 1, \ldots, n$ are discontinuous in the steady state.

A complete standard state equation model is essentially nonlinear and is difficult to obtain due to the DCM nature of the output cells, in addition to the rectification stage. Although the converter has multiple switching cells that operate in DCM, its dynamics can be approximated by a model that describes the variables averaged in a switching frequency period. To simplify, the interleaved buck is replaced by an equivalent single-cell buck converter in DCM that has the equivalent inductor L_o/n. Moreover, to avoid considering the derivative of the rectified voltage, $|v_s(t)|$, which is not well defined in the zero-crossings of v_s, the grid current i_s dynamics is considered instead of the dynamics of i_i. Therefore, a state-space model that can approximate the converter dynamics is given as:

$$L_i \dot{x}_1 = -x_2 + v_s(t), \tag{17}$$

$$C_i \dot{x}_2 = x_1 - u_s x_3, \tag{18}$$

$$(L_o/n)\, \dot{x}_3 = -dx_4 + u(x_2 - x_4), \tag{19}$$

$$C_o \dot{x}_4 = dx_3 - \frac{1}{R} x_4 + u x_3. \tag{20}$$

The variable x_1 denotes the grid current i_s, and therefore $|x_1|$ represents the averaged current i_i. Likewise, $|x_2|$ represents the averaged capacitor voltage v_i, and x_3 and x_4 are averaged variables in a switching frequency period T that are related to i_a and v_o, respectively. The variable $u \in (0,1)$ is the duty-cycle and is considered the control input, and $u = |u_s|$. On the other side, d denotes the fraction of T that takes the current of the equivalent inductor L_o/n to drop to zero in the DCM buck converter. In this analysis, it is considered that d is an unknown constant, but satisfying $d < u$. In general, d depends on R, u, v_s and L_o. Equations (17)–(20) are non-linear and may describe the averaged behavior of the converter. The control objectives are the following

1. Current tracking: $i_s \to Gv_s(t)$, as $t \to \infty$, where G is a positive constant.
2. Voltage regulation: $v_o \to V_{ref}$ as $t \to \infty$, where V_{ref} is a positive constant.

The proposed control is conventional and is based on a two-loop averaged control that assumes decoupled voltage and current dynamics. By following the design of the previous section, the input dynamics are assumed much faster than the output dynamics, and therefore, input and output dynamics can be considered decoupled. Therefore, the control objectives of output voltage regulation to constant references and AC input current tracking can be designed independently, and the control can be configured with a simple structure and a reduced number of sensors, namely the grid current, the grid voltage, and the voltage across the DC output capacitor. The inner current control loop forces the grid current to follow as closely as possible a sinusoidal reference that is proportional to the fundamental component of the input AC voltage. The outer voltage control loop regulates the average output voltage.

4.1. Current Tracking Control Loop

The control proposal proceeds by defining the current tracking loop. Since the current tracking objective imposes i_s to be proportional to v_s then it is proposed that $u_s = k_c(i_s^* - i_s) = k_c(gV_m \sin(\omega_s t) - x_1)$ where g is to be defined in the voltage regulation loop. Then the input filter dynamics become

$$\begin{aligned} L_i \dot{x}_1 &= -x_2 + V_m \sin(\omega_s t), \\ C_i \dot{x}_2 &= x_1 - k_c(gV_m \sin(\omega_s t) - x_1)x_3. \end{aligned}$$

Per the nature of the converter, x_3 is always positive, and by assuming it is constant, we can obtain the steady-state response by,

$$x_1^* = \left(\frac{K_c}{1+K_c}\right) gV_m \sin(\omega_s t) \tag{21}$$

$$x_2^* = V_m \sin(\omega_s t), \tag{22}$$

where $K_c = k_c x_3$. It can be observed that $x_1^*(t) \approx gV_m \sin(\omega_s t)$ whenever $K_c \gg 1$. The error dynamics, with error state variables $z_1 = x_1 - x_1^*$ and $z_2 = x_2 - x_2^*$ is given by

$$\begin{aligned} L_i \dot{z}_1 &= -z_2 - \left(\frac{K_c}{1+K_c}\right) gL_i V_m \cos(\omega_s t) \\ C_i \dot{z}_2 &= (1+K_c)z_1 - C_i \omega_s V_m \cos(\omega_s t). \end{aligned}$$

The latter is a forced harmonic oscillator whose solutions have a transient with natural frequency oscillation and, in steady state, have the response given by (21) and (22).

4.2. Output Voltage Regulation Control Loop

Given that i_l, $l = 1, \ldots, n$ are discontinuous at the switching frequency, therefore the voltage $v_i = V_{in}$ can be assumed constant. The output dynamics are given by

$$(L_o/n)\,\dot{x}_3 = -dx_4 + g(V_{in} - x_4) \tag{23}$$

$$C_o\dot{x}_4 = dx_3 - \frac{1}{R}x_4 + gx_3 \tag{24}$$

and therefore, to achieve output voltage regulation, a PI controller is proposed

$$g = k_p\left(V_{ref} - v_o\right) + k_i\eta \tag{25}$$

$$\dot{\eta} = V_{ref} - v_o, \tag{26}$$

where V_{ref} is the constant reference for the output voltage. Therefore the equilibrium point for the output dynamics in a closed loop is given by

$$x_3^* = \frac{V_{ref}\left(V_{in} - V_{ref}\right)}{V_{in}dR}, \quad x_4^* = V_{ref}, \quad \eta^* = \frac{dV_{ref}}{k_i\left(V_{in} - V_{ref}\right)}, \tag{27}$$

where V_{in} is the voltage v_i assumed constant with a low ripple. By defining error variables $z_3 := x_3 - x_3^*$, $z_4 := x_4 - x_4^*$ and $z_5 := \eta - \eta^*$, and considering the linearized system we obtain,

$$(L_o/n)\dot{z}_3 = -\left(k_p(V_{in} - V_{ref}) + \left(\frac{dV_{in}}{V_{in} - V_{ref}}\right)\right)z_4 + k_i\left(V_{in} - V_{ref}\right)z_5, \tag{28}$$

$$C_o\dot{z}_4 = \left(\frac{dV_{in}}{V_{in} - V_{ref}}\right)z_3 - \left(k_p x_3^* + 1/R\right)z_4 + k_i x_3^* z_5, \tag{29}$$

$$\dot{z}_5 = -z_4. \tag{30}$$

Therefore k_p, k_i can be computed numerically to obtain a given closed-loop transient response locally. The complete proposed controller is shown in the block diagram of Figure 5.

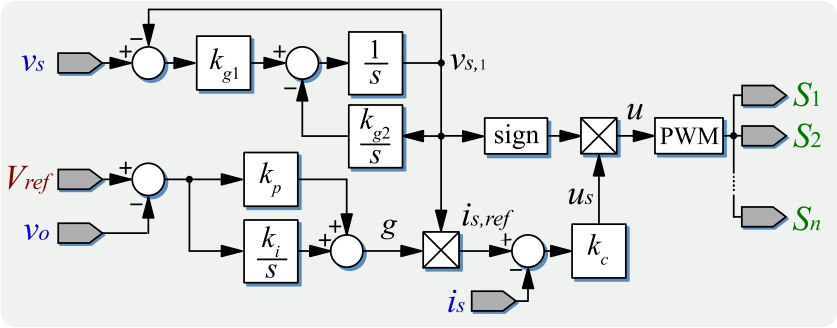

Figure 5. Diagram of the proposed controller.

In order to cope with possible distortion in the grid voltage, an estimator of the fundamental component $v_{s,1}$ is implemented as in [37], where $k_{g1} > 0$ is a constant that is related to the velocity of the convergence of the estimation, and $k_{g2} = \omega_s^2$. Then, $v_{s,1}$ is used in the controller instead of the possibly distorted v_s.

It is worth noting that although the design of the output dynamic control proceeds by assuming constants, the v_i voltage has a second harmonic grid frequency component, and therefore, the output voltage regulation is performed in average. The guidelines for converter parameter selection are presented in Section 3. These result in a range of converter

parameters for which the closed-loop operation will produce the expected results. As long as the current of L_l remains discontinuous in the steady state, and the current of L_i and the voltage of C_i remain continuous, the operation of the converter will vary qualitatively little in open loop, and the conditions for the controller will be preserved. Regarding the control parameters, all the gains are positive and do not directly depend on the converter parameters. Then, slightly modifying the controller gains is expected to slightly modify the closed-loop transient response, such as damping, overshoot, and settling time.

5. Experimental Results

Experimental tests are carried out to verify the performance of the closed-loop system in a laboratory prototype with $n = 4$ interleaved cells. The fine adjustment of the converter and control parameters is established by means of numerical simulations. For the converter parameters, the general rules described previously are followed. For example, the current of each inductor of the interleaved cells is discontinuous, which is ensured by setting L_1, L_2, L_3, and L_4 less than $L_{o,c}$ in (2). In addition, the current of L_I and the voltage of C_i are continuous at steady state and are selected according to (14). Regarding the control parameters, all the gains are positive and do not directly depend on the converter parameters. However, some general rules can also be followed, for example, k_c is chosen to be greater than k_p to force decoupling between input current and output voltage dynamics. The higher the gain k_i, the faster the convergence to the output voltage reference during voltage reference transitions or load changes. However, overshoot and oscillations increase, and a large value will lead to instability. In the estimation of the fundamental component, k_{g2} must be equal to ω_s^2, and k_{g1} is only required to be positive. The gain k_{g1} has an effect only at startup and is related to the speed of convergence for the generation of the current reference. The higher the gain k_{g1} is, the faster the convergence will be in the generation of the current reference $i_{s,ref}$ without any stability issue.

The parameters of the converter are shown in Table 1, and the experimental prototype is shown in Figure 6. The controller is implemented using the digital signal processor DSP TMS320F28335, and the switching signals are generated with the ePWM modules c2833x of the same DSP circuit. For the active switches, the CoolMOS^{TM} transistor SPP20N60C3 is used; for the output inductors, the power inductor 60A363C from Murata is used; and, for the freewheeling diodes, the SiC diode IDD10SG60C is utilized.

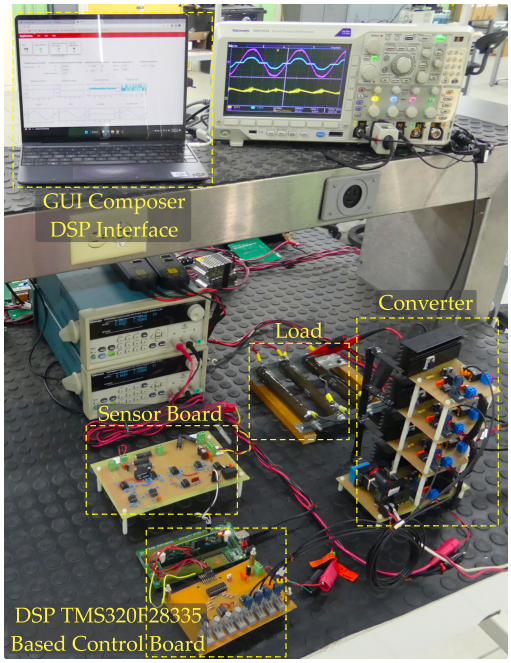

Figure 6. Experimental setup of the proposed multi-phase interleaved AC–DC step-down converter with power factor improvement.

Table 1. Converter parameters.

Parameter	Value
Input Voltage	127 V_{RMS}
Nominal Load R	73 Ω
Switching Frequency f_{sw}	50 kHz
Grid angular frequency ω_s	120π rad/s
Nominal Output Voltage V_{ref}	60 V
Input Inductor L_i	500 µH
Interleaved Inductors L_1, L_2, L_3, L_4	36 µH
Input Capacitor C_i	0.47 µF
Output Capacitor C_o	820 µF

5.1. Steady-State Response

In this subsection, the closed-loop responses in the steady state due to two different output voltage references are presented. The reference $V_{ref} = 60$ V represents a power of 49.3 W, and the reference $V_{ref} = 90$ V represents a power of 110.1 W.

In Figure 7, at the top, the grid voltage v_s and the grid current i_s are depicted, and at the bottom, the output voltage v_o, with the converter functioning at a power of 49.3 W. It can be observed that every depicted waveform is continuous and has a very low switching ripple. Moreover, current i_s is in phase with v_s, although there are non-conduction intervals around the crossing of v_s waveform with zero volts. This is because if the grid voltage is less than the output voltage at any time, then the grid is not supplying power at that time. The output voltage v_o is almost constant at the required voltage reference V_{ref} with small amplitude oscillations whose main frequency is double the grid frequency due to the rectification process. The amplitude of these oscillations is related to the value of the capacitor C_o and the magnitude of the current i_a.

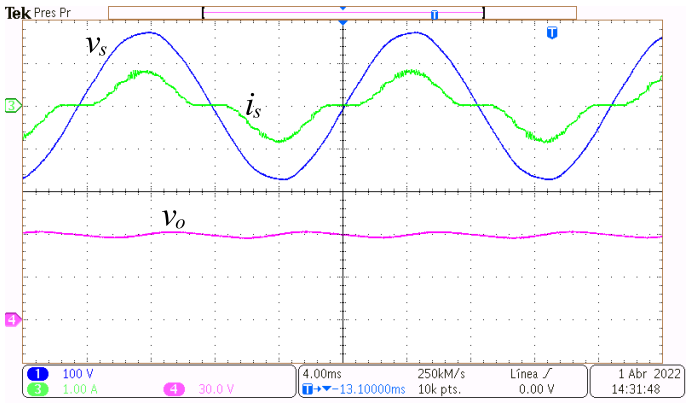

Figure 7. Steady-state operation at 49.3 W. Grid voltage v_s (y-axis 100 V/div, x-axis 4 ms/div), grid current i_s (y-axis 1 A/div, x-axis 4 ms/div), and output voltage v_o (y-axis 30 V/div, x-axis 4 ms/div).

In Figure 8, the grid voltage v_s and its Fast-Fourier-Transform (FFT) are depicted at the top, and the grid current i_s and its FFT, are depicted at the bottom, with the converter functioning at a power of 49.3 W. It can be seen that the grid voltage is almost a clean sinusoidal by having fundamental components only at the grid frequency. The grid frequency fundamental component of current i_s is the largest magnitude harmonic component; however, other components appear due to the distortion caused by the non-conduction time intervals.

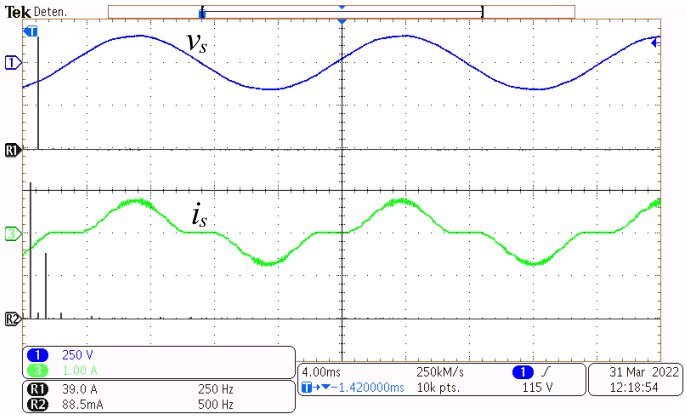

Figure 8. Steady-state operation at 49.3 W. Grid voltage v_s (y-axis 250 V/div, x-axis 4 ms/div), its FFT $v_{s\text{FFT}}$ (x-axis 250 Hz), grid current i_s (y-axis 1 A/div, x-axis 4 ms/div), and its FFT $i_{s\text{FFT}}$ (x-axis 500 Hz).

In Figure 9, at the top, the grid voltage v_s and the grid current i_s are depicted, and at the bottom, the output voltage v_o, with the converter functioning at a power of 110.1 W. In contrast to when it functions at a lower power, as depicted in Figure 9, the current i_s has a larger amplitude, and the non-conduction intervals have increased. Nonetheless, v_s, i_s and v_o are continuous and have very low switching ripple. Additionally, i_s is in phase with v_s. The voltage v_o is almost constant at the required voltage reference $V_{ref} = 90$ V with small amplitude oscillations due to the rectification process.

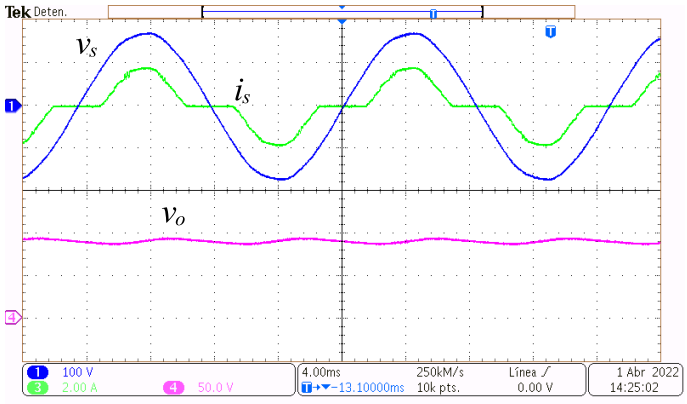

Figure 9. Steady-state operation at 110.1 W. Grid voltage v_s (y-axis 100 V/div, x-axis 4 ms/div), grid current i_s (y-axis 2 A/div, x-axis 4 ms/div), and output voltage v_o (y-axis 50 V/div, x-axis 4 ms/div).

In Figure 10, the grid voltage v_s and its Fast-Fourier-Transform, FFT, are depicted at the top, and the grid current i_s and its FFT, are depicted at the bottom, with the converter functioning at a power of 110.1 W. The same observations can be done as with Figure 8; however, current amplitude, as well as harmonic component amplitudes, have increased.

The Figure 11 presents the capacitors voltages v_i and v_o at a reference of $V_{ref} = 90$ V. The voltage v_i is shown at the top of the figure, and its waveform has a fundamental frequency twice the grid frequency. During the non-conduction intervals, v_i, on average, equals the output voltage v_o. The voltage v_i is decreasing during the non-conduction intervals. Apart from the non-conduction intervals, C_i is charged, and its voltage is approximately the rectified AC source voltage. At the bottom of the figure, v_o is depicted.

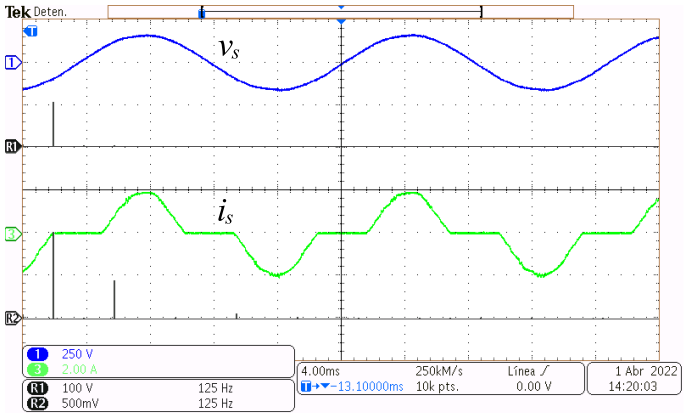

Figure 10. Steady-state operation at 110.1 W. Grid voltage v_s (y-axis 250 V/div, x-axis 4 ms/div), its FFT $v_{s\,\mathrm{FFT}}$ (x-axis 125 Hz), grid current i_s (y-axis 2 A/div, x-axis 4 ms/div), and its FFT $i_{s\,\mathrm{FFT}}$ (x-axis 125 Hz).

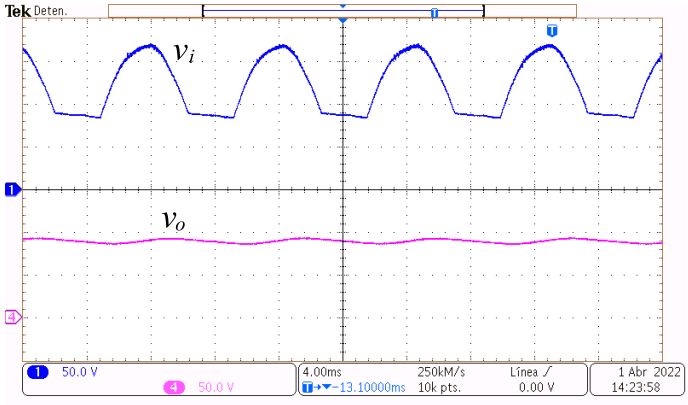

Figure 11. Steady-state operation at 110.1 W. Input capacitor voltage v_i (y-axis 50 V/div, x-axis 4 ms/div), and output voltage v_o (y-axis 50 V/div, x-axis 4 ms/div).

The Table 2 summarizes the steady-state power quality parameters for the two different powers tested.

Table 2. Power quality parameters.

	49.3 W	**110.1 W**
Displacement Power Factor DPF	1	1
Power Factor PF	0.94	0.91
Input Current THD	35.9%	45.4%

5.2. Transient Response

In this section, the experimental transient responses under step-like changes of the output voltage reference and load resistor are presented.

In Figure 12, from top to bottom, the output voltage v_o, the grid current i_s and the load current i_R transient responses are depicted. The transient is caused by step-like changes of V_{ref} from 60 V to 90 V and back.

In Figure 13, from top to bottom, the output voltage v_o, the grid current i_s and the load current i_R transient responses are depicted. The voltage referenced is set constant $V_{ref} = 60$ V while the load resistor is changed from 73 Ω to 48 Ω and back.

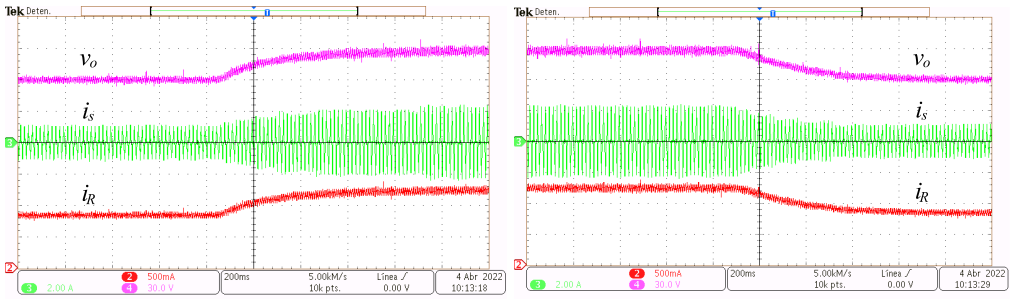

Figure 12. Transient response to step reference voltage changes. Output voltage v_o (y-axis 30 V/div, x-axis 200 ms/div), grid current i_s (y-axis 2 A/div, x-axis 200 ms/div) and load current i_R (y-axis 500 mA/div, x-axis 200 ms/div).

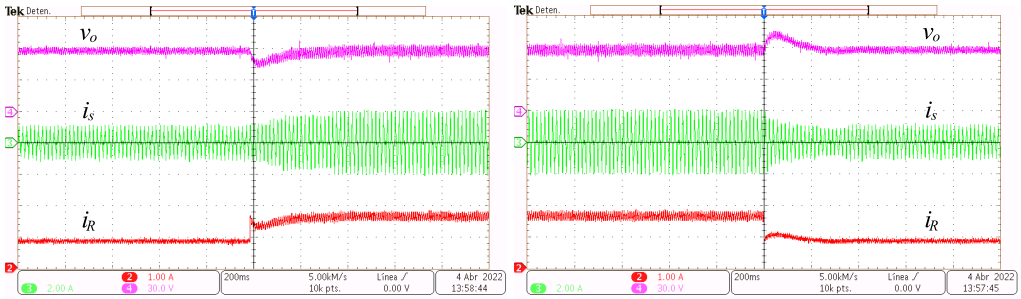

Figure 13. Transient response to step load changes. Output voltage v_o (y-axis 30 V/div, x-axis 200 ms/div), grid current i_s (y-axis 2 A/div, x-axis 200 ms/div), and load current i_R (y-axis 1 A/div, x-axis 200 ms/div).

6. Conclusions

The converter design of a single-phase step-down rectifier with PFC capabilities that is based on an interleaved buck converter together with its control has been presented. The converter achieved power factor improvement on the AC power supply while at the same time being able to maintain a lower regulated DC output voltage relative to the peak AC input voltage. The proposed controller, with a simple structure, a reduced number of sensors, and a single independent switching signal for the converter, achieved the objectives of AC current tracking and DC voltage regulation. Given the proposal for interleaved operation, the size of the output filter has been reduced with components of lower current and voltage ratings compared to components of a single switching cell in discontinuous conduction mode. High-frequency conducted noise produced using discontinuous conduction mode operation that can be injected into the grid is mitigated by the input LC filter. The high voltage spikes that withstand semiconductor devices during hard switching were reduced for a given converter power because the total current and voltage ratings were shared between each interleaved switching cell. An experimental prototype with four switching cells was built and tested to validate the proposed converter and controller. The closed-loop converter was evaluated both in steady state and in transient conditions. At steady state, the converter achieved a power factor above 0.9 with a maximum of 45.4% THD at 110.1 W. The relatively high total harmonic distortion was due to the fact that the converter was based on the buck topology, and when the required output voltage was less than the value of the grid voltage, the grid current was zero, which led to periods of non-conduction around the zero crossings of the grid voltage. Thus, harmonic distortion was reduced when lower output voltages were required. The contributions of the work were, on the one hand, the presentation of the analysis of the converter operating in discontinuous conduction mode, which allows for obtaining the design parameters of the converter. On the other hand, analysis and steady-state operation waveforms were presented. Another contribution was the controller that addresses the regulation of the DC output voltage and the tracking of the input current to a sinusoidal. The dynamics

of the input current and output voltage were considered to be naturally decoupled due to the proposed operation; thus, the controller achieved the objectives using the feedback of only three variables, namely the AC grid voltage, the AC grid current, and the DC output voltage. Interleaved operation provides redundancy to the converter, and closed-loop operation can be expected to achieve control objectives under open-circuit faults in the interleaved switching cell semiconductors, as long as the current or voltage of the semiconductors does not exceed their safe and reliable operating limits. Therefore, in future work, the fault-tolerance capabilities of the closed-loop converter can be experimentally investigated, improved, and evaluated. The solution has potential applications in any system that contains a rectification stage, which is required to reduce voltage level and power factor improvement, for example, in battery charging, LED-based lighting, and as a DC power source for electronic equipment.

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