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A Novel Asymmetric Trench SiC Metal–Oxide–Semiconductor Field-Effect Transistor with a Poly-Si/SiC Heterojunction Diode for Optimizing Reverse Conduction Performance

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Abstract: In this paper, a novel asymmetric trench SiC MOSFET with a Poly-Si/SiC heterojunction diode (HJD-ATMOS) is designed to improve its reverse conduction characteristics and switching performance. This structure features an integrated heterojunction diode, which improves body diode characteristics without affecting device static characteristics. The heterojunction diode acts as a freewheeling diode during reverse conduction, reducing the cut-in voltage ($V_{\text{cut-in}}$) to a lower level than conventional asymmetric trench SiC MOSFET (C-ATMOS), while maintaining a similar breakdown voltage. Meanwhile, the split gate structure reduces gate-to-drain charge (Q_{gd}). Through TCAD simulation, the HJD-ATMOS decreases $V_{\text{cut-in}}$ by 53.04% compared to the C-ATMOS. Both Q_{gd} and switching loss are reduced, with a decrease of 31.91% in Q_{gd} and 40.29% in switching loss.

Keywords: silicon carbide; heterojunction; asymmetric trench MOSFET; low cut-in voltage; switching loss

1. Introduction

The wide bandgap semiconductor properties of silicon carbide (SiC) make it a promising candidate for the development of future power switching devices [1,2]. This is primarily due to SiC possessing properties such as a strong breakdown field, high physical and chemical stability, high thermal conductivity, and high electron saturation velocity [3–5]. SiC devices can operate in harsh environments due to their wide band gap of 3.25 eV and high thermal conductivity of 5 W/(cm·K) [6]. The SiC MOSFET is the most significant SiC power switching device due to its lack of trail current. This reduces switching loss and radiator volume, improving system power density [7].

SiC MOSFETs commonly make use of parasitic body-PN diodes as freewheeling diodes (FWD) in power inverter and converter systems [8]. However, parasitic body-PN diodes in SiC MOSFETs are not ideal for use as freewheeling diodes [9]. The reasons for this are as follows: Stacking faults (SFs) in SiC devices may cause reliability issues and increase conduction loss [10]. Although recent papers concerning the measured degradation of SiC MOSFETs [11] show a high level of current threshold (about 5× the nominal current or more than 1000 A/cm^2) for the starting of bipolar degradation, bipolar degradation effects can still occur in SiC MOSFETs under large cyclic pulse current densities. This will limit the application of SiC MOSFET devices in key areas, such as the surge current that flows through a diode during the start-up of a power converter, which can be more than ten times its rated current [12]. Furthermore, the body diode's $V_{\text{cut-in}}$ voltage (~2.7 V) is much higher than that of its silicon counterparts due to SiC's wide bandgap [13]. To overcome the drawbacks of parasitic body-PN diodes, numerous approaches have been devised to deactivate them. One approach is to integrate SiC MOSFETs with Schottky barrier diodes (SBDs) [14–17]. However, the use of external diodes not only introduces parasitic inductance, limiting switching frequency, but also consumes additional area in the

package [18]. And Schottky contacts suffer from a significant increase in reverse leakage current at high temperatures.

Furthermore, SiC MOSFETs with low-barrier and heterojunction diodes are available [19,20]. Heterojunction diodes formed between polysilicon and SiC are attractive. Shenoy and Baliga [21] and Yamagami et al. [22] presented studies on heterojunction diodes using P-Poly-Si and n-6H-SiC, and Poly-Si and 4H-SiC, respectively. Both studies demonstrated low-forward-voltage Schottky-like characteristics. Ni et al. [23] proposed a trench SiC MOSFET integrating polysilicon/SiC HJD, exhibiting excellent freewheeling diode (FWD) performance in both the first and third quadrants. The HJD's unipolar behavior, similar to that of a Schottky diode, effectively suppresses the turn-on of the problematic body diode, mitigating the aging degradation observed in conventional SiC MOSFETs. Additionally, HJDs reduce reverse recovery voltage and losses, enhancing long-term operational reliability. Furthermore, HJD integration eliminates the need for a separate SBD, leading to a smaller chip area, simpler packaging, and reduced overall system cost. This also minimizes parasitic inductance arising from additional components.

A novel asymmetric trench SiC MOSFET with a heterojunction diode at the right of the gate trench is proposed and simulated in this paper. The structure includes a trench gate with split-gate electrodes and a thicker P-Poly-Si layer, resulting in reduced gate charge and improved switching performance. To suppress the depletion layer, an n-type doped current spreading layer (N-CSL) is formed under the entire P-well region [24]. To maintain the breakdown voltage (BV) of the device structure while maintaining transfer and output characteristics similar to those of C-ATMOS [25–27], the depth of the P-well on the right side is not changed. The N-channel (N_{ch}) is positioned below the P-Poly-Si and in contact with the CSL. The integrated HJD structure of the proposed device eliminates the requirement for an anti-parallel SiC SBD during reverse conduction. The HJD turns on at a low source–drain voltage (V_{sd}), thus eliminating bipolar degradation by inactivating the body diode. The split gate results in a decrease in gate charge, leading to a reduction in switching losses in the HJD-ATMOS without affecting other characteristics.

2. Device Structure and Mechanism

The schematic cross section of HJD-ATMOS and C-ATMOS is shown in Figure 1. Similar to C-ATMOS, the device forms an inversion layer channel in the first quadrant to facilitate electron conduction. The N-CSL layer on the N-drift region reduces the on-resistance. Deep P-wells are used to reduce the electric field stress in the gate oxide at the trench bottom and corner [27]. The primary distinction is the body diode structure. The N_{ch} region under the P-Poly-Si provides a low-barrier path for electrons. Meanwhile, the HJD-ATMOS has a split gate and HJD structure on the right of the gate oxide layer. The split gate structure uses only a portion of the trench space for the gate electrode, while the other part is thicker P-Poly-Si that forms a portion of the HJD structure. The HJD-TMOS facilitates low-voltage conduction by allowing electrons to cross the lower heterojunction barrier in the third quadrant. The structure of N_{ch} and N-channel doping concentration (N_{nch}) will be further discussed based on this optimization in this paper. Device specifications are presented in Table 1.

Table 1. Main parameters used in the simulation.

Parameter	HJD-ATMOS	C-ATMOS
T_{drift}	9 μm	9 μm
T_{CSL}	1 μm	1 μm
W_{CSL}	0.9 μm	0.9 μm
N_{drift}	7×10^{15} cm^{-3}	7×10^{15} cm^{-3}
W_{cell}	2.7 μm	2.7 μm
T_{OX}	50 nm	50 nm
D_T	1 μm	1 μm
L_G	0.25 μm	-

Table 1. *Cont.*

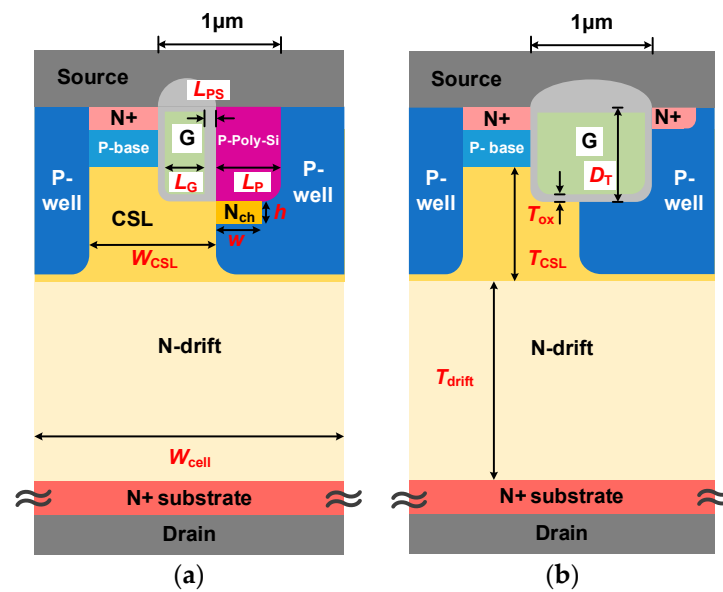| Parameter	HJD-ATMOS	C-ATMOS
L_P	0.6 μm	-
L_{GP}	0.1 μm	-
h	0.3 μm	-
w	0.5 μm	-
N_{nch}	2×1017 cm^{-3}	-
$N_{P\text{-Poly-Si}}$	1×1020 cm^{-3}	-
N_{CSL}	2.5×10^{16} cm^{-3}	2.5×10^{16} cm^{-3}
Fixed charges (SiC/SiO$_2$)	6×10^{11} cm^{-2}	6×10^{11} cm^{-2} [28]

Figure 1. Schematic cross section of (**a**) HJD-ATMOS and (**b**) C-ATMOS.

Sentaurus TCAD simulations are used to analyze the performances of the HJD-ATMOS and the C-ATMOS, considering doping and temperature-dependent Shockley–Read–Hall and Auger recombination, doping-dependent transport, impact ionization, band narrowing, high-field velocity saturation, and mobility degradation [29], as well as fixed charges at the SiC/SiO$_2$ interface for closer simulation results to experimental data.

The energy band diagram of the P-Poly-Si/N-SiC heterojunction at thermal equilibrium is shown in Figure 2b. The energy band diagram at thermal equilibrium along the A-A' cut-line is shown in Figure 2a. The heterojunction has a conduction energy gap of 0.46 eV and a valence barrier energy gap of 1.78 eV. The electron barrier height Φ_{BN} is determined by the Fermi level energy E_f and the conduction band peak energy E_c, which is about 1.39 eV. Figure 2c shows the simulated carrier density at the heterojunction interface under forward bias at the rated voltage. Electrons are injected from N-SiC to P-poly, but there are few holes from P-poly to N-SiC due to the high hole barrier. Therefore, the HJD exhibits unipolar action, similar to the SBD [30].

We also constructed a 3D band diagram of the device to better observe the working state of the device. Figure 3a shows the 3-D conduction band energy distribution of the device at V_{ds} = 10 V and V_{gs} = 15 V. The band energy of N_{ch} is higher than that of N-CSL, which prevents electron current from flowing to P-poly and enables the device to work normally like C-ATMOS. Figure 3b shows the distribution of the devices when V_{ds} = −5 V and V_{gs} = −5 V. The band energy of N_{ch} is lower than that of N-CSL, resulting in electron current flowing from N-CSL to P-poly and preventing the turn-on of parasitic body-PN diodes.
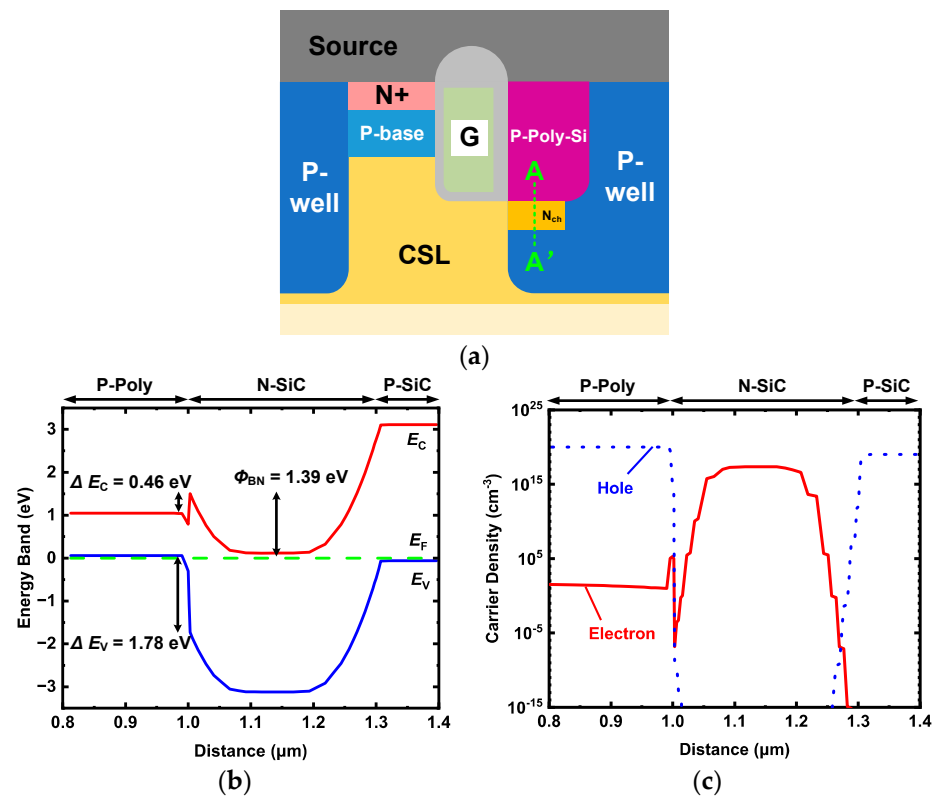
(a)

(b)

(c)

Figure 2. (**a**) Schematic cross section of HJD-ATMOS; (**b**) energy band diagram at thermal equilibrium along the A-A' cut-line; (**c**) carrier density of the HJD when forward biased at rated voltage.
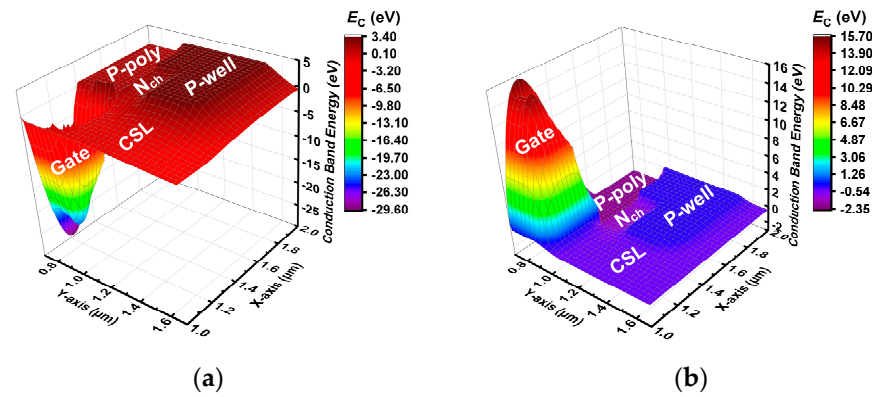

(a)

(b)

Figure 3. Three-dimensional conduction band energy distribution between P-poly, gate, N_{ch}, N-CSL, and P-well (**a**) when conduction is forward and (**b**) when conduction is reverse.

Figure 4 shows the distribution of the total current density, hole current density, and electron current density of the device. From the total current density distribution, it can be seen that the current does not flow from P-Poly-Si to P-well. But a high current density is also noted at the gate corner of P-Poly-Si, which should be noted in use. From the hole current density distribution, it can be seen that holes do not enter N-drift. This is due to the difference in the band gap between SiC and polysilicon. Since the energy barrier height between the SiC and polysilicon junctions in the valence band is very large, in the HJD-ATMOS, electron current can move toward the source while hole current cannot move toward the drain [31]. The device can operate normally at electron current densities of 10 A/cm^2 and 500 A/cm^2.
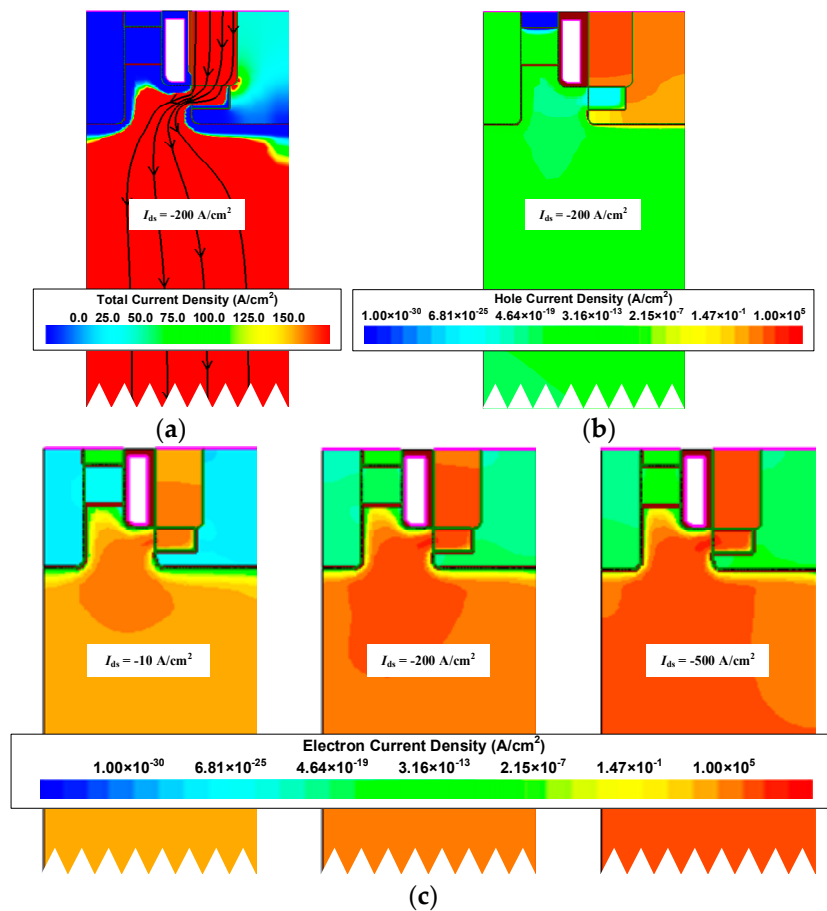
Figure 4. (**a**) Total current density distribution, (**b**) hole current density distribution, and (**c**) electron current density distribution at low and high current in the reverse conduction.

Figure 5 shows the I–V curves of HJD-ATMOS and C-ATMOS in forward and reverse conduction at room temperature. The steeper slope of the I–V curve of HJD-ATMOS in the first quadrant indicates that its specific on-resistance ($R_{on,sp}$) is lower than that of C-ATMOS. This is because the presence of N_{ch} in HJD-ATMOS results in a smaller depletion region of P-well on N-CSL, leading to a wider current conduction region. According to the calculations, at V_{gs} = 15 V and I_{ds} = 200 A/cm^2, the $R_{on,sp}$ values for HJD-ATMOS and C-ATMOS are 1.35 mΩ·cm^2 and 1.46 mΩ·cm^2, respectively. In the third quadrant, at I_{ds}= −10 A/cm^2, HJD-TMOS exhibits a significantly lower V_{cut-in} of only 1.39 V compared to the PN diode of C-TMOS. As a result, HJD-ATMOS is capable of reducing switching losses. The rated operating current of the device in the third quadrant is generally I_{ds} = −200 A/cm^2 [8]. This means that the proposed HJD-ATMOS has a clear advantage over C-ATMOS in that it can start working at a lower voltage. The hole density distribution diagram in Figure 5 for I_{ds} = −200 A/cm^2 shows that the integrated HJD effectively suppresses minority carrier injection, reducing bipolar degradation.

In Figure 6, the local magnification shows that the HJD-ATMOS is affected by current spikes due to leakage. The figure demonstrates the change in breakdown voltage as a function of h and w when N_{nch} is, respectively, 2×10^{17} cm^{-3} and 2.5×10^{17} cm^{-3}. It can be observed that when N_{nch} is 2.5×10^{17} cm^{-3}, with h at 0.25 μm and w at 0.5 μm, the spike in the current is large, indicating the occurrence of leakage. When N_{nch} is 2.5×10^{17} cm^{-3}, increasing h to 0.30 μm and w to 0.4 μm also results in leakage. However, when N_{nch} is 2.0×10^{17} cm^{-3} and h increases to 0.3 μm, the device does not exhibit leakage, demonstrating that variations in N_{nch} have a significant impact on device performance. As shown in Figure 7, V_{cut-in} varies significantly with h. The minimum point of V_{cut-in} is 1.31 V at N_{nch} = 2×10^{17} cm^{-3}, which is lower compared to its value of 1.71 V

at $N_{\text{nch}} = 2.5 \times 10^{17}$ cm^{-3} and $h = 0.2$ μm. This point represents the critical condition for the device not exhibiting leakage when $N_{\text{nch}} = 2.5 \times 10^{17}$ cm^{-3}. After h is greater than 0.25 μm, the variation in $V_{\text{cut-in}}$ with h tends to be flat, and if the value of h is larger, the protective effect of P-well on the gate oxide will also be weakened, and it will also increase the difficulty of process manufacturing. As can be seen from Figure 8, when the device V_{ds} is 0 V, N_{nch} is 2.5×10^{17} cm^{-3}, and h is 0.25 μm, the HJD-ATMOS has more leakage than the device with N_{nch} is 2.0×10^{17} cm^{-3} and h is 0.30 μm. The darker regions in the current density plot for the HJD-ATMOS with N_{nch} at 2.5×10^{17} cm^{-3} and h at 0.25 μm are larger than those with N_{nch} at 2.0×10^{17} cm^{-3} and h at 0.30 μm, indicating higher leakage currents. This also confirms the hypothesis that the breakdown voltage spike is caused by heterojunction leakage. So the results indicate that $N_{\text{nch}} = 2 \times 10^{17}$ cm^{-3}, $h = 0.3$ μm, and $w = 0.5$ μm are the optimal values.
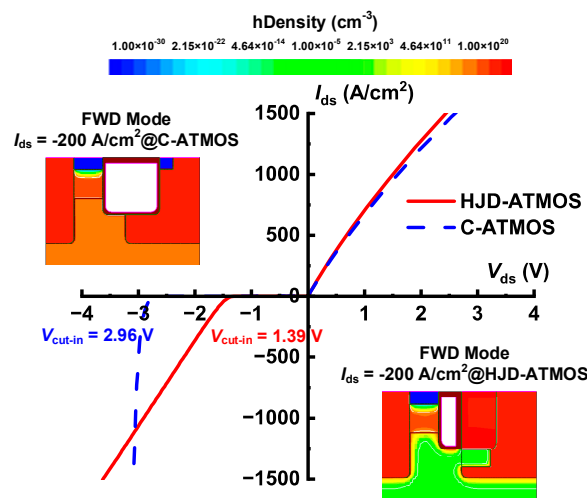

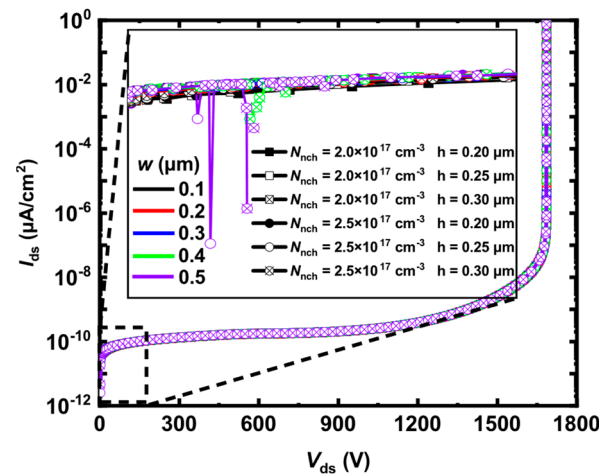**Figure 5.** First and third quadrant characteristics of HJD-ATMOS and C-ATMOS.

Figure 6. The breakdown voltage varies with h, w, and N_{nch}, when N_{nch} is 2.0×10^{17} cm^{-3} and 2.5×10^{17} cm^{-3}, h is 0.20 μm, 0.25 μm and 0.30 μm, and w is 0.1 μm to 0.5 μm, respectively.

(**a**)   (**b**)
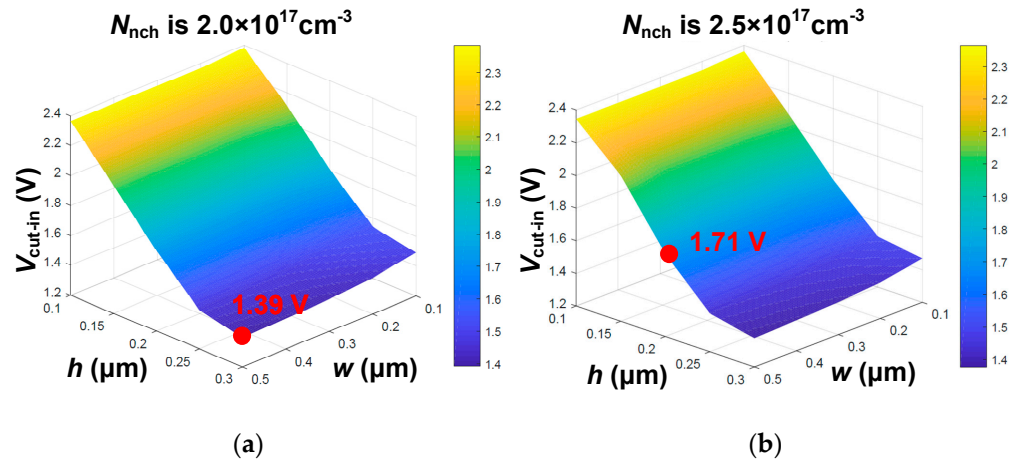
Figure 7. $V_{\text{cut-in}}$ varies with h, w, and N_{nch}, when N_{nch} is (**a**) 2.0×10^{17} cm^{-3}, and (**b**) 2.5×10^{17} cm^{-3}.

(**a**)   (**b**)
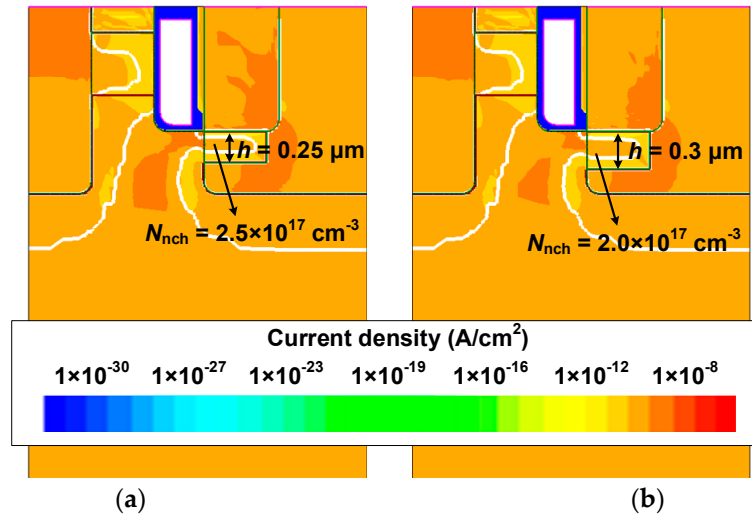
Figure 8. Current density distribution when (**a**) N_{nch} is 2.5×10^{17} cm^{-3}, h is 0.25 μm, and (**b**) N_{nch} is 2.0×10^{17} cm^{-3}, h is 0.30 μm at $V_{\text{ds}} = 0$ V.

3. Simulation Results and Discussion

Figure 9 shows the capacitances of HJD-ATMOS and C-ATMOS. Gate voltage was fixed at 0 V, a 1 MHz AC signal was applied [32,33], and drain voltage was swept from 0 to 1000 V. HJD-ATMOS has lower gate-to-source capacitance (C_{gs}) than C-ATMOS due to the smaller contact area with the source caused by the split gate structure. HJD-ATMOS's gate-to-drain capacitance (C_{gd}) does not decrease. This is because the P-well blocks the right side of the gate of C-ATMOS, performing a similar function as the split gate. Therefore, it can be observed that the C_{iss} ($C_{\text{gs}} + C_{\text{gd}}$) of the HJD-ATMOS with split gates is also smaller than that of the C-ATMOS.

Gate-to-drain charge (Q_{gd}) is critical for power device switching speed in device applications. Figure 10 shows a test circuit to simulate HJD-ATMOS and C-ATMOS gate charges during turn-on. The miller plateau height of HJD-ATMOS is less than that of C-ATMOS, indicating that the threshold voltage of HJD-ATMOS is smaller than that of C-ATMOS [34]. Because the gate charge is proportional to the gate capacitance, the HJD-ATMOS has a lower gate charge (Q_{g}) and Q_{gd} compared with the C-ATMOS. The Miller platform in HJD-ATMOS is shorter because of the reduced gate area. The Q_{gd} values for HJD-ATMOS and C-ATMOS are 32 nC/cm^2 and 47 nC/cm^2, respectively. Q_{gd} of HJD-ATMOS decreased by 31.91% compared to C-ATMOS. Reduced Q_{gd} leads to a smaller high-frequency figure of merit in HJD-ATMOS.
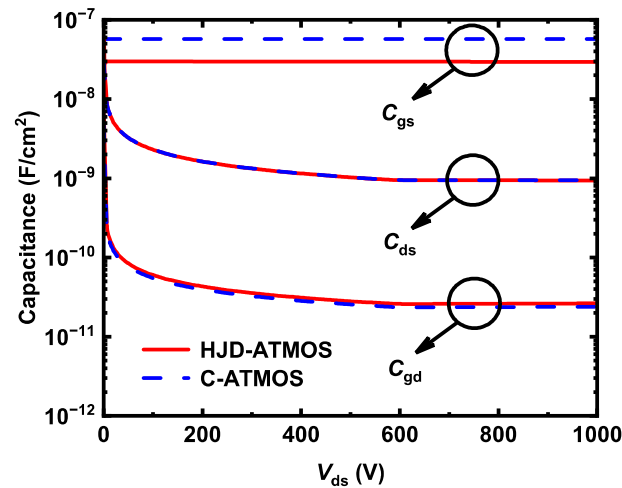
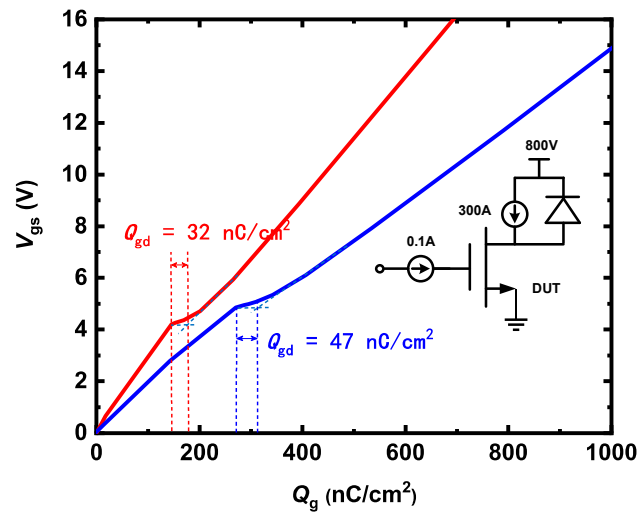**Figure 9.** The device capacitance of HJD-ATMOS and C-ATMOS.

Figure 10. The gate charge characteristics of HJD-ATMOS and C-ATMOS.

Figure 11 shows the electric field distribution at the breakdown of HJD-ATMOS and C-ATMOS. The electric field at the gate oxide of HJD-ATMOS is smaller than that of C-ATMOS. This is because the presence of the N_{ch} introduces a portion of the electric field into this region, which alleviates the electric field that the gate oxide withstands. Although increasing the electric field at the heterojunction raises leakage current risk, it is a trade-off for improved reverse conduction performance. Figure 12 shows the blocking characteristics of the HJD-ATMOS and the C-ATMOS at room temperature and high temperature. At room temperature, the data are represented by solid lines, whereas at elevated temperatures, they are depicted by dashed lines. HJD-ATMOS and C-ATMOS have similar breakdown voltages at room temperature. But the leakage current of the HJD-ATMOS increases at high temperature due to the increased thermal energy of the charge carriers. The generation of leakage currents, as demonstrated and discussed in Figures 6 and 8, arises due to leakage occurring at the heterojunction, where higher N_{nch} and greater values of thickness h both contribute to this effect. By improving the semiconductor material growth process, reducing defects and traps, and enhancing the material quality and interface integrity, it is possible to mitigate non-ideal scattering and trap effects experienced by charge carriers at the heterojunction interface, thus suppressing the leakage current. As discussed in reference [20,35,36], regarding leakage current, while the HJD-ATMOS structure does indeed experience leakage under temperature influence, this leakage is within acceptable limits, with the level of leakage current being 1×10^{-5} µA/cm^2.
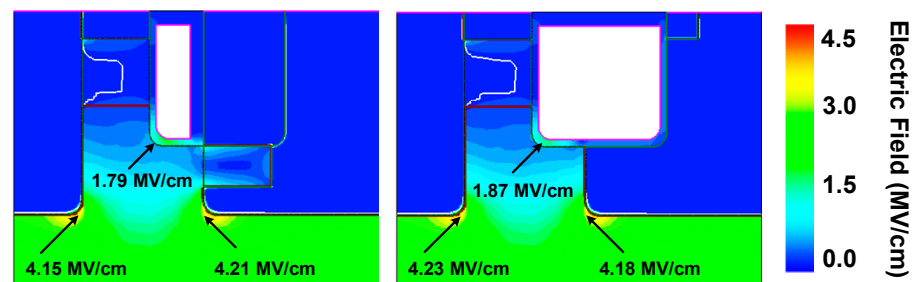
Figure 11. Electric field distribution for the HJD-ATMOS and the C-ATMOS at BV.
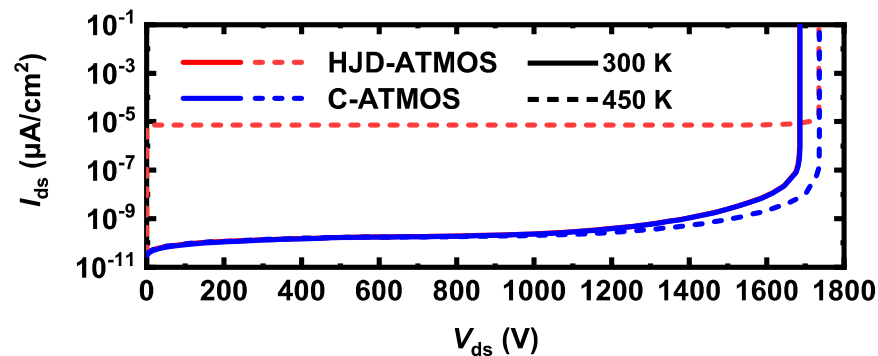

Figure 12. Blocking characteristics of the HJD-ATMOS and the C-ATMOS.

Figure 13 shows a double pulse test circuit for investigating switching characteristics. This is a common circuit configuration employed in device testing [16]. Stray inductance is 10 nH, and load inductance is 80 μH. The gate voltage source (V_g) is turned on from −5 V to 15 V at t = 16 μs and turned off from 15 V to 0 V at t = 11 μs. Figure 14 shows the switching waveforms of devices. The switching speed of the HJD-ATMOS is faster than that of the C-ATMOS with an external SBD diode, which results in a smaller switching loss. Figure 15 compares the switching losses between the two devices. In HJD-ATMOS, the turn-on loss (E_{on}) is 0.26 mJ/cm^2, and the turn-off loss (E_{off}) is 0.41 mJ/cm^2, which demonstrate a reduction of 62.32% and 4.65%, respectively, compared to C-ATMOS. The total switch loss of HJD-ATMOS is reduced by 40.29% compared to C-ATMOS. This is due to the smaller Q_{gd} compared with the C-ATMOS. Reduced switching losses in power electronic devices are instrumental in improving operational longevity and reliability. As losses during switching are directly proportional to heat generation, a significant decrease in these losses curtails thermal build-up, mitigating the risk of device overheating and extending its operational life. This reduction also sustains lower junction temperatures, crucial for preventing material degradation in high-power-density applications where maintaining low operating temperatures is vital for ensuring long-term stability and reliability. Furthermore, minimizing switching losses allows power converters and similar equipment to function efficiently at elevated frequencies without sacrificing efficiency, empowering designers to develop compact, lightweight systems while consistently meeting reliability standards.

The majority of the process steps for HJD-ATMOS, including epitaxial growth, N+ source and P-well implantation, trench etching, P-base implantation, isolation oxidation, gate oxidation, polysilicon gate deposition, and metallization, are fully compatible with the manufacturing processes of C-ATMOS. The N-channel region is formed by ion implantation at the bottom of the trench after trench etching [37]. The split gate is formed by etching after trench oxidation, resulting in a thin layer of oxide between the gate and the P-Poly-Si. The gate-P-Poly-Si trench isolation layer is formed by thermal oxidation, and the trench oxide layer is fully etched and filled with P-Poly-Si.

Table 2 compares the HJD-ATMOS and the C-ATMOS in terms of their main characteristics. Dynamic FOM indicates the value of $R_{on,sp} \times Q_{gd}$ [38]. The HJD-ATMOS performs better due to the integrated HJD structure.
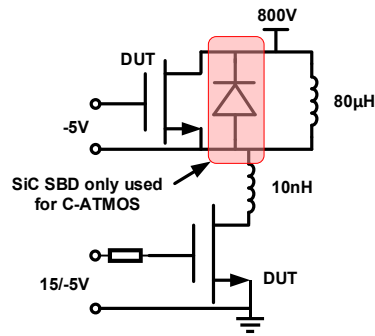
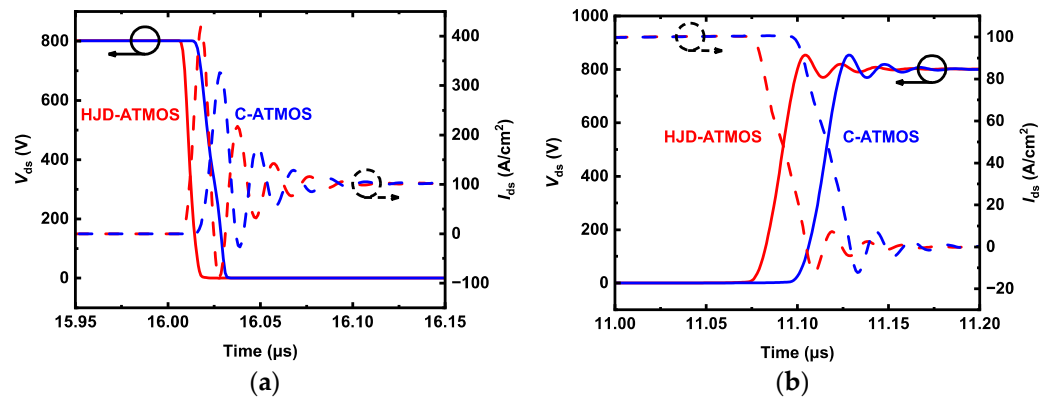**Figure 13.** A circuit for simulating switching with a double pulsed test.

Figure 14. The switching characteristics of HJD-ATMOS and C-ATMOS, including the (**a**) turn-on process and (**b**) turn-off process.
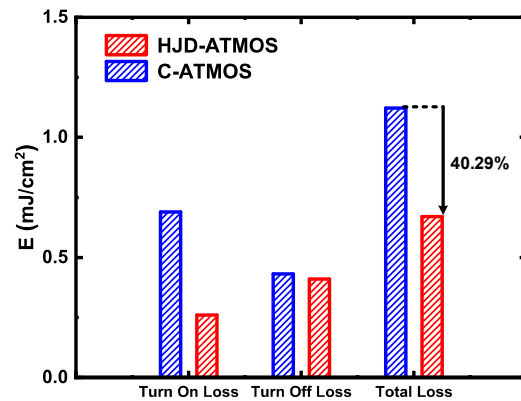

Figure 15. Switching loss comparison of IJ-ATMOS and C-ATMOS.

Table 2. Device characteristics comparison.

Parameter	HJD-ATMOS	C-ATMOS
$V_{\text{cut-in}}$	1.39 V	2.96 V
$R_{\text{on,sp}}$	1.35 mΩ·cm^2	1.46 mΩ·cm^2
Q_{gd}	32 nC/cm^2	47 nC/cm^2
BV	1685.39 V	1686.21 V
E_{on}	0.26 mJ/cm^2	0.69 mJ/cm^2
E_{off}	0.41 mJ/cm^2	0.43 mJ/cm^2
V_{th}	4.28 V	4.86 V
Dynamic FOM	43.20 mΩ·nC	68.62 mΩ·nC

4. Conclusions

This paper proposes a novel asymmetric trench SiC MOSFET with a heterojunction diode. The performance of HJD-ATMOS and C-ATMOS is compared in detail. It can be observed that HJD-ATMOS demonstrates superior third-quadrant performance with a lower $V_{\text{cut-in}}$ because of the integrated HJD. Compared with C-ATMOS, the Q_{gd} of HJD-ATMOS has decreased by 31.91%. This is because the split gate design further reduces the total gate charge, which reduces the switching loss of the HJD-ATMOS device without affecting other key characteristics. As a result, HJD-ATMOS eliminates bipolar degradation and reduces the turn-on loss from 0.69 mJ/cm^2 in C-ATMOS to 0.26 mJ/cm^2. With its advantageous features, HJD-ATMOS is a strong contender for power electronic applications.

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Data Availability Statement: Data is contained within the article.

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