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Article

Self-Assembly of Chip-Size Components with Cavity Structures: High-Precision Alignment and Direct Bonding without Thermal Compression for Hetero Integration

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Abstract: New surface mounting and packaging technologies, using self-assembly with chips having cavity structures, were investigated for three-dimensional (3D) and hetero integration of complementary metal-oxide semiconductors (CMOS) and microelectromechanical systems (MEMS). By the surface tension of small droplets of 0.5 wt% hydrogen fluoride (HF) aqueous solution, the cavity chips, with a side length of 3 mm, were precisely aligned to hydrophilic bonding regions on the surface of plateaus formed on Si substrates. The plateaus have micro-channels to readily evaporate and fully remove the liquid from the cavities. The average alignment accuracy of the chips with a 1 mm square

cavity was found to be 0.4 μm. The alignment accuracy depends, not only on the area of the bonding regions on the substrates and the length of chip periphery without the widths of channels in the plateaus, but also the area wetted by the liquid on the bonding regions. The precisely aligned chips were then directly bonded to the substrates at room temperature without thermal compression, resulting in a high shear bonding strength of more than 10 MPa.

Keywords: self-assembly; room-temperature bonding; direct bonding; liquid; surface tension; cavity chip; hetero integration

1. Introduction

Traditional robotic pick-and-place chip assembly takes a great investment of time to precisely align and tightly bond large numbers of device chips and components onto substrates, such as printed wiring boards (PWB), flexible printed circuits (FPC), and Si wafers. In general, the pick-and-place assembly requires sophisticated die bonders or flip-chip bonders equipped with high-resolution cameras, high-precision multiaxis stage positioners, and ultrafast operation robots with special picking-up tools called collets. The alignment accuracy resulted from mechanical assembly using commercially available high-performance bonders is ±2 μm (model FC 2000 Flip-Chip Bonder, Toray Engineering Co., Ltd., Japan) [1]. The assembly throughput is 1.8 s per a chip (2,000 units per hour) although the cycle time does not include processing time (*i.e.*, loading, bonding and vacuum release). Such bonding equipment has increasingly enhanced the alignment accuracy for assembling chips having high-density metal microbump electrodes with a pitch of less than 5 μm [2]. The alignment accuracy of ±0.5 μm can be obtained with a higher-performance bonder (model OF 2000 Super High Accuracy Flip-Chip Bonder, Toray Engineering Co., Ltd., Japan). The assembly throughput is 15 s per a chip (240 units per hour) [3]. Higher alignment accuracy can be usually realized by longer alignment time. The tradeoff problem between alignment accuracy and assembly throughput is inextricable for present-day mechanical chip alignment and bonding.

In contrast, liquid-mediated chip self-assembly is well known to be an innovative solution for massively parallel assembly. In the last 15 years, a number of regular [4-13] and review [14-17] papers describing the liquid-mediated chip self-assembly have been published. A great advantage in the liquid-mediated self-assembly is that a large number of chips can be simultaneously and precisely aligned onto predetermined regions in a short time by liquid flow or surface tension as driving forces, and additionally, complicated control systems with robotic operation and various kinds of sensors to precisely catch chip positions at a high resolution are not necessary for chip assembly. The first fluidic self-assembly was reported in 1994, where small trapezoidally-shaped light emitting diodes (LEDs) are self-assembled into anisotropically etched pockets formed on Si substrates by combining gravitational force with shape/size reorganization [4]. So far, small volume droplets of water [5,6], molten solders [7,8], and polymeric solutions [9,10] as liquid mediates have been studied for chip self-assembly. Most papers describe self-assembly with very small, hard to handle, optical device chips, such as LEDs and Si mirrors, which have a side length smaller than 1 mm. In addition, elevated

temperature for melting solders or curing resins is indispensable to precisely align and/or tightly bond the tiny chips onto substrates. In several papers, self-assembly has been demonstrated for positioning the microparts with submicron alignment accuracy [8,9]. In recent years, a wafer-level packaging technology using self-assembly, called dry, uniquely orienting, self-organizing parallel assembly (DUO-SPASS) has been presented for the mounting of millimeter-scale chips in a high yield [11]. Bock *et al.*, have reported a self-assembly technology using a unique surface modification technique for mounting chips on flexible polymeric substrates with roll-to-roll processes [12]. Sariola *et al*., have studied hybrid microhandling combining robotic assembly with self-assembly using capillary force to solve the throughput-alignment tradeoff problem [13].

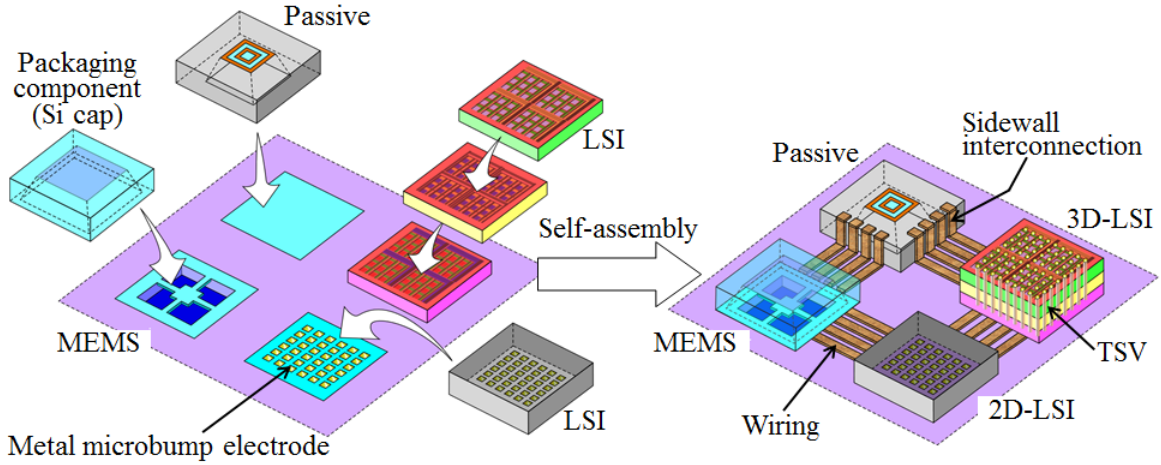
We have demonstrated for the first time that surface tension-driven chip self-assembly, with a small volume droplet of an aqueous solution, can be applied to stack many chips on wafers in batch for three-dimensional large-scale integration (3D-LSI) with TSV (Through-Si Via), in order to overcome the bottleneck of low assembly throughput in conventional pick-and-place alignment and bonding processes [18]. We have further developed 3D integration technologies based on chip-to-wafer stacking using self-assembly techniques [19,20]. In the past two years, several groups have been studying self-assembly using chip-to-wafer stacking for 3D integration [21,22]. On the other hand, heterogeneous system integration with microelectromechanical systems (MEMS) and LSIs has recently been of great interest due to its high functionality and potential applications [23]. A new concept of heterogeneous integration has been proposed in our recent paper, where electrical, mechanical, optical, biomedical, fluidic, and passive devices and components are highly integrated in two- and three- dimensions [24].

This paper deals with self-assembly of chips having cavity structures for 3D and hetero integration of MEMS and LSI, as shown in Figure 1. The representative chips with cavity structures are passive device chips such as on-chip inductors. The elimination of Si substrates underneath inductor chips by micromachining techniques is an effective method because passive device fabrication on Si substrates causes an undesirable increase in parasitic capacitance derived from the Si substrate [25]. The substrate losses from coupling effects between metal strips and the substrate are removed from planar-type inductor chips giving cavity structures that provide a significant increase in quality factor and self-resonant frequency. In this paper we focus on liquid-mediated self-assembly for wafer-level packaging of MEMS devices with cavity chips such as Si caps. In general, MEMS devices have brittle thin moving elements on their chip surface for sensing mechanical quantities such as pressure, accelerated velocity, gravity force, and so on. Therefore, packaging technologies that do not damage the moving elements are of technical interest.

In our self-assembly, aqueous solutions, including hydrogen fluoride (HF), have been used so that chips can be precisely aligned to hydrophilic bonding regions formed on substrates, and in addition, the chips can be tightly bonded to the substrates without thermal compression [26]. After chip bonding, no intermediates, such as solder or polymeric materials, exist at the bonding interface between chips and substrates, which is commonly known as direct bonding techniques [27-29]. The direct bonding techniques are widely employed for wafer bonding by which Si/Si, Si/SiO_2, and SiO_2/SiO_2 interfaces can be created without any intermediate adhesive layers. Our aqueous solution, including a small amount of HF, can produce SiO_2/SiO_2 direct bonding at room temperature, thermally-stable bonding interface, and clean interface without adhesives. In this paper, we demonstrate self-assembly with Si

chips with cavity structures and describe the several parameters affecting alignment accuracy of the cavity chips. In addition, we detail the direct bonding mechanism of the self-assembled cavity chips to Si substrates using the HF solutions.

Figure 1. Self-assembly of various kinds of chips with/without cavity structures for MEMS-LSI 3D and hetero integration.



2. Results and Discussion

2.1. Chip and Substrate Fabrication

Five kinds of cavity chips and substrates were formed by anisotropic wet and dry etching. Photomicrographs of the back of the resulting cavity chips and the front of the resulting bonding regions on plateaus formed on Si substrates are shown in Figure 2. The first chip has a cavity with a side length of 1 mm. The second chip has also one cavity, but the side length of the cavity is 2 mm. The corresponding bonding regions on the substrates have the same design to bonding regions formed on the back of the chip except for the area of two channels connected to the outside of the plateaus. The third, fourth, and fifth chips have two, four, and nine pieces of 0.5 mm square cavities and the numbers of channels in the plateaus formed on the corresponding substrates is two, eight, twelve. The channels formed on the substrate for self-assembling the latest chips having nine cavities are thoroughly connected to each other by the formation of additional channels. All channels are 200 μm in width and 10 μm in depth. Figure 3 shows a SEM cross-sectional view of a representative cavity chip. A cavity with a depth of 40 μm is clearly seen in the figure. The resulting cavity structure formed by anisotropic etching with TMAH was approximately 55° in taper angle.

Figure 2. Photomicrographs of fabricated chips with cavities, and substrates with channels.

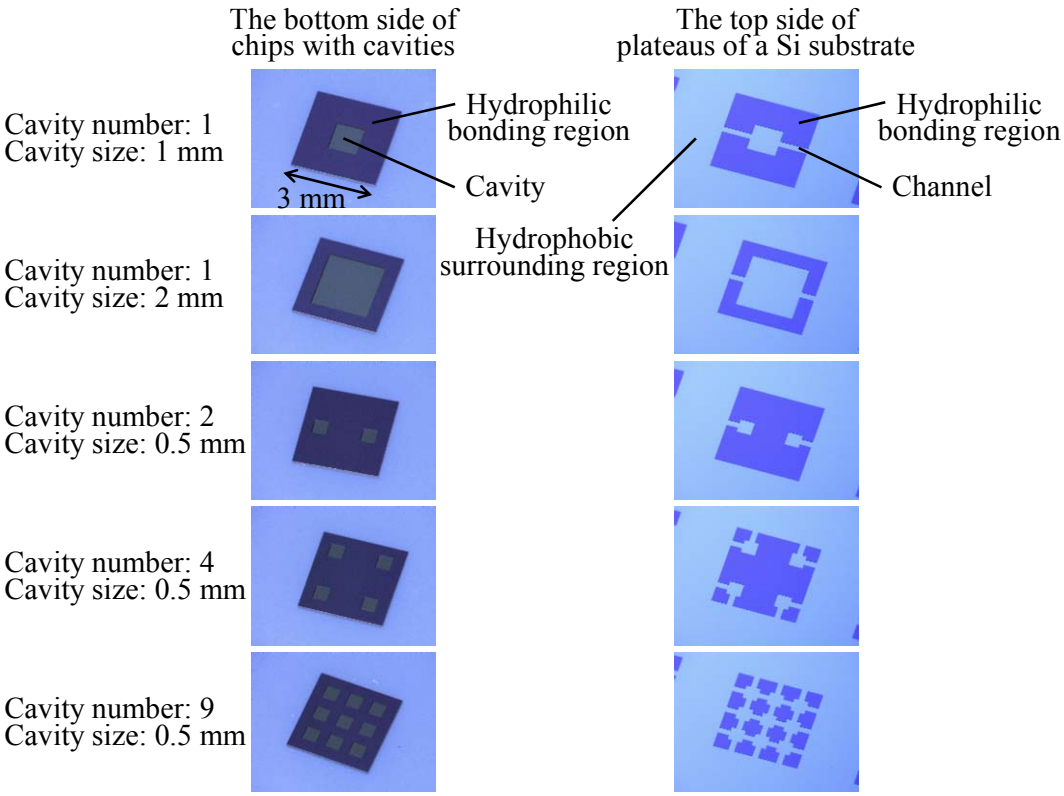


Figure 3. A cross-sectional SEM view of chips with a cavity.

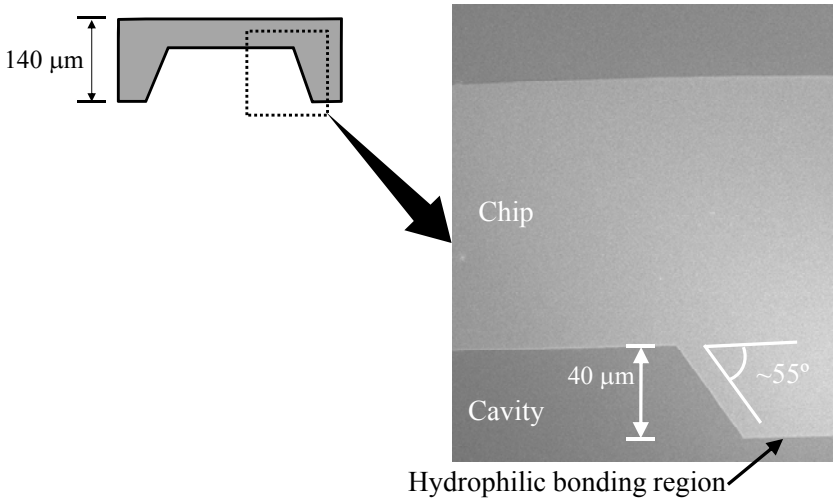


Figure 4(a) shows the results of contact angle measurements with a water droplet added to a bare Si region, and a thermally oxidized Si region, that has the same surface to bonding regions on plateaus formed on substrates. As shown in this figure, the thermally oxidized Si region exhibits an extremely low contact angle of 4°, indicating that the bonding region has high hydrophilicity. In contrast, the bare Si region, exposed by plasma etching, shows hydrophobic property with a contact angle of 80°. Such a relatively high wettability contrast between the hydrophilic bonding regions and the surrounding hydrophobic regions on the substrates leads to a high alignment accuracy. These hydrophilic and hydrophobic properties can be kept for 30 minutes or more at an ambient temperature

and pressure, without any protection from contaminants and particles in a clean room. Figure 4(b) shows the relationship between standing time of a Si substrate and water contact angle on both plateaus and the surrounding regions on the substrate. The initial contact angle on thermal oxide and etched bare Si on the substrate was 4° and 80°. After the substrates had been standing for 120 min, the contact angle on the thermal oxide slightly increased to 8°, indicating that the bonding regions on the plateaus still exhibit high hydrophilic; sufficient to precisely align chips. On the other hand, the surface of bare Si etched by the Bosch process, showed significant reduction of water contact angle, to almost 50°, 120 min after the first measurement. The decrease of the contact angle on the surface of the bare Si exposed by reactive ion etching (RIE) seems to be attributed to re-oxidation of the Si surfaces in air. It will be noted from these results that the high wettability contrast cannot be kept at a high level for more than 60 min without further treatment.

Figure 4. (a) Contact angle on thermal oxide surface (left) and on etched Si surface (right) and **(b)** time course of water contact angle on the oxide surface and the bare Si surface.

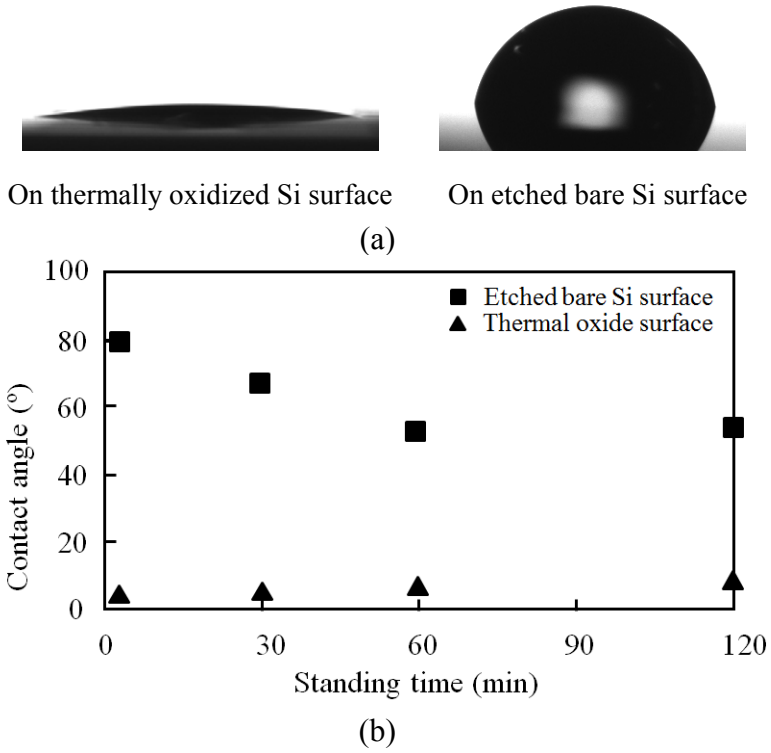
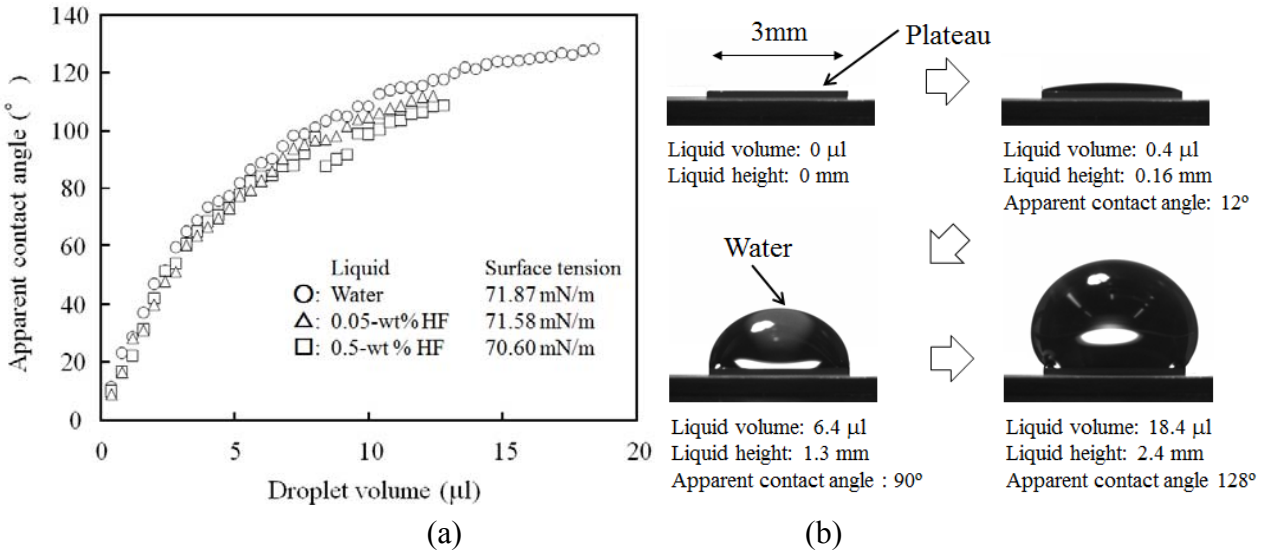


Figure 5(a) shows the plot of apparent contact angle with respect to horizon against the volume of a droplet as more liquid is added. Three kinds of liquid were employed in the experiments: ultrapure water (0 wt% HF solution), 0.05 wt% HF solution, and 0.5 wt% HF solution. The ultrapure water shows the highest surface tension, of 71.87 mN/m, whereas 0.5 wt% HF solution shows the lowest surface tension of 70.60 mN/m. Although the increase in HF concentration slightly lowers the surface tension of water, the amount of the reduction is very small. The three liquids were added to the surface of each bonding region on plateaus formed on a Si substrate (Figure 5(a)). As is also shown in Figure 4, the surface of the thermally oxidized bonding regions on the top of the plateaus was hydrophilic (the intrinsic contact angle is 4°), whereas the bare Si of the surrounding regions including sidewall of the

plateaus was hydrophobic. The apparent contact angle increases with increasing the droplet volume in all three cases. Once each droplet of liquid reaches the edge, the droplet does not overflow and clings to the edge. Upon increasing the droplet volume, the droplets remained confined to the center of the hydrophilic bonding regions until exceeding critical values. The confinement of the liquid droplet is given by the stepwise geometry of the plateaus and by the presence of a ring of air surrounding the plateaus. The critical angle was 128° at the largest water volume of 18.4 μl, which means wettability contrast between bonding regions on plateaus and the surrounding regions is extremely high. Figure 5(b) demonstrates typical cross-sectional pictures of the droplet states in each regime. A small volume of the water droplet can spread to cover the whole bonding region. The resulting apparent contact angle was 12° at the smallest water volume of 0.4 μl. The edge works as a hinge to confine the droplet and the liquid volume grows until it exceeds the critical angle of 128°.

Figure 5. (a) Relationship between droplet volume and apparent contact angle on each bonding region on plateaus and **(b)** cross-sectional images of a water droplet on the bonding region.

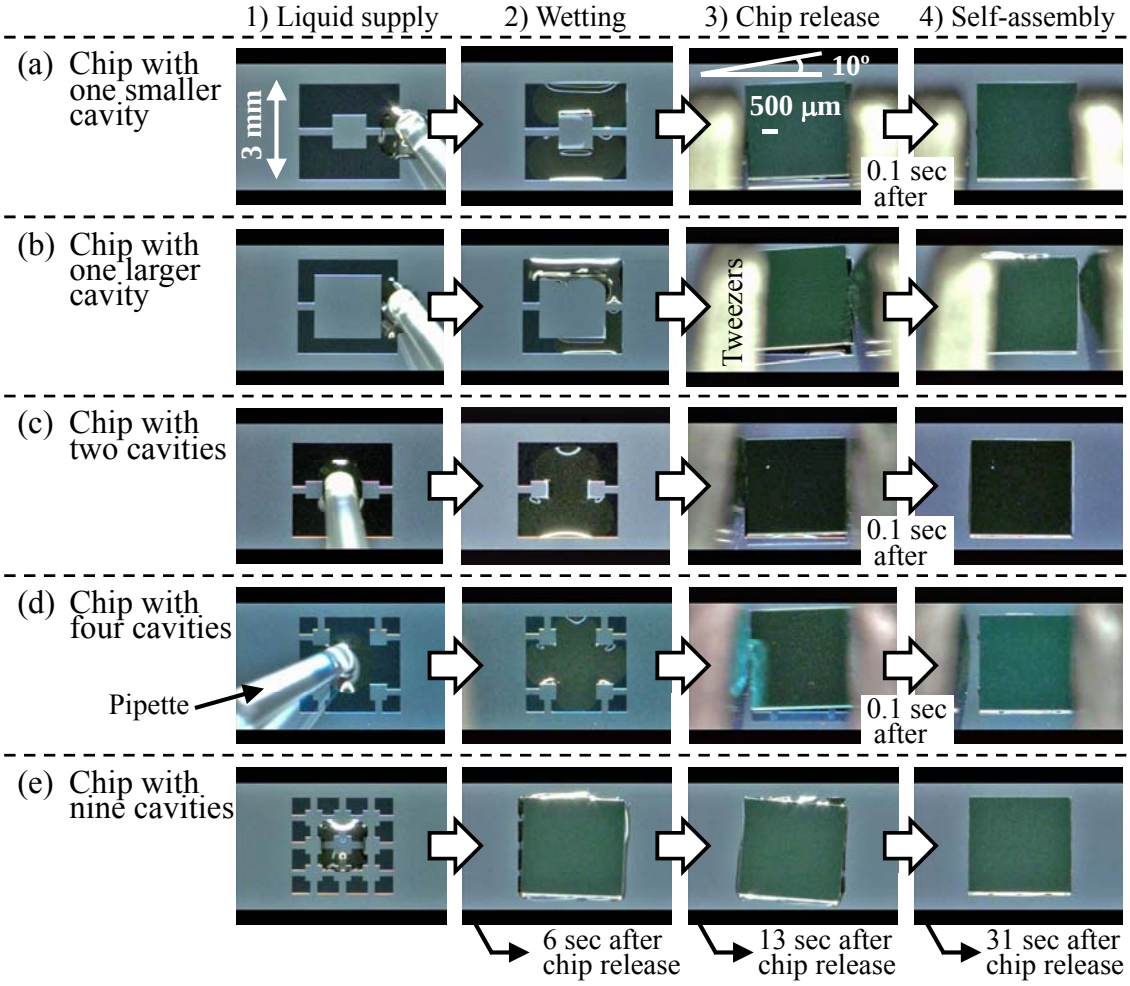


2.2. Self-Assembly of Cavity Chips

Figure 6 shows video frames taken from short movies of self-assembly with various kinds of cavity chips that have a 1 mm square cavity, with a 2 mm square cavity, with 0.5 mm square two cavities, with 0.5 mm square four cavities, and 0.5 mm square nine cavities. First of all, a 0.3 μl liquid droplet was delivered with a micro-pipette to one spot on the surface of a part of each hydrophilic bonding region formed on Si substrates. As seen in Figure 6(a,c), the liquid droplet wets almost all the hydrophilic bonding regions of the first and the third chips. In contrast, as seen in Figure 6(b,d,e), the liquid droplet does not fully spread onto the whole bonding region before chip release when the second, the forth, and the fifth chips are self-assembled. In the case of the self-assembly with the first and the second chips, the liquid droplet was provided on one channel on which the droplet straddles both separated bonding regions. Several seconds later, the liquid droplet was divided into two fluids that selectively wet both the bonding regions. However, the volume of one fluid flows over the upper bonding region,

especially in Figure 6(b), is not necessarily the same as the other fluid which flows to the lower bonding region. Therefore, the chips with a larger cavity are liable to be misaligned to the bonding regions as described below in detail. The first, the third, and the forth chips were precisely aligned immediately after the chips were released from each tweezer to hydrophilic bonding regions formed on the substrates. It takes below 0.1 s to completely align each chip in X, Y, and θ directions from when the chips contact the liquid surface. On the other hand, much longer time was required for the alignment of the fifth chip, as shown in Figure 6(e). The chip with nine cavities travels with the motion of the liquid droplet that gradually wet all of the scattered 16 bonding regions. 31 s after dropping the cavity chip onto the substrate, the chip was aligned and then bonded to the target bonding region.

Figure 6. Video frames from shorts movies of self-assembly with chips having a smaller cavity **(a)**; a larger cavity **(b)**; two cavities **(c)**; four cavities **(d)**; and nine cavities **(e)**.



In our previous study, average alignment accuracy was kept constant at approximately 1 μm when we employed a liquid droplet ranging in volume from 0.3 μl to 1.8 μl for self-assembly of 3 mm square chips [30]. The accuracy was not highly sensitive to the liquid volume in the 0.3 μl to 1.8 μl region. When chips with cavity structures are self-assembling to the bonding regions on plateaus formed on substrates, 0.3 μl droplets of 0.5 wt% HF solution were well confined to the bonding regions. However, the liquid droplets spread within the cavities under the present self-assembly

conditions. 0.3 μl liquid volume used in this study seems to be slightly larger than optimal volume. Self-assembly of the chip with a smaller cavity and the corresponding substrate was monitored with IR microscope. Figure 7 shows IR transmission images of the self-assembling chip and the evaporating liquid through the channels formed on the substrate. As seen in the figure, immediately after chip placement, the chip is driven by surface tension of a small volume of a water droplet; the water used as a liquid for this self-assembly then moves inside the cavity. 4 min after chip release, the liquid trapped within the cavity readily drains through the channel connected to the outside of the chip. Alternatively, the channel allows air to enter the cavity. Finally, the liquid is completely removed, as shown in Figure 7(d). This observation indicates that the channels are effective tools to remove liquid from the cavity and bonding interface. Consequently, many chips with cavities were precisely aligned and directly bonded to bonding regions on the surface of plateaus formed on Si substrates. Figure 8 shows a photomicrograph of an array of self-assembled chips having a smaller cavity on plateaus formed on a structure. Although the bonding interface between the self-assembled chips and the plateaus formed on the substrate is not clearly observed due to mirror images reflected on the surface, the existence of the channel structures can be recognized. It can also be seen from this figure that thin cavity chips with a thickness of 140 μm are successfully self-assembled with a high alignment accuracy.

Figure 7. IR transmission images of a self-assembling chip having one cavity and evaporating liquid through a channel formed on a Si substrate.

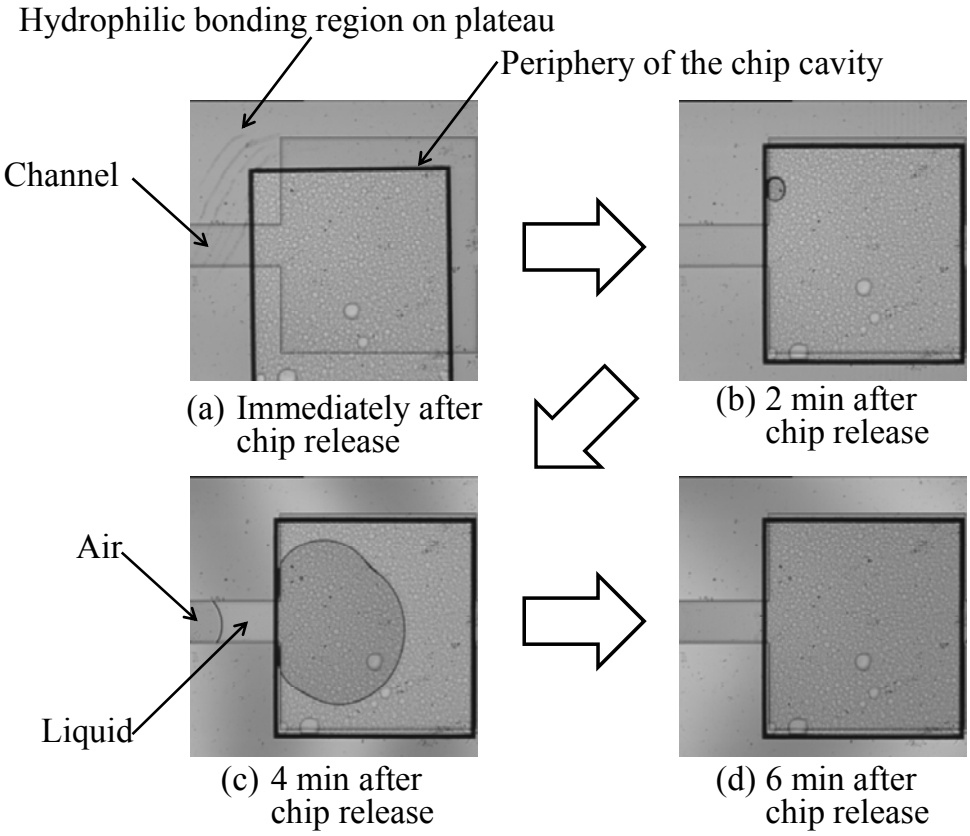
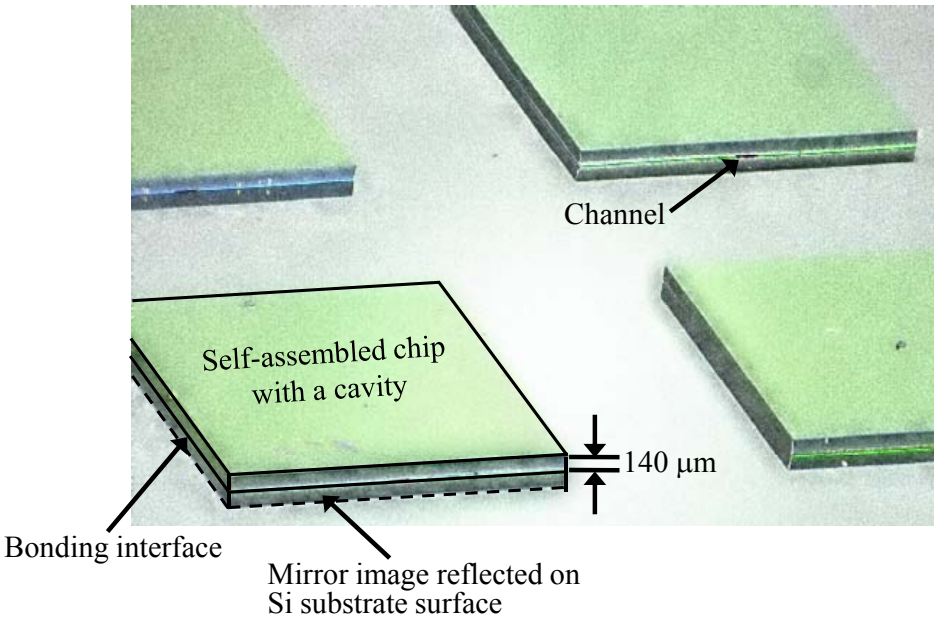


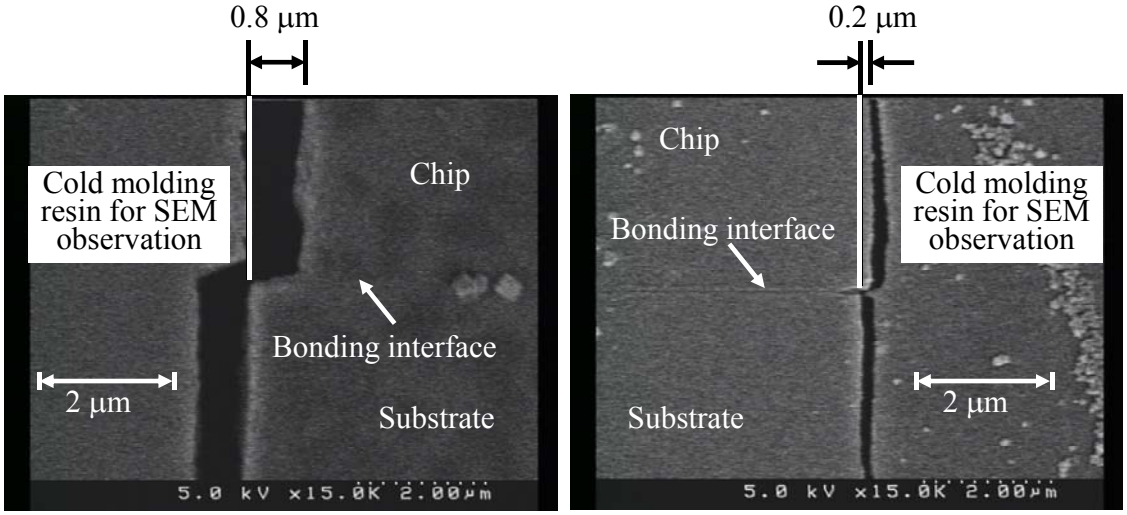
Figure 8. A photomicrograph of the self-assembled chips having cavity structures to the Si substrate with channels.



The self-assembled chips are cut in half and then polished in order to clearly observe the bonding interface by SEM and to evaluate the alignment accuracy. The alignment accuracy of a self-assembled cavity chip was found to be approximately 0.5 μm from cross-sectional SEM observation of the left and right sides of the chip, as shown in Figure 9. The alignment error of the left side was +0.8 μm and that of the right side was +0.2 μm in X direction, leading to the value of alignment accuracy of 0.5 μm. Figure 10 shows effects of both cavity size and the number of cavities on alignment accuracy. Here, chips with a smaller or a larger cavity, chips with two cavities, and chips with four cavities were employed. Each value of alignment accuracy obtained from four pieces of the four kinds of the cavity chips is listed in this figure. The highest average alignment accuracy was 0.4 μm when we used the chips having two cavities. The chips having a smaller cavity showed a little bit higher average accuracy of 0.8 μm than that of 0.9 μm obtained from the chips having four cavities. The latter multi-cavity chips exhibits large accuracy distribution in alignment accuracy, compared to the former single-cavity chips. In contrast, the chips having a larger cavity showed much lower alignment accuracy and larger distribution than the other three chips. The average alignment accuracy was 3.7 μm. For comparison, chip/substrate specifications and the resulting alignment accuracy are summarized in Table 1, where the information of self-assembled chips with nine cavities is also listed. The nine-cavity chips showed the lowest alignment accuracy and the largest accuracy distribution in the five cavity chips. The alignment accuracies of four pieces of the chips with nine cavities were 0.6, 1.6, 46, and 73 μm. As seen in Figure 10 and Table 1, lower alignment accuracy and larger accuracy distribution are liable to result from a decrease in the area of bonding regions on a plateau and an increase in the number of bonding regions scattered on a plateau. Shorter lengths of chip periphery also tend to result in lower alignment accuracy due to a shape recognition effect. The worst alignment characteristics of the nine-cavity chips seem to be attributed to the highly scattered bonding regions on a plateau in addition to small total area (6.75 mm^2) of the bonding regions and the shortest length

(9.6 mm) of chip periphery without channel width. As is seen in Figure 6, however, cases Figure 6(a,c and d) have a large part of their hydrophilic bonding regions connected, while case Figure 6(e) has only isolated hydrophilic islands. In addition, case Figure 6(b) has the smallest area of hydrophilic bonding regions separated, between which liquid volume mismatch is induced in the self-assembly events. Therefore, increases in not only the area of hydrophilic bonding regions and the length of the periphery but also the uniformly- and completely-wetted area of the bonding regions would give higher alignment accuracy and smaller accuracy distribution.

Figure 9. Cross-sectional SEM images of the left and right sides of a chip self-assembled to a Si substrate.



Left side of a self-assembled chip Right side of a self-assembled chip

Figure 10. Effects of cavity size and the number of cavities on alignment accuracy.

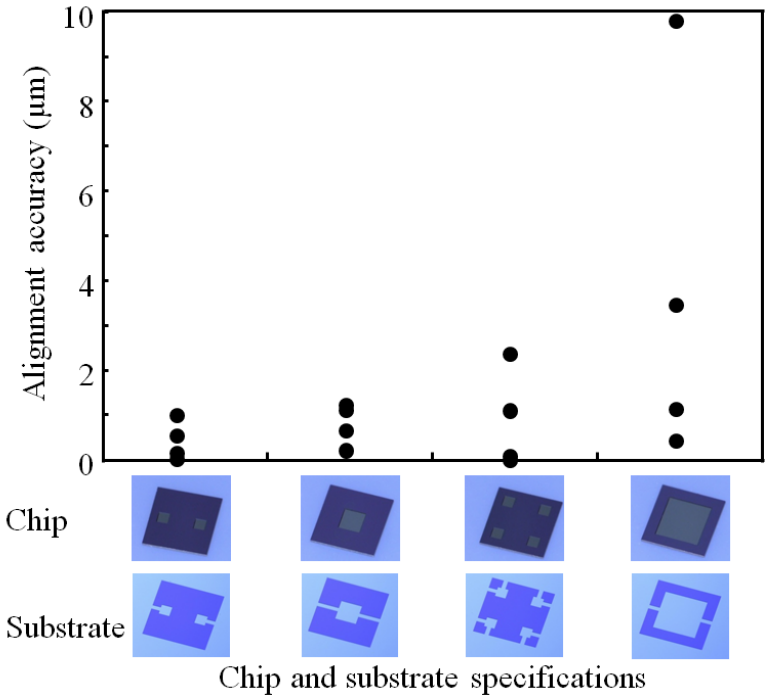
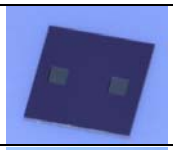
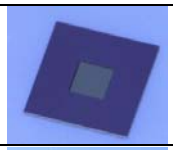
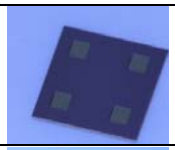
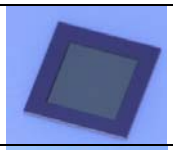
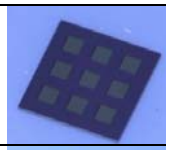
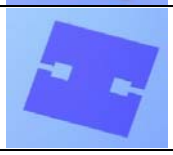
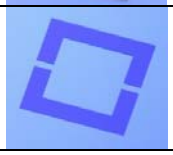
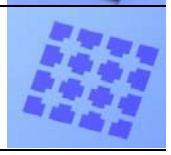


Table 1. Chip and substrate specification and the obtained alignment accuracy.

Chip appearance					
Substrate appearance					
Cavity size (mm)	0.5 × 0.5	1.0 × 1.0	0.5 × 0.5	2.0 × 2.0	0.5 × 0.5
The number of cavity	2	1	4	1	9
Bonding area (mm^2)	8.75	8.00	8.00	5.00	6.75
Total length of chip periphery without channel width (mm)	11.6	11.6	10.4	11.6	9.6
Average accuracy (μm)	0.4	0.8	0.9	3.7	30*

* The chips with 9 cavities showed a large deviation of accuracy: 0.6, 1.6, 46, and 73 μm.

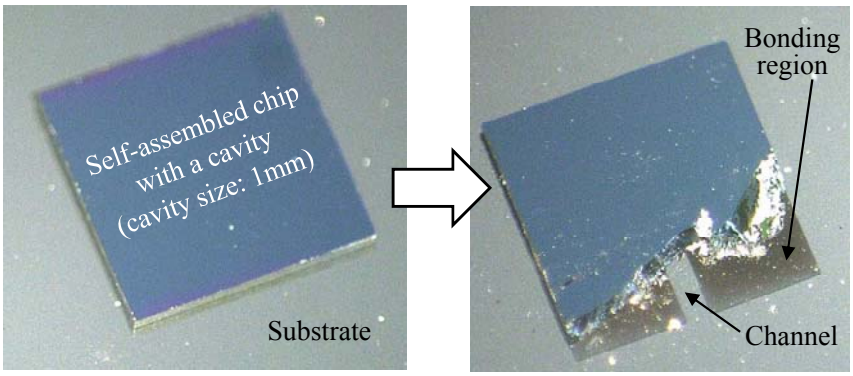
Alignment accuracy also depends on wettability contrast between bonding regions and the surrounding background. In our self-assembly, the contact angle of the former hydrophilic bonding regions on plateaus formed on substrates is below 5°, whereas the latter contact angle is approximately 80°. The plateau structures used in this study can confine a liquid droplet to the center of a bonding region on plateaus. The apparent contact angle with respect to horizon was found to be above 125° when more than 18 μl water was dropped to a 3 mm square bonding region on a plateau, as described in the previous section. Wettability contrast is the key primary parameter for high-precision chip alignment by liquid surface tension. The high wettability contrast can afford high surface tension of the liquid, resulting in high-precision chip self-assembly. In our previous study, chip sizes hardly affected the alignment accuracy in the self-assembly experiments [23]. This is most likely because the driving force acting on self-assembling chips in X-Y direction is higher than the gravitational force (driving force acting on self-assembling chips in Z direction) from their own weight lightened by the buoyancy. Here, the stage inclination was kept within 0.1° and chips were released from several millimeters higher than hydrophilic bonding regions on plateaus formed on substrates. Initial misalignment before chip release is seen in the second view from the right in Figure 6(a): <1 mm in X-Y directions and <10° in θ direction, which were not well controlled due to manual handling. Higher alignment accuracy can be obtained by the optimization of assembly conditions such as stage inclination [26] and initial positioning error of X, Y, Z, θ, $X\theta$, and $Y\theta$ directions before chip release [6].

2.3. Direct Bonding of Cavity Chips

As mentioned in the previous section, after the evaporation of water in HF solution in our self-assembly process, precisely aligned chips can be directly bonded to substrates at room temperature without applying mechanical force to tightly bond the chips to the substrates. Figure 11 shows an experimental result of shear bonding strength measurement for a self-assembled chip having a smaller cavity. As seen in this figure, bulk deformation of the cavity chip was observed after the

shear test. In addition, a channel structure was clearly observed by removing a part of the cavity chip with brittle failure. This result suggests that the cavity chip was successfully self-assembled onto the Si substrate by the surface tension of a small droplet of dilute HF solution.

Figure 11. Shear bonding strength measurement of a self-assembled chip with a smaller cavity to a Si substrate.



Before shear test

After shear test
(Si bulk deformation)

The bonding strength is influenced by the surface roughness on the hydrophilic bonding regions on the surface of plateau structure formed on Si substrates. Here, we used a thin layer of thermal oxide as hydrophilic bonding regions on substrates. The R_a roughness of the plateau surface was 1.82 Å from the AFM observation, as shown in Figure 12. By using the as-deposited thermal oxide, we obtained high shear bonding strengths of over 10 MPa which is enough to allow bulk deformation or edge chipping of the 140 μm thick chips. On the other hand, as-deposited TEOS (tetraethylorthosilicate) oxide, formed by plasma-enhanced chemical vapor deposition, was used for the bonding regions on the substrates. As a result, cavity chips were not able to bond to the substrates. In contrast, high bonding strength comparable to the as-deposited thermal oxide was obtained from polished TEOS oxide by chemical mechanical polishing (CMP) for 1min. The as-deposited TEOS oxide exhibits 4.63 nm in R_a of surface roughness, whereas the polished TEOS oxide exhibits 0.63 nm. From these results, surface roughness turns out to be a key parameter for the load-free room-temperature direct chip bonding by self-assembly. It can be said that TEOS oxide having a very smooth surface is a promising candidate for chip self-assembly because thermal oxide is not necessarily applicable for thermally unstable devices/components and substrates such as PWB and FPC due to the extremely high formation process.

Figure 13 shows cross-sectional TEM images of the bonding interface between a self-assembled chip and a Si substrate when we used 0.5 wt% HF solution as a liquid. The microstructure involving chemical composition and bond distance is relatively changed at the bonding interface between the chip and the substrate. As seen from the magnified view of the thermal oxide-oxide bonding interface, the thickness of an interlayer amorphous layer was approximately 3 nm. In the very thin 3 nm region, HF molecules in water, and silanol groups existing on the bonding regions on the surface of both cavity chips and substrates, chemically react with each other while the liquid fully evaporates within 10 min at the most. Nakanishi *et al*., postulated in their study on SiO_2–SiO_2 compression bonding with hydrofluoric acid that the bonding mechanism is attributed to the existence of a fluorine-atom-containing binding interlayer formed by resolidifications of the dissolved silicon dioxide which resulted from chemical

reaction with HF molecules [31]. Certainly, SIMS measurement (the data is not shown here) indicates that F atom would exist at the oxide-oxide bonding interface between the chips and substrate.

Figure 12. AFM images of bonding regions on the back surface of chips having cavity structures.

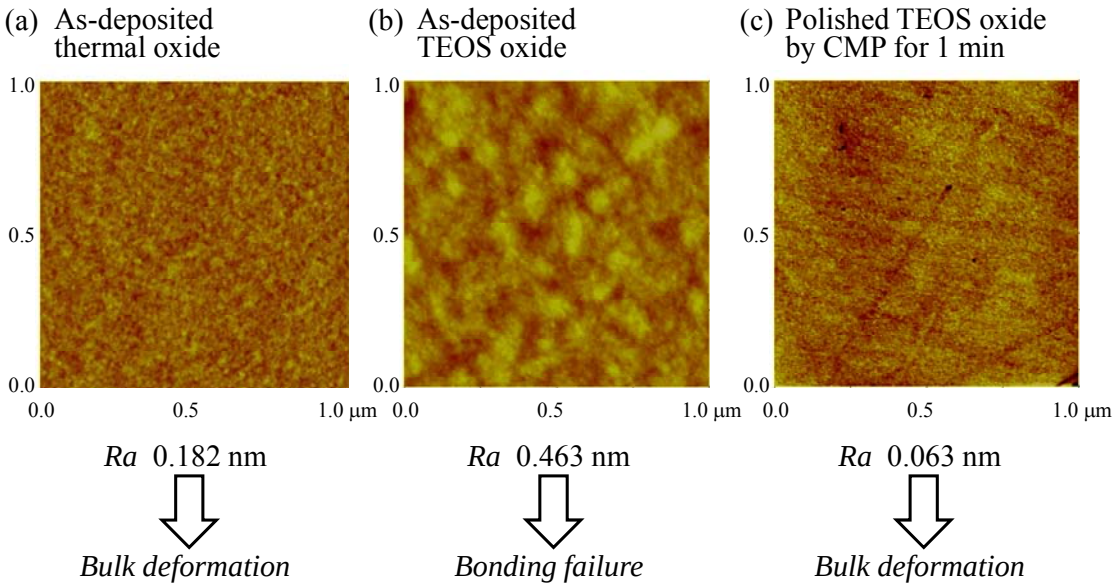
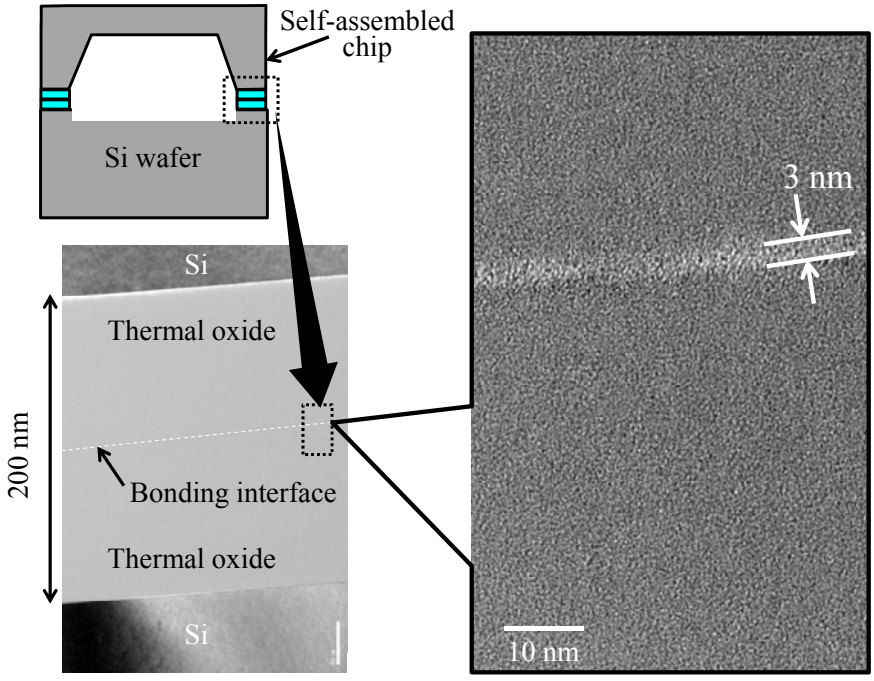


Figure 13. Cross-sectional TEM images of bonding interface between a self-assembled chip and a Si substrate.



We assume that thermally oxidized Si substrates have approximately 1.4 μmol/m^2 of –Si–OH groups on the surface [32], and thus, 0.0126 nmol –Si–OH groups are on the surface of 3 mm-square chips. On the other hand, 0.3 μl of 0.5-wt% HF solution prepared from commercially available 49 wt% HF in water possess approximately 75 nmol of HF in its solution. Even 0.3 μl of 0.005 wt% HF solution includes 0.75 nmol of HF molecules. The HF concentration is high enough to chemically react

with thermal oxide layers at the bonding interface between chips and substrates during water evaporation. We expect that the mechanism of the HF-assisted load-free room-temperature direct bonding is based on liquid-solid chemical reactions between the HF molecules and the surface silanol groups on both chips and substrates to give strong hydrogen bonding networks between the resulting –Si–OH and–Si–F groups [33]. In general, hydrogen bonding energy between hydrogen and fluorine is relatively high (~60–170 kJ/mol), and thereby, some hydrogen bonding between hydrogen and fluorine is comparable to a covalent bonding. In addition, the resulting fresh silanol groups would form siloxane bridges of –Si–O–Si– covalent bonding by fluorine-catalytic dehydration of the silanol groups. Polymerization of silanol groups is possible in the presence of fluorine ion [34]. Furthermore, intermediates such as hexafluorosilicates of end products from HF-SiO_2 reactions in water could be at the bonding interface layer between the chips and the substrates.

3. Experimental Section

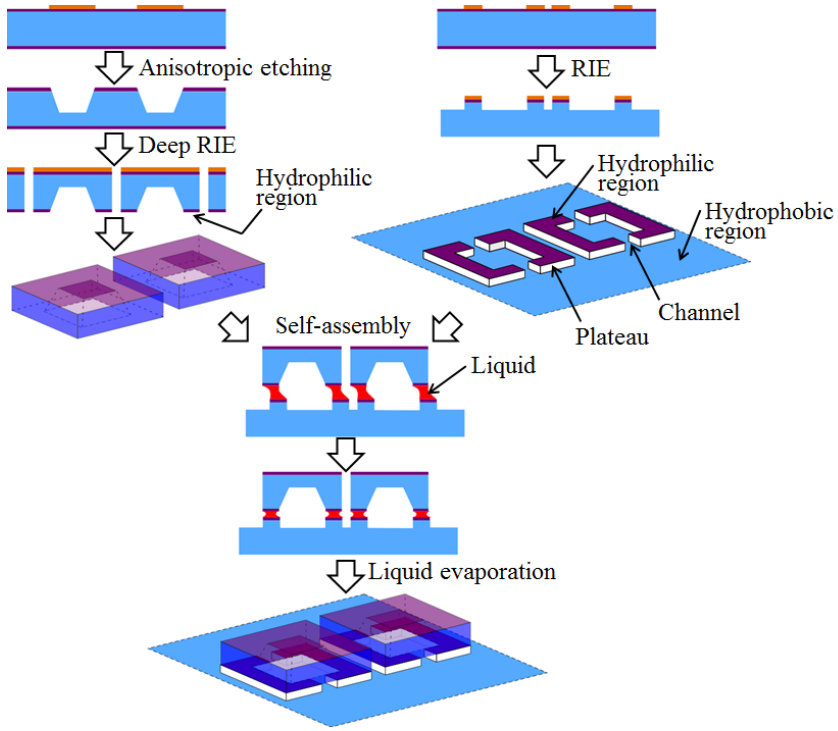
3.1. Chips and Substrates

Process sequences for chip and substrate fabrication and self-assembly with the chips and substrates are schematically shown in Figure 14. 140 μm-thick chips having cavities (0.5 mm-, 1 mm- or 2 mm square on a side) were fabricated with thermally oxidized p-type Si(100) wafers by standard i-line photolithography techniques and the subsequent anisotropic etching with 25% tetramethylammonium hydroxide (TMAH) at 70 °C, followed by plasma dicing using the Bosch process with inductively coupled plasma (ICP) RIE to create precisely defined chip sizes. The resulting chip size was 3 × 3 mm. These chips have hydrophilic bonding regions made of thermal oxide at the backside surface. The thickness of the thermal oxide was approximately 100 nm. The substrates for cavity chip self-assembly were also formed with thermally oxidized Si wafers. Plateau structures having channels with a depth of 10 μm were formed on the substrates by the Bosch process. The top surface of the plateaus is also covered with thermal oxide, and the surrounding regions are air on bare Si. The bonding regions of the chips have the same size to the plateau surface regions except for the area of the channels.

3.2. Self-Assembly

The resulting cavity chips and substrates were cleaned with a solution of $H_2SO_4/H_2O_2/H_2O$ at over 100 °C, followed by additional cleaning with 0.5 wt% HF solution. In the self-assembly operation, first, a 0.3 μl droplet of 0.5 wt% HF solution was dropped onto each hydrophilic bonding region on the plateau surface. Then, the chips with the hydrophilic back were roughly pre-aligned and placed onto the hydrophilic bonding regions. Immediately after chip release, the chips were precisely aligned to the plateaus formed on the substrates. Finally, the chips were bonded on the plateaus at room temperature without applying a load to the chips after liquid evaporation.

Figure 14. A process flow of the fabrication of chips with cavities and substrates with channels.



3.3. Contact Angle

The contact angle was measured on an optical contact angle meter CAM101 (KSV Instruments Ltd.) using a droplet of ultrapure water with a volume of approximately 1 μl by means of the sessile drop method. The droplet was monitored by a high resolution CCD camera and analyzed by Drop Shape Analysis software (CAM 200) utilizing a monochromatic light source which generates the highest quality images with minimal sample heating. The complete profile of the droplet was fitted by the Young-Laplace equation to give the slope at the three-phase boundary where a liquid, gas, and solid intersect. The resulting static contact angles were determined both on the right and left sides.

3.4. Surface Tension

The liquid surface tension was measured by the Wilhelmy plate method on a digital tensiometer CBVP-Z (Kyowa Interface Science Co., Ltd.) using a Pt plate with the specification of 23.8 ± 0.05 mm in width, 0.15 ± 0.02 mm in thickness, and 960 ± 50 mg in weight. The plate insertion depth into each 30 mL liquid was 2.5 mm, and the ascent rate of the plate was 0.2 ± 0.05 mm/s.

3.5. Bonding Strength

The shear bonding strength test was carried out with a multi-purpose bond tester Series 4,000 (Dage Holdings Ltd.). DS100KG and SHR-250-3000 were used as a load cell and a shear tool. The length of the tip of the tool was 3 mm. Measurement conditions were 100 μm/s in shear speed and 20 μm in shear height.

3.6. Alignment Accuracy

The accuracy was determined from both the right and the left sides of alignment errors by scanning electron microscope (SEM) (JEOL JSM-7400F) observation of the bonding interface between self-assembled cavity chips and plateaus formed on substrates. To clearly observe the bonding interface, the self-assembled chips were diced in half with a ceramic blade and then polished.

3.7. AFM

Surface roughness of Si substrates was characterized by atomic force microscopy (AFM). The AFM topography images (512 pixels wide) were obtained with a Digital Instruments NanoScope III operating in tapping mode by use of phosphorous doped Si (1–10 Ω/cm) cantilevers. The length, width, and thickness of the cantilevers are respectively 115 μm, 30 μm, and 3.5 μm, and the cantilevers have a force constant and resonance frequency of 20 Nm^{-1} and 282 kHz, respectively. AFM images were recorded on a maximum scan region of 10 × 10 μm^2 and with a scanning frequency of 0.5 Hz per a line. Though the measurements were carried out in normal ambient conditions, meticulous care was taken to shut out the noise due to external factors. The images were automatically plane-fitted to account for sample tilt, and flattened by use of the standard NanoScope III software.

3.8. TEM

The interface microstructure of bonding interface between self-assembled cavity chips and plateaus formed on substrates was evaluated by field emission transmission electron microscopy (FE-TEM) (Hitachi HF-2000) with an accelerating voltage up to 200 kV for a range of applications requiring high resolution to sub-nm levels. The lattice and point resolution are 0.11 nm and 0.23 nm, respectively. Very thin (0.1 μm or less) samples prepared using an Ar ion milling system illuminated by an electron beam.

4. Conclusions

Self-assembly of Si chips with cavity structures was demonstrated using the surface tension of 0.5 wt% HF solution to achieve MEMS-LSI 3D and heterogeneous integration. The cavity chips were self-assembled with high alignment accuracy within 500 nm to target bonding regions on the surface of plateaus formed on substrates. The self-assembled chips also showed a high shear bonding strength of over 10 MPa. The mechanism of the HF-assisted load-free room-temperature direct bonding is thought to be based on surface chemical reactions between HF molecules and silanol groups on the surface of both chips and substrates to give strong intermolecular forces, such as hydrogen bonding networks between the resulting silanol and silicon fluoride groups.

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