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The Fringe-Capacitance of Etching Holes for CMOS-MEMS

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Abstract: Movable suspended microstructures are the common feature of sensors or devices in the fields of Complementary-Metal-Oxide-Semiconductors and Micro-Electro-Mechanical Systems which are usually abbreviated as CMOS-MEMS. To suspend the microstructures, it is commonly to etch the sacrificial layer under the microstructure layer. For large-area microstructures, it is necessary to design a large number of etching holes on the microstructure to enhance the etchant uniformly and rapidly permeate into the sacrificial layer. This paper aims at evaluating the fringe capacitance caused by etching holes on microstructures and developing empirical formulas. The formula of capacitance compensation term is derived by curve-fitting on the simulation results by the commercial software ANSYS. Compared with the ANSYS simulation, the deviation of the present formula is within $\pm 5\%$. The application to determine the capacitance of an electrostatic micro-beam with etching holes is demonstrated in a microstructure experiment, which agrees very well with the experimental data, and the maximum deviation is within $\pm 8\%$. The present formula is with simple form, wide application range, high accuracy, and easy to use. It is expected to provide the micro-device designers to estimate the capacitance of microstructures with etching holes and predominate in the device characteristics.

Keywords: CMOS; etching holes; fringe capacitance; MEMS

1. Introduction

Movable suspended microstructures are the common key feature of sensors and devices in the fields of Complementary-Metal-Oxide-Semiconductors and Micro-Electro-Mechanical Systems which are usually abbreviated as CMOS-MEMS. To suspend the microstructures, it is commonly required to etch the sacrificial layer under the microstructure layer. For large-area microstructures, it is necessary to design a large number of etching holes on the microstructure to enhance the etchant uniformly and rapidly permeate into the sacrificial layer. However, the etching holes may alter the characteristics of the microstructures, such as mechanical properties [1], magnetic field [2] and electrical field [3–6]. According to the aforementioned literature, etching holes have great influences on the characteristics of micro-devices not only the mechanical but also the electrical properties.

For parallel-plate capacitive micro-devices, etching holes may decrease the parallel-plate capacitance but increase the fringe capacitance due to the fringe fields of the inner perimeters of the etching holes. As a result, etching holes make evaluating the capacitance of microstructures becomes much more difficult. There was some literature that evaluated the two-dimensional [7–11] or three-dimensional [8,9,12] fringe capacitances of the microstructures without etching holes. However,

no literature mentioned the evaluation of the capacitance of perforated microstructures. Therefore, the authors of this work had presented an empirical formula for evaluating the fringe capacitance of etching holes [13]. However, its structural dimension-range was too narrow for practical application for CMOS-MEMS sensors and devices. Therefore, by modifying the previous work, this paper proposes a simple but more accurate empirical formula for compensating the fringe capacitances of etching holes for CMOS-MEMS. We carry out extensive simulations by the use of the commercial software ANSYS (Ansys, Inc., Canonsburg, PA, USA) and then derive an empirical formula by curve fitting on the simulation results. Then, the empirical formula is verified by practical microstructures.

2. Formula Derivation

There are four steps to derive the formula of the capacitance compensation term for etching holes. Firstly, to determine the dominant terms of the influence of etching holes on capacitance, a comparison will be carried out between a perforated and a non-perforated parallel-plate capacitor with the same dimensions. Secondly, ANSYS simulation is employed to compute the capacitance difference. Thirdly, the empirical formula of the capacitance compensation term is derived by curve fitting on the simulation results. Finally, verify the empirical formula by many practical microstructures with different etching holes dimensions.

2.1. The Capacitance Compensation Terms of Etching Hole

Figure 1 shows the cross-sectional view of a capacitive micro-plate-structure. The total electrical fields consist of two parts: one is the uniform field under the bottom-surface of the plate and the other one is the fringe field from the sidewalls and top-surface of the structure. Therefore, the total capacitance (C) is the sum of the parallel-plate capacitance (C_p) under the bottom-surface and the fringe capacitance around the sidewalls and the top-surface (C_f), *i.e.*, $C = C_p + C_f$. For a perforated capacitive micro-plate (Figure 2), the electrical fields may pass through the etching holes and thus alter the total capacitance of the plate. Etching holes are usually uniform-distributed in MEMS fabrication processes to ensure completely removing the sacrificial layer under the structural layer. Therefore, we can divide the whole structure into the combination of many square unit modules and analyze the fringe capacitance of a unit module. Figure 3 illustrates the unit modules as well as their dimensions, where s, s^e, h and g represent the length of unit module, the length of etching hole, the plate thickness, and the gap between the plate and ground respectively.

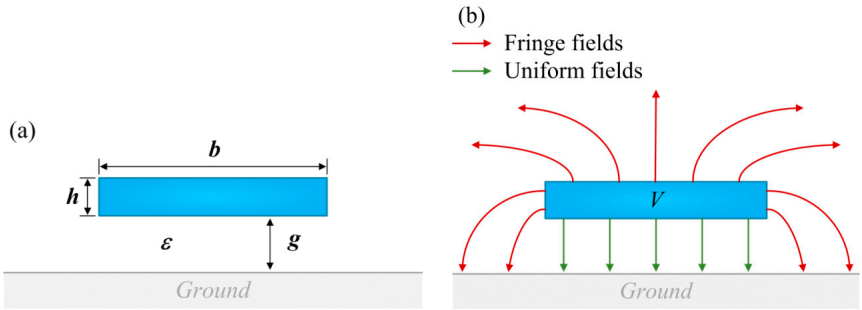

Figure 1. (**a**) The cross-sectional view of a flat-plate capacitor; (**b**) The field lines resulted by a bias voltage V, where b, g, h and ε are width, gap, thickness and permittivity of dielectric, respectively.

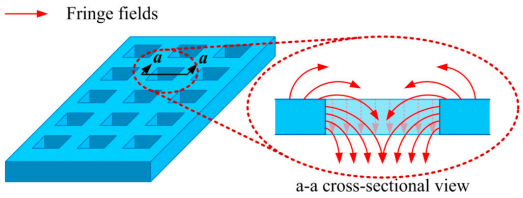

Figure 2. Schematic diagram of the fringe fields of the etching-hole.

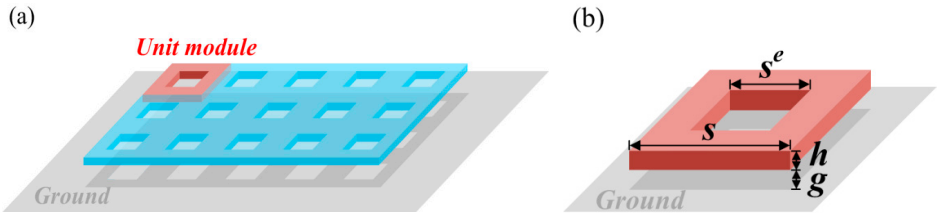

Figure 3. (**a**) Schematic diagram of the capacitive structure with etching holes; (**b**) Schematic diagram of the unit module. s: The length of unit module; s^e: The length of etching hole.

To understand the influence of the etching hole on the total capacitance of a unit module, let us consider a contrastive unit module without etching hole, as shown in Figure 4a, the capacitance can be expressed as:

$$C = C_p + C_f \tag{1}$$

where C is the total capacitance, C_p is the ideal parallel-plate capacitance under the bottom-surface, and C_f is the fringe capacitance around the sidewalls and top-surface. C_p can be calculated by the ideal parallel-plate capacitance formula, namely $C_p = \varepsilon A/g$ where A is the area of the bottom-surface of the unit module. On the other hand, the total capacitance C^e of the unit module with etching hole, as shown in Figure 4b, can be expressed as:

$$C^e = C_p^e + C_f^e \tag{2}$$

where C_p^e is the ideal parallel-plate capacitance under the bottom-surface of the unit module with etching hole, that can be represented as:

$$C_p^e = C_p - C_{p\_hole} \tag{3}$$

where C_{p_hole} is the ideal parallel-plate capacitance of the area that the etching hole occupied; C_f^e is the fringe capacitance that can be approximately represented as:

$$C_f^e = C_f + C_{f\_hole} \tag{4}$$

where C_{f_hole} is the fringe capacitance around the sidewalls and top surface nearby etching hole. By comparing the capacitance between the perforated and non-perforated unit module, a compensation term of etching holes effects on capacitive microstructures will be carried out. The formula of the capacitance compensation term (ΔC) of etching hole can be expressed as follows:

$$\Delta C = C^e - C = -C_{p\_hole} + C_{f\_hole} \tag{5}$$

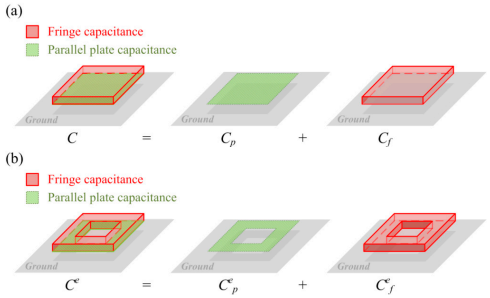

Figure 4. (**a**) Capacitance analysis of the non-etching-hole unit module; (**b**) Capacitance analysis of the etching-hole unit module. C: The total capacitance of the unit module; C_p: The ideal parallel-plate capacitance under the bottom-surface; C_f: The fringe capacitance around the sidewalls and top-surface; C^e: The total capacitance of the unit module with etching hole; C_p^e: The ideal parallel-plate capacitance under the bottom-surface of the unit module with etching hole; C_f^e: The fringe capacitance.

2.2. Simulations by ANSYS

To extract the capacitance compensation terms (ΔC) of etching hole, the commercial finite element software, ANSYS, is employed. Similar to our previous work [13], a series of three-dimensional electrostatic field simulation for the unit modules with different dimensions are carried out. To reduce the computing time, only a quarter of the unit module and electric field is modeling in simulation because of its symmetric (Figure 5). Table 1 shows the parameters of simulation. The size of the etching hole is characterized by the ligament coefficient μ, which is defined as the ratio of the remaining link width (l) to the etching hole pitch, *i.e.*, $\mu = l/pitch$ (Figure 6). The non-perforated unit module ($\mu = 1$) is also simulated as a standard for calculating the capacitance compensation term of etching hole.

We divide the entire electrostatic field region (16μm × 16μm × 16μm) into the three regions with different mesh sizes (Figure 7) and use the element type of Solid 122 to mesh the electrostatic field. Table 2 shows the mesh sizes for each region. There are 27 regions with corresponding mesh sizes. The elements near the electrodes have smaller mesh size due to the rapid changes in electrostatic field. Table 3 compares the capacitances simulated by different mesh densities for different electrostatic field spaces. The simulation results show good convergence, whose deviation is within 1%, even increasing the mesh density and the space of electrostatic field. After a large number of simulations, the capacitances of the perforated and non-perforated unit module with the same dimension would be determined. By the use of Equation (5), the capacitance compensation term of etching hole (ΔC) can be extracted. Figure 8 shows one of the simulation results (s = 8 μm) and it was found that the absolute value of capacitance compensation term increases as the ligament coefficient decreases. However, the capacitance compensation will approach zero with increasing electrode gap. The reason is due to fringe fields filling the area of the etching holes.

Table 1. Parameters of simulation.

Parameters and Units	Values
Length of unit module, s (μm)	4.0, 6.0, 8.0, 10.0, 12.0
Thickness of unit module, h (μm)	1.0
Gaps, g (μm)	0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3, 1.4, 1.5, 2.0, 4.0
Ligament coefficient, $\mu = l/pitch$ [a]	1.0, 0.7, 0.6, 0.5, 0.4, 0.3
Length of the cubic region of the electrostatic field in simulation, f (μm) [b]	16.0

[a] l and *pitch* are shown in Figure 6, [b] f is shown in Figure 5.

Table 2. Mesh sizes and densities.

Position		Mesh Density × 1	Mesh Density × 8
Region	Value	Mesh Size (μm)	Mesh Size (μm)
1	$0 \leqslant x \leqslant s/2 + 0.1$ $0 \leqslant y \leqslant s/2 + 0.1$ $0 \leqslant z \leqslant g + h + 0.1$	0.1	0.05
2	$s/2 + 0.1 \leqslant x \leqslant s/2 + 2.1$ $s/2 + 0.1 \leqslant y \leqslant s/2 + 2.1$ $g + h + 0.1 \leqslant z \leqslant$ $g + h + 2.1$	0.5	0.25
3	$s/2 + 2.1 \leqslant x \leqslant f$ $s/2 + 2.1 \leqslant y \leqslant f$ $g + h + 2.1 \leqslant z \leqslant f$	1	0.5

Table 3. Capacitance comparison with different mesh densities and electrostatic fields for the perforated unit module (s = 8.0 μm, h = 1.0 μm, g = 1.0 μm, μ = 0.5).

Electrostatic Field (μm³)	8^3		12^3		16^3		20^3		24^3	
Mesh Density	C (pF)	Error (%)	C (pF)	Error (%)	C (pF)	Error (%)	C (pF)	Error (%)	C (pF)	Error (%)
×1/8	242.47	−6.60%	256.60	−1.16%	260.08	0.18%	261.33	0.66%	261.88	0.88%
×1	242.05	−6.76%	256.13	−1.34%	259.61	0.00%	260.85	0.48%	261.40	0.69%
×8	241.88	−6.83%	255.94	−1.41%	259.41	−0.08%	260.65	0.40%	261.20	0.61%

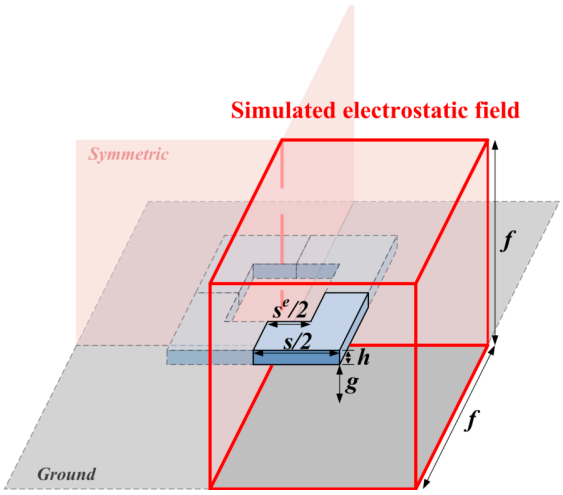

Figure 5. Scheme of simulation model. f: Length of the cubic region of the electrostatic field in simulation.

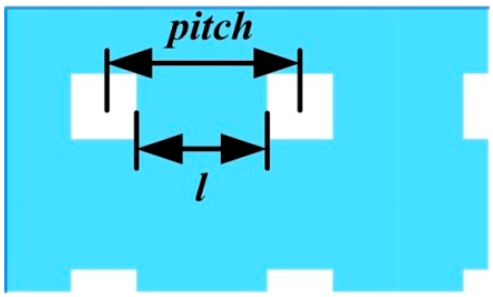

Figure 6. Scheme of ligament coefficient μ = $l/pitch$. l: The interval between two etching holes.

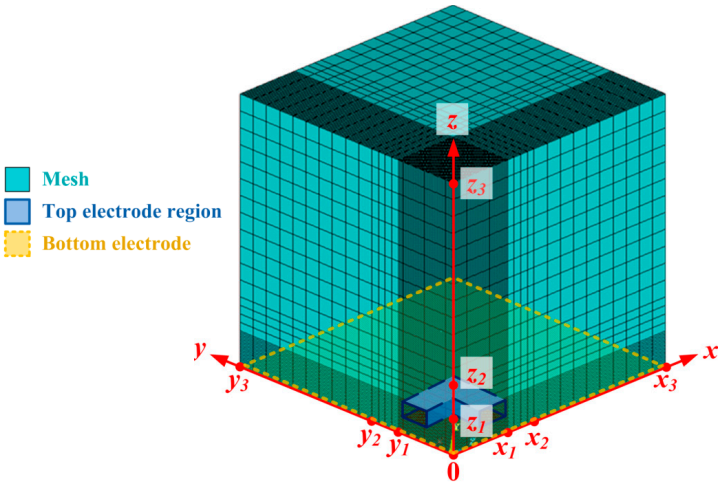

Figure 7. Scheme of the mesh size distribution.

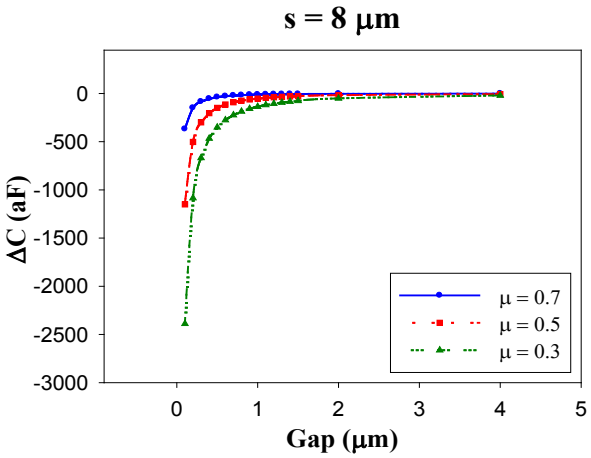

Figure 8. Simulation results of capacitance compensation term (s = 8 μm). ΔC: The capacitance compensation term of etching hole.

2.3. Empirical Formula

The authors had never applied the previous work [13] on real devices and found large deviation. By a real device experiment, we found that the ratio of hole-dimension to the gap between microstructure and ground (s^e/g) had a significant effect on the fringe capacitance and this effect was not considered in that work. Therefore, the main difference between the present work and [13] is including the term s^e/g into the empirical formula. For easy and quick estimating of the influence of etching holes on the entire capacitance of microstructures, this paper derives an empirical formula for the capacitance compensation term of etching hole. The empirical formula is obtained by curve fitting on the ANSYS simulation results. According to the capacitance analysis, the decreasing of parallel-plate capacitance and the increasing of fringe capacitance cause the capacitance compensation term. For the decreasing of the parallel-plate capacitance, it can be calculated by the ideal parallel-plate capacitance formula. On the other hand, for the increasing of the fringe capacitance, we introduce three dimensionless parameters, s^e/g, h/g and μ, to estimate the fringe capacitance. Therefore, the dimensionless functional form used to fit the ANSYS simulation results is:

$$\frac{\Delta C}{\varepsilon s} = -(1-\mu)(s^e/g) + \alpha(1-\mu)(s^e/g)^{\beta} + \gamma(1-\mu)^{1-\lambda}(h/g)^{\lambda} \quad (6)$$

where α, β, γ and λ are the constants to be defined by curve fitting. The first term on the right-hand side of Equation (6) accounts for the ideal parallel-plate capacitance and the remaining terms account for the fringe capacitance due to the side walls and the upper surface, respectively. Since Equation (6) is nonlinear, the authors adopt the nonlinear curve-fitting algorithm, "nonlinearmodelfit" commend and loop operation, of the technical computing software Mathematica. By curve fitting on a large number of ANSYS simulation results within the dimension ranges, $5 \leqslant s^e/g$, $0.25 \leqslant h/g \leqslant 10$ and $0.3 \leqslant \mu \leqslant 0.7$, the values of the optimized constants are $\alpha = 0.913$, $\beta = 0.557$, $\gamma = 0.465$ and $\lambda = 0.318$. Therefore, the dimensionless capacitance compensation term of etching hole that we propose is:

$$\frac{\Delta C}{\varepsilon s} = -(1-\mu)(s^e/g) + 0.913(1-\mu)(s^e/g)^{0.557} + 0.465(1-\mu)^{0.682}(h/g)^{0.318} \quad (7)$$

In the applicable ranges of s^e/g, h/g, and μ, the maximum deviation in capacitance between the empirical Formula (7) and the ANSYS simulation is within ±5% (Figure 9). The applicable geometrical range of this work is wider than that of [13] (Table 4).

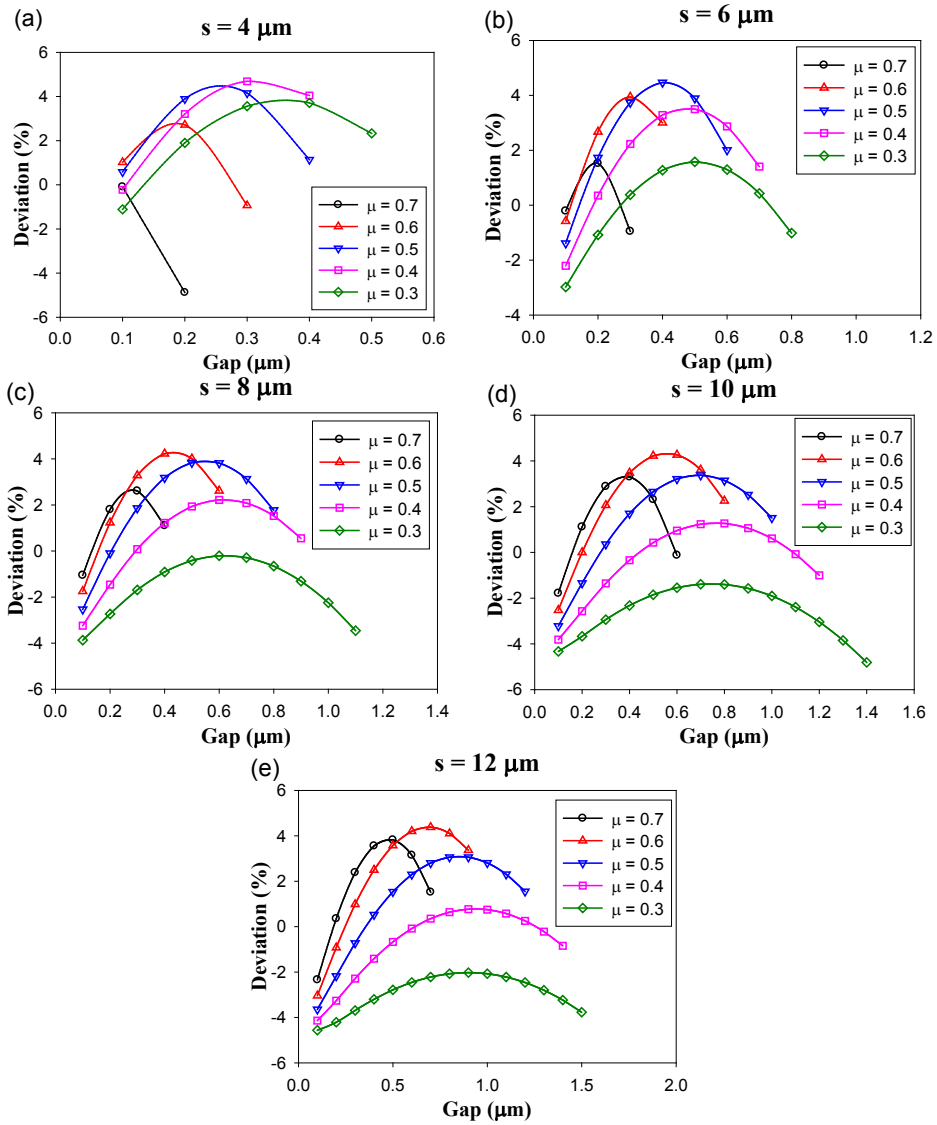

Figure 9. The deviations of the capacitance compensation term of etching hole in comparison with the simulations by the commercial software ANSYS, (**a**) s = 4 μm; (**b**) s = 6 μm; (**c**) s = 8 μm; (**d**) s = 10 μm and (**e**) s = 12 μm.

Table 4. The comparisons of the empirical formulas for the capacitance compensation term of etching hole in comparison with the simulation by the commercial software ANSYS.

Empirical Formula	Deviation	Geometrical Range
Equation (8) in [13]	±10%	$5 \leqslant s^e/g$, $0.25 \leqslant h/g \leqslant 5$ and $\mu = 0.7$
Equation (7) in this work	±5%	$5 \leqslant s^e/g$, $0.25 \leqslant h/g \leqslant 10$ and $0.3 \leqslant \mu \leqslant 0.7$

3. Experiment Verification

We make perforated micro-beams to demonstrate the application of the present capacitance compensation formula on determine their capacitance. Figure 10 shows the schematic of the test micro-beam. A series of micro-beams with different lengths, widths, and etching-hole sizes are manufactured by the MEMS process. Table 5 lists the dimensions of the test micro-beams. In total, there are nine test-chips containing 54 test-beams. By unit-module length, they are divided into three groups. Each group contains three chips and the three chips have three different ligament coefficients (μ). Each chip contains six beams (Figure 11). By width, they are divided into two groups; each group contains three beams with three different lengths.

To control the size of the test structure precisely, the authors adopt a low-resistance silicon-on-insulator (SOI) wafer to make the micro-beam. Table 6 details the specifications of the SOI wafer. The device layer forms the beam structure (thickness = 10 μm), which is patterned by induction coupling plasma etching. The buried oxide layer forms the anchor of the test structure and decides the gap between micro-beam and substrate (gap = 2 μm). After patterning the device layer, 49% Hydrogen Fluoride etchant is used to etch the silicon dioxide under the device layer and makes the micro-beam release. The scanning electron microscope picture (Figure 11) shows that the test beam with etching holes is completely suspended and without curl.

Table 5. Dimensions of the test micro-beams and unit modules. The beam thickness (h) is 10 μm and the gap (g) between the beam and ground is 2 μm.

Chip	Unit Module Dimensions		Beam Dimensions	
	Length s (μm)	Ligament Coefficient μ	Width b (μm)	Length L (μm)
1	80	0.7	400, 640	1920, 2880, 3840
2	80	0.5	400, 640	1920, 2880, 3840
3	80	0.3	400, 640	1920, 2880, 3840
4	100	0.7	400, 600	2000, 3000, 4000
5	100	0.5	400, 600	2000, 3000, 4000
6	100	0.3	400, 600	2000, 3000, 4000
7	120	0.7	360, 600	1920, 2880, 3840
8	120	0.5	360, 600	1920, 2880, 3840
9	120	0.3	360, 600	1920, 2880, 3840

Table 6. Specification of the silicon-on-insulator (SOI) wafer.

Diameter (mm)	Type/Dopant	Orient	Device Layer			BOX Layer (μm)	Handle Wafer		
			Thick (μm)	Resist (ohm-cm)	Finish		Thick (μm)	Resist (ohm-cm)	Finish
100 ± 0.1	P/B	<1-1-1>	10 ± 0.5	0.010–0.015	P	2	400 ± 10	0.010–0.015	P

P/B: Positive/Boron.

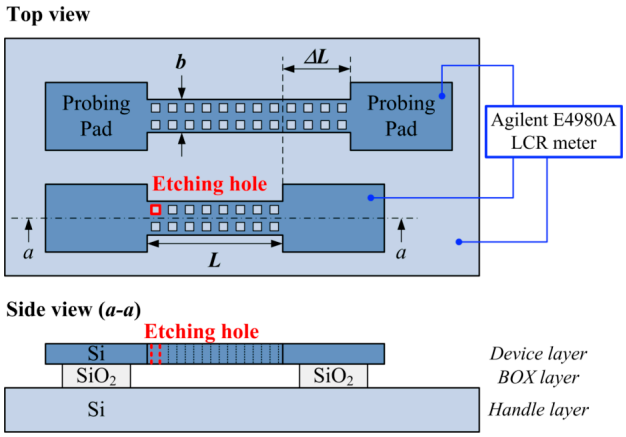

Figure 10. The schematic of test microstructures. L: length of the test beam.

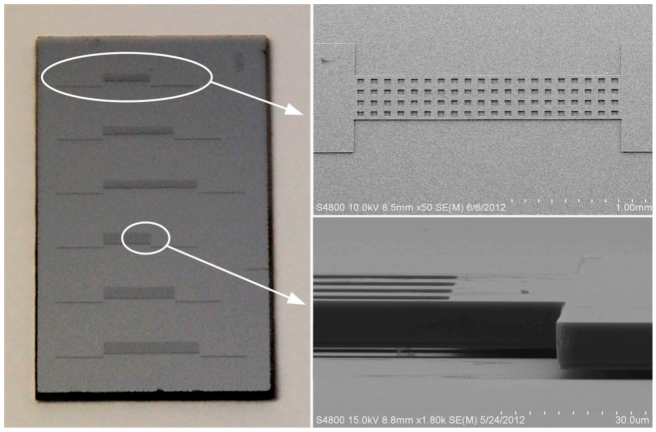

Figure 11. The scanning electron microscope picture of the test sample.

The capacitances of the test structures are measured by Agilent E4980A LCR meter (Agilent Technologies, Santa Clara, CA, USA) (Figure 10). To eliminate the fringe effects of the probing pads and anchors, two test beams with different lengths fabricated in the same chip are required. The capacitance difference ($C_{\Delta L}$) of the two beams is obtained by mutually subtract their capacitances measured by Agilent E4980A LCR meter. The experiment results are listed in the sixth column of Tables 7–9. The authors of this paper had published a two-dimensional capacitance formula for determining the capacitance of the micro-beam without etching hole [11], we can use that formula to calculate the capacitance difference of the present two test beams, that is:

$$C'_{\Delta L} = \varepsilon \Delta L \left[\frac{b}{g} - 1.06 + 3.31 \left(\frac{h}{g} \right)^{0.23} + 0.73 \left(\frac{b}{h} \right)^{0.23} \right] \tag{8}$$

where ΔL is the length difference of the two test beams. It should be mentioned here that Equation (8) does not consider the effects of etching holes. The results of Equation (8) are listed in the 6th column of Tables 7–9. For considering the effects of etching holes, we can add Equation (7) into Equation (8) to calculate the capacitance difference of the present two test beams, that is:

$$C_{\Delta L} = C'_{\Delta L} + N \Delta C \tag{9}$$

where ΔC is given by Equation (7) and N is the total number of etching holes. The results of Equation (9) are listed in the ninth column of Tables 7–9. Tables 7–9 compare the numerical results obtained

by experiment and empirical formula for the ligament coefficients μ = 0.7, 0.5 and 0.3, respectively. The smaller the ligament coefficient is, the larger the total area of the etching holes is. When the ligament coefficient μ is 0.7 (Table 7), the mean deviation between Equation (8) (neglecting the effect of etching hole) and experiment is 5.89%, while those of this work and the authors' previous work [13] are both about 3%. When the ligament coefficient μ is 0.5 (Table 8), the mean deviation of Equation (8) reaches to 24.40%, while those of this work and the authors' previous work [13] are about 4% and 3% respectively. When the ligament coefficient μ = 0.3 (Table 9), the most critical case in experiment and regular design, the deviation of Equation (8) reaches to 62.99%, while those of this work and the authors' previous work [13] are about 3% and 7%, respectively. This is because the larger etching holes cause a significant capacitance decrease, but Equation (8) neglects the effect of etching hole. Figure 12 summarizes Tables 7–9. According to the aforementioned results and comparisons, accompanied with the capacitance compensation term of this work, Equation (7), significantly improves the capacitance prediction of the microstructures with etching holes. The maximum deviation of the 54 test-beams compared with experiment is within 8%. The present capacitance compensation term of etching holes can provide the MEMS designers to estimate the capacitance of micro-devices with etching holes and predominate in the device characteristics.

Table 7. Comparisons of capacitance between experiment and formulae (μ = 0.7).

Chip	Dimension		Unit Module	Experiment (Average)	[11] [a]		[13] [b]		[This work] [c]	
	ΔL (μm)	b (μm)	s (μm)	$C_{\Delta L}$ (pF)	$C'_{\Delta L}$ (pF)	Deviation	$C_{\Delta L}$ (pF)	Deviation	$C_{\Delta L}$ (pF)	Deviation
1	960	400	80	1.712	1.746	2.00%	1.663	2.86%	1.654	3.38%
		640		2.514	2.768	10.11%	2.634	4.77%	2.621	4.25%
4	1000	400	100	1.697	1.819	7.21%	1.717	1.17%	1.716	1.11%
		600		2.637	2.706	2.60%	2.554	3.15%	2.551	3.28%
7	960	360	120	1.527	1.576	3.19%	1.480	3.08%	1.482	2.97%
		600		2.356	2.598	10.26%	2.438	3.48%	2.441	3.60%
Mean Deviation						5.89%		3.08%		3.10%

[a] $C'_{\Delta L}$ is given by Equation (8); [b] ΔC is given by the Equation (8) in [13]; [c] ΔC is given by Equation (7).

Table 8. Comparisons of capacitance between experiment and formulae (μ = 0.5).

Chip	Dimension		Unit Module	Experiment (Average)	[11] [a]		[13] [b]		[This Work] [c]	
	ΔL (μm)	b (μm)	s (μm)	$C_{\Delta L}$ (pF)	$C'_{\Delta L}$ (pF)	Deviation	$C_{\Delta L}$ (pF)	Deviation	$C_{\Delta L}$ (pF)	Deviation
2	960	400	80	1.423	1.746	22.70%	1.437	0.98%	1.445	1.51%
		640		2.437	2.768	13.55%	2.274	6.69%	2.285	6.24%
5	1000	400	100	1.509	1.819	20.52%	1.473	2.39%	1.490	1.25%
		600		2.136	2.706	26.68%	2.187	2.39%	2.213	3.61%
8	960	360	120	1.209	1.576	30.35%	1.263	4.47%	1.283	6.13%
		600		1.959	2.598	32.59%	1.972	0.66%	2.110	7.69%
Mean Deviation						24.40%		2.93%		4.40%

Table 9. Comparisons of capacitance between experiment and formulae (μ = 0.3).

Chip	Dimension		Unit Module	Experiment (Average)	[11] [a]		[13] [b]		[This Work] [c]	
	ΔL (μm)	b (μm)	s (μm)	$C_{\Delta L}$ (pF)	$C'_{\Delta L}$ (pF)	Deviation	$C_{\Delta L}$ (pF)	Deviation	$C_{\Delta L}$ (pF)	Deviation
3	960	400	80	1.067	1.746	63.68%	1.076	0.84%	1.113	4.31%
		640		1.744	2.768	58.74%	1.696	2.75%	1.754	0.62%
6	1000	400	100	1.156	1.819	57.35%	1.087	5.97%	1.137	1.66%
		600		1.625	2.706	66.46%	1.608	1.05%	1.683	3.51%
9	960	360	120	0.914	1.576	72.44%	0.842	7.88%	0.972	6.40%
		600		1.631	2.598	59.25%	1.294	20.66%	1.592	2.41%
Mean Deviation						62.99%		6.53%		3.15%

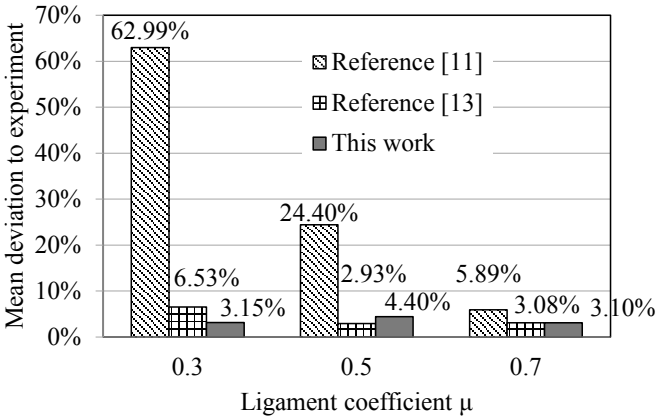

Figure 12. Comparisons of capacitance between experiment and formulae, summary of Tables 6–8.

4. Conclusions

This paper presents a capacitance compensation term applying to the estimation of the capacitance differences caused by the etching holes on capacitive micro devices. In the geometrical dimension range $5 \leqslant s^e/g$, $0.25 \leqslant h/g \leqslant 10$ and $0.3 \leqslant s^e/s \leqslant 0.7$, the deviation between the formula and ANSYS simulation is within 5%. Compared with the experiment, the capacitance evaluation is also very accurate (the maximum deviation is within 8%). The most significant benefits of the present formula are its simple form, wide applicable dimension range and high accuracy. With the existing literature, this empirical formula is able to provide designers with a criterion to evaluate the effects of etching holes on micro devices promptly and precisely.

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