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A 32 μm^2 MOS-Based Remote Sensing Temperature Sensor with 1.29 °C Inaccuracy for Thermal Management

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Abstract: This paper introduces a compact NMOS-based temperature sensor designed for precise thermal management in high-performance integrated circuits. Fabricated using the TSMC 180 nm process with a 1.8 V supply, this sensor employs a single diode-connected NMOS transistor, achieving a significant size reduction and improved voltage headroom. The sensor's area is 32 μm^2 per unit, enabling dense integration around thermal hotspots. A novel voltage calibration method ensures accurate temperature extraction. The measurement results demonstrate three-sigma errors within ±0.1 °C in the critical range of 75 °C to 95 °C and +1.29/−1.08 °C outside this range, confirming the sensor's high accuracy and suitability for advanced thermal management applications.

Keywords: complementary metal oxide semiconductor (CMOS) temperature sensor; smart sensor; thermal management; temperature calibration; remote sensing

1. Introduction

With the increasing complexity and density of integrated circuits (ICs), addressing the non-uniform heat distribution across the chip has become a crucial concern. Chips can exhibit significant thermal variations of up to 15 °C [1], requiring the strategic placement of thermal sensors near hotspots. The spatial locations of these hotspots shift according to different applications, making it impractical to rely on a single temperature sensor or a limited number of temperature sensors for comprehensive thermal management [2]. Consequently, a robust thermal management strategy requires the deployment of a large number of sensors across the chip to accurately monitor temperature variations.

For high-performance ICs like Central Processing Units (CPUs) and Dynamic Random-Access Memories (DRAMs), tens of temperature sensors are required for effective thermal monitoring, such as the sixty-three thermal sensors used in IBM's Power9 processor [3]. These sensors need to occupy minimal space to avoid interference with the protected circuit's functionality and to allow for the placement of multiple sensors in areas known as hotspots. To address the challenges of space and power consumption, several designs have been proposed to support remote sensing techniques [4–6]. These techniques involve placing the sensor's sensing elements near the hotspots while situating the sensor's core components in less area-constrained locations. Thermal-sensitive components, such as current sources, can be strategically located far from the hotspot locations to minimize the effects of thermal sensitivity. Multiple sensing elements can be distributed throughout the chip for thermal monitoring, resulting in a reduction in the area and power consumption per sensor.

The choice of sensing element plays a critical role in minimizing the space requirements. The sensing elements of most compact on-chip temperature sensors can be

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classified into three types: Bipolar Junction Transistors (BJTs) [7–11], resistors [12–14], and metal oxide semiconductor (MOS) transistors [1,15–19]. Resistor-based sensors often require larger silicon areas to maintain high accuracy due to the need for precise resistor values [12]. This limitation reduces their spatial efficiency in dense applications. BJT-based sensors have been preferred due to their dependable operation [20], with a single remote PNP device achieving a remarkable 20× reduction in the area of silicon compared to that in conventional full sensors [6]. However, MOS-based sensors emerge as the superior choice in terms of their spatial efficiency, boasting an approximately 15× decrease in size relative to comparable diode-based sensors, as introduced in [21], for the same fabrication process. Furthermore, the operational limitations of BJT sensors, particularly their base-emitter voltage requirement of around 0.7 V, present challenges for low-voltage applications. In contrast, MOS transistors demonstrate their ability to operate effectively at voltages below 1 V, offering a significant advantage in low-voltage operation. These advantages are especially beneficial in thermal management applications demanding the integration of multiple sensors per processing core, where space is at a premium and power efficiency is paramount.

Temperature sensors for thermal management require specific accuracy at throttling temperatures, distinct from those applicable across broader temperature ranges, to ensure optimal performance and reliability [20]. The Joint Electron Device Engineering Council (JEDEC) 21-C standard, represented by the blue line in Figure 1, establishes a thermal mask for the chip-level and board-level temperature sensors used in power and thermal management, specifying a maximum temperature error of ±1 °C within the 75 °C to 95 °C range [22]. However, the temperature variances commonly encountered during actual testing necessitate a level of precision beyond the standard guidelines. This work, signified by the orange line in Figure 1, commits to this temperature interval and advances the accuracy beyond the standard, targeting an optimal worst-case temperature error of ±0.1 °C within this critical range. Beyond this range, this work aims to maintain the standard accuracy of ±1 °C. This level of precision makes the sensor especially suited to integration across chips where precise thermal monitoring is crucial.

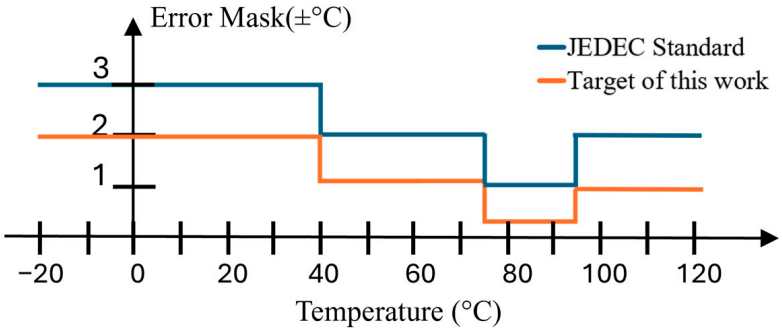

Figure 1. Thermal masks for temperature sensors of JEDEC 21-C Grade B Standard [22] and the target mask for this work.

Building upon these considerations, this work introduces a compact design for a MOS-based temperature sensor aiming to address the aforementioned challenges. The sensor unit consists of a small diode-connected N-channel MOS (NMOS) transistor, allowing for the distribution of multiple remote sensing elements across the chip. Compared to previous related publications [23,24], which utilized two series-connected NMOS transistors, this work employs a single diode-connected NMOS transistor as the sensing unit. This approach significantly improves the voltage headroom, thereby enhancing the sensor's performance in low-voltage applications. Fabricated using the Taiwan Semiconductor Manufacturing Company (TSMC) 180 nm technology, each sensor occupies only 32 μm^2, achieving an

approximately 7× reduction in size compared to previously reported sensing elements [20]. This design also incorporates a temperature measurement system that connects all of the remote sensing elements through current-forcing and voltage-sensing buses. This configuration eliminates the dependence on local analog power supplies and addresses voltage drop concerns. The system utilizes a combination of three different input currents and their corresponding output voltages measured across each sensor to mitigate the nonlinear mobility and lambda effects, thus enabling temperature sensing through the relationship between the MOS transistor's threshold voltage and temperature. This method significantly enhances the accuracy of the sensor. Additionally, this work details a novel method for temperature extraction, applied during the sensor's characterization and calibration phases, to ensure accurate temperature estimation.

The simulation results of the temperature sensor were previously published in [25]. In this work, multiple measurement setups were conducted to validate the design, showing that the maximum observed temperature error was approximately ±1 °C, spanning a temperature range from −10 °C to 100 °C. Notably, within the critical temperature range of 75 °C to 95 °C, which is of particular interest for thermal management applications, the maximum error recorded for these setups was approximately ±0.1 °C. These results underscore the sensor's capability to meet stringent accuracy requirements, aligning with the performance of state-of-the-art temperature sensors. Furthermore, the observed variance provides valuable insights into the sensor's reliability and accuracy across diverse operational scenarios, highlighting its potential for widespread application in precision thermal management systems.

2. Circuit Description

Figure 2 illustrates the architecture of our temperature measurement system, which is designed to distribute multiple temperature sensors across several cores. This system employs a single Temperature Measurement Controller (TMC) that is shared among all sensor units. The TMC serves as a stable current source, generating the required bias currents delivered to the sensors via a current-forcing I_{TMC} bus. In the proposed system, the TMC circuit is strategically excluded from the direct temperature monitoring of the hotspots, allowing for it to be installed to circumvent high-temperature areas. This flexibility in the TMC circuit's placement liberates it from strict constraints regarding its location and size. Positioned away from the hotspot areas, the TMC circuit's operational temperature is theoretically lower than the sensor temperature.

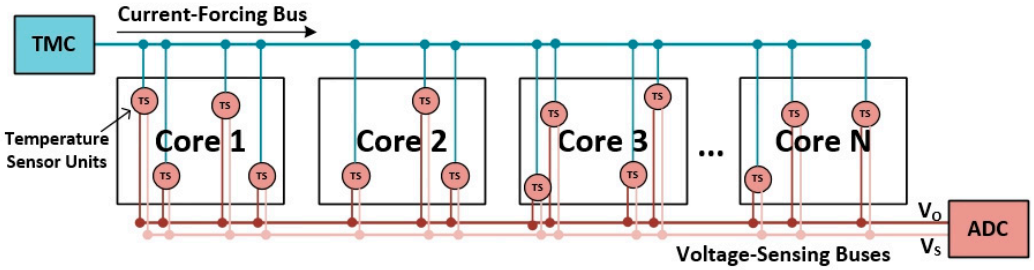

Figure 2. Temperature measurement system with distributed sensor units across multiple cores.

Each core contains several temperature sensor units strategically placed around the hotspots. Although only a few sensors are depicted in each core for clarity, the actual number of sensors can be much higher. This is due to the extremely compact design of the sensors, which allows for their dense placement around thermal hotspots. Two voltage-sensing buses connect the outputs of all of the sensor units, carrying the sensor data to an Analog-to-Digital Converter (ADC) for further processing.

Due to the current-based input of each sensor, no additional local analog power supply is required. Furthermore, the IR voltage drop issue in this system is alleviated because the I_{TMC} bus focuses solely on the current flow, and appropriate sizing of the sensors and switches effectively minimizes the leakage current of offline sensors along the sensing buses. With this setup, temperature information can be efficiently collected at different chip locations, and self-heating effects and power consumption can be mitigated. Additionally, the compact size of each sensor significantly enhances the feasibility of deploying multiple units within a constrained area of the chip. This enables the connection of dense sensor networks through the buses, optimizing the chip area without compromising its density. This design is particularly advantageous in scenarios requiring comprehensive thermal monitoring within dense chip areas.

Figure 3 provides a detailed schematic of the temperature sensing circuit. This work employs the Banba bandgap reference circuit [26] as the TMC, employing switches, SW_X and SW_Y, to generate two types of bias currents, I_X and I_Y, for the temperature sensor array. The sum of the two currents, I_{XY}, can be simply and accurately generated in the TMC without additional hardware costs. A single TMC circuit can supply input currents to numerous small-sized sensors via the dedicated current-forcing I_{TMC} bus.

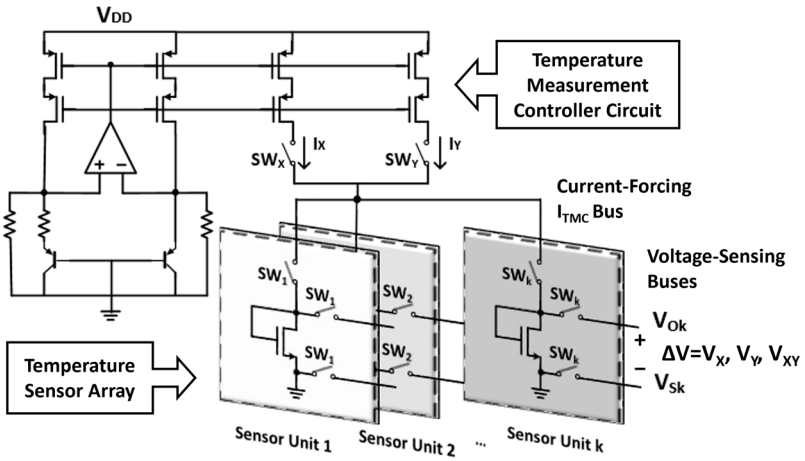

Figure 3. The schematic of the temperature sensing circuit with the Banba bandgap reference circuit as the Temperature Measurement Controller (TMC) circuit.

At the core of each sensor unit, shown within the dashed box, is a single diode-connected NMOS transistor. This compact element can be designed to be extremely small so that it can be distributed densely across the die. The V_O and V_S sensing buses allow for precise measurement of the drain-to-source voltage across this transistor, which carries information about the sensor's local temperature. To initiate a temperature measurement, three switches connected to the transistor are simultaneously triggered, ensuring accurate data from the specified sensor unit. The voltage differences between the V_O and V_S buses are measured to estimate the local temperature at the sensor's position. In alignment with the three TMC currents, the drain-to-source voltages are designated as V_X, V_Y, and V_{XY}. This work introduces an innovative methodology that combines multiple current inputs with their respective voltage outputs to derive enhanced accuracy in sensor temperature estimation. The details of this method will be explained in the subsequent section.

3. Derivation of the Temperature Formula

As shown in Figure 4, the proposed temperature sensor is a single diode connected NMOS transistor operating in the saturation region. To initiate the analysis, the square-law model [27] is employed to define the current flowing through the transistor when it is

subjected to bias currents at the TMC's operational temperature, T_{TMC}. The expression for the drain current I_X is formulated as follows:

$$I_X(T_{TMC}) = \frac{\mu(T) C_{OX} W}{2L} (V_X - V_{TH}(T))^2, \quad (1)$$

where

- I_X: Drain current of the NMOS transistor (μA);
- T_{TMC}: TMC's operational temperature (°C);
- T: Sensing unit's local temperature (°C);
- μ: Carrier mobility ($cm^2/V{\cdot}s$);
- C_{OX}: Oxide capacitance per unit area (F/cm^2);
- W and L: Width and length of the NMOS transistor (μm);
- V_{TH}: Threshold voltage of the NMOS transistor (V).

Correspondingly, the current I_Y, which is influenced by the current mirror gain M_{XY}, is expressed as follows:

$$I_Y(T_{TMC}) = M_{XY} \cdot I_X(T_{TMC}) = \frac{\mu(T) C_{OX} W}{2L} (V_Y - V_{TH}(T))^2, \quad (2)$$

where the carrier mobility μ and the threshold voltage V_{TH} are both dependent on the sensor temperature T. Considering that the switching frequency of the TMC current significantly exceeds the rate of the temperature change at the sensor, the temperature can be assumed to be invariant during the interval of the voltage measurements.

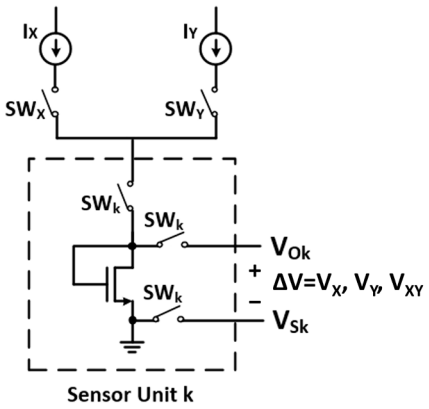

Figure 4. The schematic of the temperature sensor unit.

The analysis begins by assuming a linear relationship between the threshold voltage V_{TH} and the sensor temperature T, represented as follows:

$$V_{TH}(T) = V_{TH0} + \alpha \cdot T, \quad (3)$$

where V_{TH0} and α are model parameters that are dependent on the process and independent of temperature. This linear approximation is commonly used in MOS transistor modeling, such as in the BSIM4 model [28]. However, it is acknowledged that this linearity assumption oversimplifies the actual temperature dependence of V_{TH}. Nonlinearities, including higher-order effects, will be considered in the following analysis by incorporating additional terms into the temperature estimation model.

Combined with the previous current equations, the threshold voltage can be expressed in terms of the measured voltages V_X and V_Y as

$$V_{TH}(T) = \frac{\sqrt{M_{XY}}}{\sqrt{M_{XY}} - 1} V_X - \frac{1}{\sqrt{M_{XY}} - 1} V_Y. \quad (4)$$

Utilizing two distinct input currents for sensing helps to eliminate the nonlinear temperature dependence of mobility. Therefore, the sensor temperature derived from the threshold voltage takes the following form:

$$T = \frac{1}{\alpha}[-V_{TH0} + \frac{\sqrt{M_{XY}}}{\sqrt{M_{XY}}-1}V_X - \frac{1}{\sqrt{M_{XY}}-1}V_Y], \tag{5}$$

which indicates that the sensor temperature can be inferred linearly from the voltage measurements V_X and V_Y. The upcoming analysis will refine this model by incorporating terms that address nonlinearity, further enhancing the accuracy.

Given that M_{XY} is susceptible to local mismatches, process variations, and power supply variations at the TMC, substituting M_{XY} for an additional voltage measurement V_{XY} can potentially enhance the precision of the sensor's temperature estimation, without incurring additional hardware costs. Thus, the current mirror gain M_{XY} is reformulated by introducing V_{XY} to enhance the model's accuracy:

$$M_{XY} = \frac{(V_{XY} - V_{TH}(T))^2}{(V_X - V_{TH}(T))^2} - 1. \tag{6}$$

Substituting (6) into (5), the coefficients of V_X and V_Y can be expressed as linear functions of V_X and V_Y employing a first-order Taylor expansion approximation as

$$\frac{\sqrt{M_{XY}}}{\sqrt{M_{XY}}-1} \approx c_0 + c_1 V_X + c_2 V_{XY}, \tag{7}$$

$$\frac{-1}{\sqrt{M_{XY}}-1} \approx c_3 + c_4 V_X + c_5 V_{XY} \tag{8}$$

The resulting Equation (5) is thus reformulated into

$$T = a_0 + a_1 V_X + a_2 V_Y + a_3 V_X^2 + a_4 V_X V_Y + a_5 V_X V_{XY} + a_6 V_Y V_{XY}, \tag{9}$$

which is the combination of three voltage measurements at the sensor locations without information on the TMC's current and temperature.

Furthermore, it should be noted that both the sensor temperature formula and the current mirror gain, M_{XY}, can be alternatively expressed by

$$T = \frac{1}{\alpha}[-V_{TH0} + \frac{\sqrt{1+M_{XY}}}{\sqrt{1+M_{XY}}-1}V_X - \frac{1}{\sqrt{1+M_{XY}}-1}V_{XY}], \tag{10}$$

$$M_{XY} = \frac{(V_Y - V_{TH}(T))^2}{(V_X - V_{TH}(T))^2} - 1. \tag{11}$$

Similar to the previous analysis, the coefficients related to V_X and V_{XY} in Equation (10) are also represented as linear functions of V_X and V_Y through the application of a first-order Taylor series expansion. This results in an alternative expression of the sensor temperature as

$$T = b_0 + b_1 V_X + b_2 V_{XY} + b_3 V_X^2 + b_4 V_X V_Y + b_5 V_X V_{XY} + b_6 V_Y V_{XY}. \tag{12}$$

Taking the average of (9) and (12), the sensor temperature, represented by a combination of three voltage measurements, can be formulated as

$$T = c_0 + c_1 V_X + c_2 V_Y + c_3 V_{XY} + c_4 V_X^2 + c_5 V_X V_Y + c_6 V_X V_{XY} + c_7 V_Y V_{XY}. \tag{13}$$

By relying solely on these voltage measurements, the approach circumvents the variability introduced by TMC-specific factors, enhancing the robustness and applicability of the temperature estimation method. Consequently, the temperature formula depends only on sensor measurements, simplifying the integration of the sensor into various systems. Furthermore, the temperature formula represented in Equation (13), incorporating second-order terms, delivers a notable increase in accuracy compared to Equation (5), which contains only linear terms. A detailed comparison of these two models' accuracy based on simulation results was previously reported in [25]. This advanced formulation addresses and corrects the nonlinearities that were initially simplified during the analytical phase.

4. The Temperature Extraction Method

Variability in sensor outputs due to differences in their manufacturing and environmental conditions can significantly affect temperature accuracy. To address this, characterization and calibration are critical procedures that enhance sensors' reliability by aligning sensor outputs with known temperature standards. The proposed temperature extraction methodology employs a collaborative voltage calibration method. This approach involves generating a temperature model during the characterization phase and applies precise two-point calibration in production tests. Calibrating each sensor individually using two specific temperature points ensures enhanced accuracy. This mitigates discrepancies in the sensor outputs for the same temperature conditions, which are crucial to achieving high fidelity in temperature readings [29].

The characterization phase establishes a temperature model defining the coefficients necessary for accurate temperature estimation. This preliminary model forms the foundation for subsequent refinement through individual sensor calibration. The first step involves acquiring voltage outputs from a collection of sensors across several chips, designated as the training set. These outputs are recorded at a series of temperature points specifically chosen for the characterization process. The average voltage output is calculated, consolidating the responses of all of the sensors in the training set at each temperature point as

$$V_{AVG,Z}(T) = \frac{\sum_{k=1}^{N} V_{Z,S_k}(T)}{N}, \tag{14}$$

where k indexes the sensor units within the training set, N is the total count of the sensors in the set, and $Z \in \{X, Y, XY\}$ corresponds to the three voltage outputs for each sensor: V_X, V_Y, and V_{XY}. The averaged outputs will be utilized to determine the coefficients within the temperature model.

The next step involves the integration of the average voltage values, as determined from Equation (14), into the established temperature formula. For each selected temperature point, the voltages in the temperature Equation (13) are replaced with their corresponding V_{AVG} values. The coefficients for the temperature formula are then derived using linear regression. An initial model is established for accurate temperature estimation during characterization. It utilizes temperature sensors from the training set that capture process variations and local random mismatches. This approach guarantees that the model includes information from sensors across different wafers, thereby enhancing its robustness and adaptability under diverse operational conditions.

Following characterization, every sensor undergoes a calibration process to fine-tune the preliminary temperature model. The calibration is performed at two pivotal temperature points, T_1 and T_2. In this work, to ensure highly accurate thermal management within the critical temperature range of 75 °C to 95 °C, the individual calibration process specifically targets the two temperature points within this span: 80 °C as T_1 and 90 °C as T_2.

This ensures that the sensor provides the most precise readings where it is most necessary for effective thermal management.

Each sensor's outputs V_Z are calibrated against the average values $V_{AVG,Z}$ to determine the gain error α and the offset error β at the two temperature points from

$$V_{AVG,Z}(T_1, T_2) = \alpha_{Z,S_k} \cdot V_{Z,S_k}(T_1, T_2) + \beta_{Z,S_k}, \tag{15}$$

where $Z \in \{X, Y, XY\}$ corresponds to the three voltage outputs per sensor. The calculated offset errors and slope errors vary from sensor to sensor but stay the same from temperature to temperature for each sensor.

The calibrated voltages for the sensors at other temperature points are then calculated using

$$V_{CAL,Z,S_k}(T) = \alpha_{Z,S_k} \cdot V_{Z,S_k}(T) + \beta_{Z,S_k}, \tag{16}$$

where $V_{V,Sk}$ are the three measured voltages for each sensor.

These calibrated voltages are then applied to the temperature formula, utilizing the coefficients established during characterization. The resulting temperature model is then applied to each sensor for accurate temperature estimation as

$$\hat{T}_{CAL,S_k} = c_0 + c_1 V_{CAL,X,S_k} + c_2 V_{CAL,Y,S_k} + c_3 V_{CAL,XY,S_k} + c_4 V_{CAL,X,S_k}^2 + c_5 V_{CAL,X,S_k} V_{CAL,Y,S_k} + c_6 V_{CAL,X,S_{k3}} V_{CAL,XY,S_k} + c_7 V_{CAL,Y,S_{k3}} V_{CAL,XY,S_k} \tag{17}$$

The evaluation involves comparing the temperatures calculated from the sensors using Equation (17) with those obtained from high-precision instruments. Accuracy is assessed by the error given by

$$Error = T_{Actual} - \hat{T}_{CAL}, \tag{18}$$

where T_{Actual} is the temperature recorded by a precise resistance thermometer (CTR2000) in this work. The temperature error results for the proposed temperature sensor, vital for evaluating the overall effectiveness of the calibration process, will be discussed in detail in the following section.

5. Measurement Results

To validate the proposed temperature sensor technique on silicon, the sensor design was fabricated using the TSMC 180 nm process with a 1.8 V supply. A photograph of the fabricated chip is shown in Figure 5.

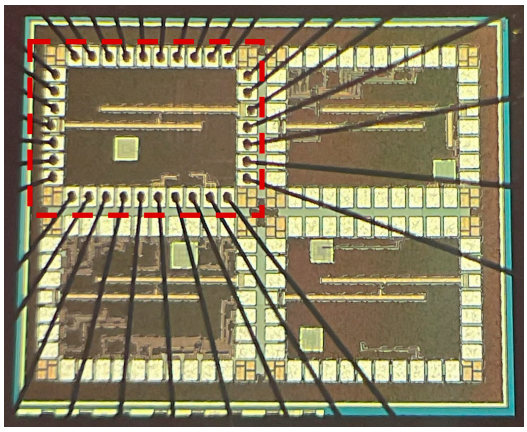

Figure 5. Photograph of the chip of the temperature measurement system (highlighted within the red dashed block).

Figure 6 presents a detailed layout of the temperature measurement system, highlighting the TMC circuit, an array of 36 temperature sensors, and shift registers that manage the selection of the currents and sensors. The temperature sensor array is organized into four

groups of nine sensor units, with varying distances between them to facilitate potential measurement of the temperature gradients across the chip in future studies. Consequently, the overall area of the system and sensor array includes these larger-distance gaps. The figure also emphasizes the compact design of the sensor unit, with dimensions of 3.8 µm by 8.2 µm, ensuring efficient use of the chip space.

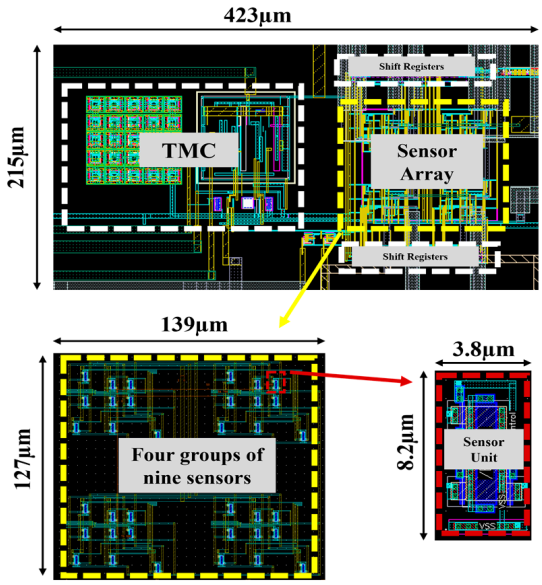

Figure 6. Layout of the temperature measurement system with distances between 36 sensor units.

As shown in Figure 7, this work utilized the Fluke 7103 oil bath to adjust the sensor temperatures from −10 °C to 100 °C, a range selected based on the oil's accuracy and cost considerations. To simulate the temperature variations between the TMC and the sensors, two PCBs were used: one serving as the TMC current source and the other hosting the sensors. These PCBs were placed in separate oil baths and connected via a current pin to the I_{TMC} bus of the two dies. Temperature estimations for the sensors were conducted through measurements on the sensor die. Each temperature stabilization phase in the oil baths took approximately 30 min, which was the most time-consuming aspect of the experimental process. To optimize the testing efficiency, all of the data necessary for characterization and calibration were collected within the same thermal run. Repeated measurements, with 40 repetitions for this work, were taken from each sensor to mitigate noise and enhance the data reliability; the average of these measurements forms the basis of the data processed. A precision resistance thermometer CTR2000 was inserted into the oil to measure the sensor temperatures.

Figure 7. Test instrument setup.

This work currently comprises three distinct measurement setups, designed to assess the sensor's performance under varying conditions:

5.1. Case 1: External Instrument Current Sources

To enhance efficiency and assess the functionality, this work initiated measurements by employing external instrument current sources set at 9 µA, 18 µA, and 27 µA to measure the sensors on five DUTs. Each sensor underwent 40 repeated measurements to average out the measurement noise, and the resulting average values were used for further data analysis. The sensors were tested across a broad temperature range from −10 °C to 100 °C, progressing in 10 °C increments and supplemented using additional temperature points that fell within our targeted operational range.

For this case, three of the five DUTs were selected as the training set, with the remaining two serving as the test set for verification purposes. Upon analyzing the temperature errors, it became apparent that the complex model described by Equation (13), which includes four second-order terms, tended to overfit the data. In response to this, this work explored simpler and more generalizable models. Notably, a refined version of the model that included one squared term for V_X and a single cross-product term combining the remaining two voltages exhibited significantly better accuracy and broader applicability. Consequently, the temperature estimation model was refined into

$$T = c_0 + c_1 V_X + c_2 V_Y + c_3 V_{XY} + c_4 V_X^2 + c_5 V_Y V_{XY} \tag{19}$$

Figure 8 illustrates the temperature error results of 180 sensors from five DUTs, calibrated at two temperatures, 80 °C and 90 °C, focusing on the critical thermal management range of 75 °C to 95 °C. The proposed temperature sensor achieves a worst-case inaccuracy of +0.05 °C/−0.06 °C within this range, meeting the target accuracy requirement of ±0.1 °C.

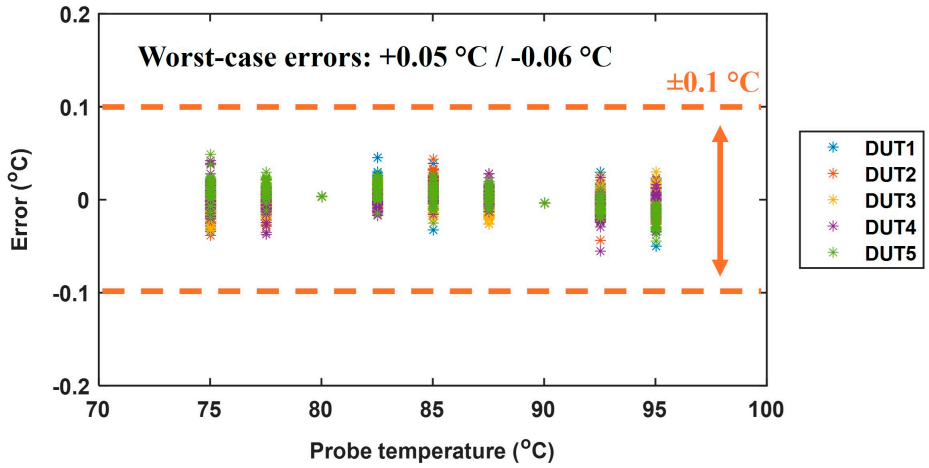

Figure 8. The temperature errors of 180 sensors on 5 DUTs with external instrument current sources after individual calibration at 80 °C and 90 °C.

5.2. Case 2: An Internal Current Source TMC

In this setup, the current for the sensors was sourced internally from the TMC on the same chip (denoted as DUT 6), ensuring that both the TMC and the sensors maintained the same temperature conditions. This setup involved a single DUT, with 24 sensors used as the training set and the remainder used as the test set for validation.

Figure 9 presents the relationship between the TMC currents and temperatures. The Banba bandgap circuit was untrimmed and designed to optimize the performance within the critical temperature range. Figure 10 provides the temperature error results for the 36 sensors on DUT 6, with the TMC on the same chip serving as the current source, as shown in Figure 9. Despite the untrimmed current source, the temperature sensors demonstrate

an impressive performance, with a worst-case inaccuracy of ±0.08 °C from 75 °C to 95 °C. These errors also satisfy the accuracy standards established for this work.

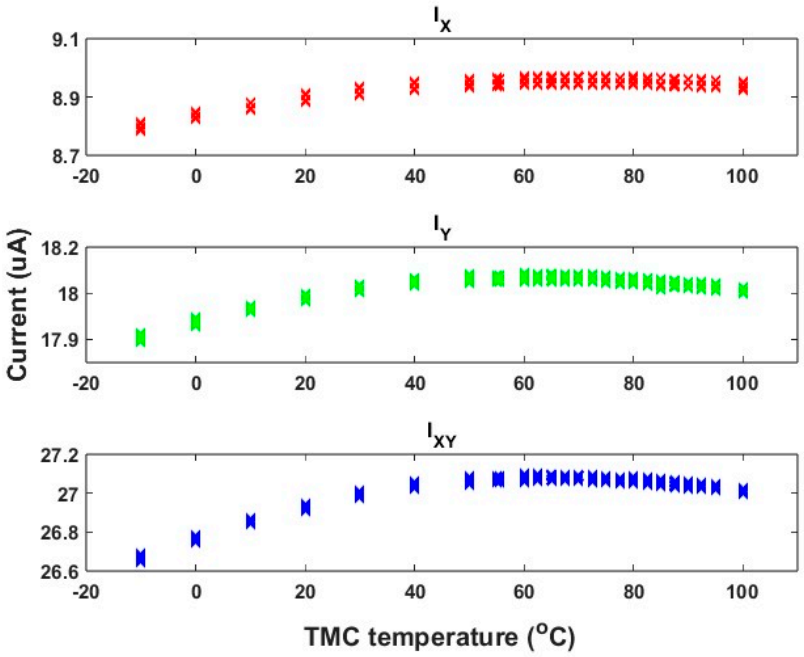

Figure 9. Relationship between TMC currents and temperatures.

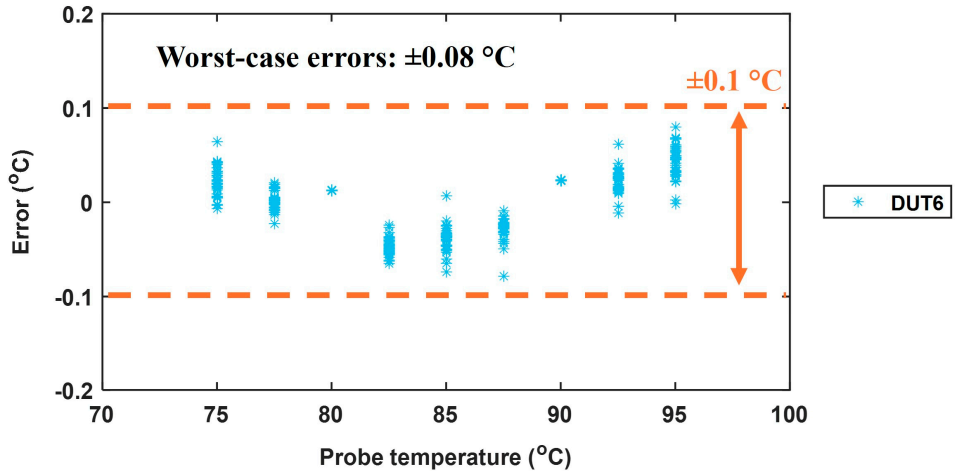

Figure 10. The temperature errors of 36 sensors on 1 DUT with the internal current source TMC on the same chip after individual calibration at 80 °C and 90 °C.

5.3. Case 3: An External Current Source TMC with Temperature Variations

In real applications, temperature sensors are often located around hotspots, which have higher temperatures than the large core, which is the TMC circuit in the work. Hence, case 3 was used to simulate different temperatures between the TMC circuit and the sensor arrays. Two DUTs were placed in two oil baths, with one provided for the TMC and the other for the sensors. The sensor temperatures, *Ts*, were set to match those of the previous setups. The temperatures in the TMC bath were selected to be approximately equal to *Ts* and *Ts*−20 °C at each sensor temperature point. The temperatures chosen for characterization should reflect varying TMC temperatures at each sensor temperature. Therefore, this case selected 12 temperatures for characterization, as detailed in Table 1. At each sensor temperature, two different TMC temperatures were considered to build the temperature model so that the model could consider temperature variations between the

core and the sensor arrays. The temperatures used for characterization were mainly located within the critical temperature range.

Table 1. Temperatures for characterization.

Ts (in °C)	T_{TMC} (in °C)	Ts (in °C)	T_{TMC} (in °C)
20	0	85	65
20	20	85	85
75	55	90	70
75	75	90	90
80	60	95	75
80	80	95	95

The temperature errors of the 180 sensors on five DUTs are illustrated in Figure 11. The TMC currents for these 5 DUTs were provided by DUT 6. The coefficients of the temperature formula were extracted from measurements from the three training set DUTs conducted at the twelve temperatures listed in Table 1. All the other sensors and measurements at different temperatures were used for verification. In case 3, the worst-case inaccuracy was +0.1 °C/−0.09 °C from 75 °C to 95 °C. Due to the consideration of the TMC temperature variations in case 3, there are nonzero errors at the two calibration points, unlike the previous two cases. While more measurement noise is involved due to the use of two separate oil baths and two separate test chips, the temperature measurement errors are only slightly worse compared to those in the previous two cases.

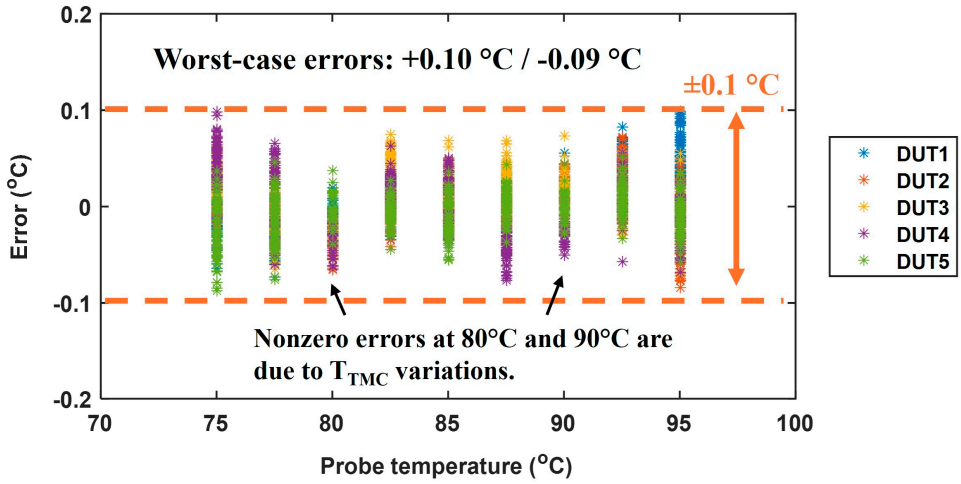

Figure 11. The temperature errors of 180 sensors on 5 DUTs with temperature differences between the TMC and sensors after individual calibration at 80 °C and 90 °C.

After analyzing the temperature errors for the three cases, it is essential to assess the overall performance using 3-sigma errors. Figures 12 and 13 provide a comprehensive view by combining the temperature errors in all cases. Figure 12 focuses on the critical temperature range of 75 °C to 95 °C, presenting the 3-sigma error lines for a detailed accuracy evaluation. The results show that the 3-sigma errors remain within ±0.1 °C, meeting the stringent accuracy requirements. This close grouping around the zero-error line highlights the sensors' exceptional precision within this range, which is vital for thermal management applications, such as data centers, where even minor temperature fluctuations can significantly impact performance and reliability.

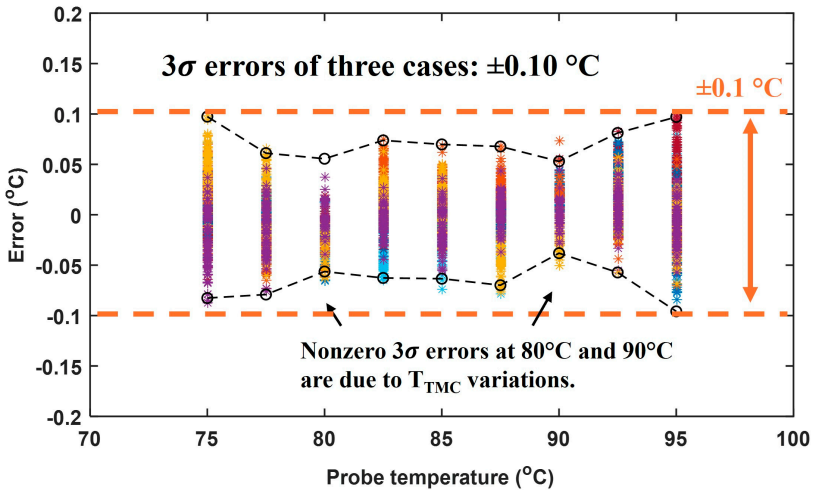

Figure 12. The temperature errors in three cases after individual calibration at 80 °C and 90 °C within the critical range of 75 °C to 95 °C.

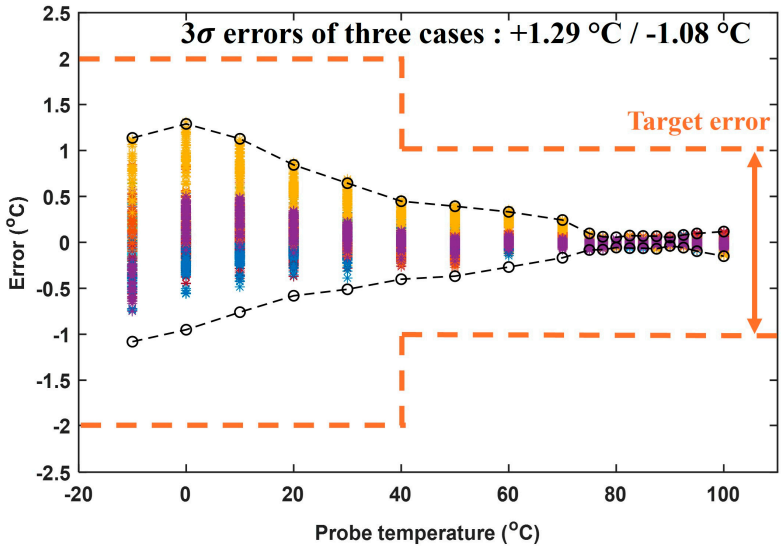

Figure 13. The temperature errors in three cases after individual calibration at 80 °C and 90 °C across the wider temperature range of −10 °C to 100 °C.

Figure 13 illustrates the temperature errors over a wider range from −10 °C to 100 °C, also including the 3-sigma error lines. The worst-case error outside the critical range is +1.3 °C/−0.75 °C, and the 3-sigma error is +1.29 °C/−1.08 °C. Although the focus of this work is on the critical range of 75 °C to 95 °C for temperature management applications, it is noteworthy that the sensors still exhibit competitive accuracy outside this range. As shown in Figure 1, the JEDEC standard has varying accuracy requirements over different temperature ranges, and our work follows this trend and significantly exceeds our target accuracy.

To further emphasize these results, Table 2 provides a comprehensive summary of the accuracy metrics achieved by the proposed sensor across both the critical range and the broader temperature range. The critical range of 75 °C to 95 °C is particularly important for thermal management applications in high-performance integrated circuits, as it encompasses throttling temperatures where precise monitoring and control are essential to maintain stability and prevent performance degradation. Uniform accuracy requirements across a wide temperature range often fail to deliver optimal performance for such applications, as they do not reflect the need for heightened precision at critical temperatures. By setting stricter accuracy targets for the critical range—such as ±1 °C in the JEDEC standard

and ±0.1 °C achieved in this work—while allowing for more relaxed requirements outside this interval, this design ensures exceptional accuracy where it is most crucial. At the same time, the sensor maintains a robust performance over the broader range, underscoring its versatility and practical adaptability for diverse thermal monitoring scenarios.

Table 2. Summary of accuracy performance.

Accuracy	Critical Range (75–95 °C)	Broad Range (−10–100 °C)
JEDEC standard accuracy	±1 °C	±3 °C
Worst-case error in this work	+0.1 °C/−0.09 °C	+1.3 °C/−0.75 °C
Three-sigma error in this work	±0.1 °C	+1.29 °C/−1.08 °C

In this section, the measurement results from the three distinct setups validate the efficacy and precision of the proposed temperature sensor. Each case, encompassing different operational conditions, demonstrated the sensor's robust performance. The worst-case errors across all setups were within ±0.1 °C in the critical range of 75 °C to 95 °C, with 3-sigma errors also within this range. This level of precision is crucial for applications requiring stringent thermal management. Table 3 presents a performance comparison between this work and state-of-the-art studies on compact temperature sensors used for thermal monitoring. While many prior works in the literature have focused on achieving accuracy in a broad temperature range, relatively few have explored the optimal accuracy over narrow ranges, such as the critical 75–95 °C range targeted in this work. As a result, direct comparisons of the accuracy within this critical range are challenging. Nevertheless, the accuracy of this work over the wider range of −10 °C to 100 °C remains highly competitive, with a 3-sigma error of +1.29 °C/−1.08 °C, aligning with or exceeding the performance of other works. Furthermore, the compactness of the sensing unit area is another key highlight of this work. Unlike most prior papers, which have primarily focused on the overall sensor system area, this work emphasizes a highly compact sensing unit design suitable for remote sensing applications, achieving an area of just 32 μm^2. Reference [6] is one of the few works to provide the sensing unit area, reporting 0.00021 mm^2, which achieved a remarkable 20X reduction in the area of silicon compared to that in conventional full sensors. However, the sensing unit area achieved in this work is approximately 7× smaller than that reported in [6], highlighting the superior spatial efficiency of the proposed design. It should be noted that the larger overall area (0.09 mm^2) in this work is primarily due to the inclusion of the TMC and the spacing between the 36 sensor units for the potential temperature gradient measurements, as shown in Figure 6. This highlights the design's scalability for applications requiring multiple sensors distributed across a chip. The compact sensing unit area of this work is particularly advantageous for dense thermal management applications, where space efficiency is paramount. In summary, this work uniquely balances high accuracy, spatial efficiency, and practical design considerations for thermal management applications. The exceptional accuracy achieved within the critical range and the competitive performance over the broader range, combined with the compact sensing unit area, underscore the significance of this work in advancing thermal management solutions for high-performance integrated circuits.

Table 3. Performance comparison with other works.

References	This Work		[1]	[6]		[10]	[30]
Process	180 nm		90 nm	FinFET 22 nm		65 nm	180 nm
Supply Voltage (V)	1.8		1.3	1		1.3	0.6
Sensor Type	MOS		MOS	PNP & MOS		PNP	MOS
Temperature Range (°C)	75~95	−10~100	20~130	−30~120		−10~110	0~100
Trim	2-pt		2-pt	1-pt	No	2-pt	2-pt
Inaccuracy (°C)	±0.1 (±3σ)	−1.08/1.29 (±3σ)	±0.5	±1.07 (±3σ)	±2.81 (±3σ)	±1.35 (±3σ)	−1.45/1.4
Area (mm^2)	0.09 **		0.00375	0.0043		0.003	0.021
Sensor Unit Area (mm^2)	0.000032 *			0.00021 *			

* Sensing element area when using the remote sensing technique. ** The circuit area includes the area for the TMC circuit, which is strategically situated away from the sensor array. Additionally, the sensor array consists of 36 sensor units, which are distributed with spacing between them.

6. Conclusions

This work presents a novel design and implementation of a compact NMOS-based temperature sensor aiming to address the challenges of accurate thermal management in high-performance integrated circuits. Fabricated using the TSMC 180 nm process with a 1.8 V supply, the proposed sensor exhibits significant advancements in terms of the size reduction and accuracy, making it highly suitable for dense integration around thermal hotspots. The design employs a single diode-connected NMOS transistor as the sensing element, offering improvements in voltage headroom compared to that in earlier designs that utilized series-connected NMOS transistors [23,24]. This simplification of the circuit architecture reduces the minimum voltage required for reliable operation, enhancing the sensor's compatibility with low-voltage IC applications. While this work focuses on temperature accuracy, the improved voltage margin ensures greater practicality for systems with stringent power supply constraints. Additionally, the sensor array, consisting of 36 units, demonstrates a highly compact design with an individual sensor area of 32 μm^2, allowing for the efficient use of chip space.

Additionally, this work introduces a voltage-calibrated temperature extraction method for precise temperature estimation. The measurement results from three distinct experimental setups validate the sensor's performance under various operational conditions. The three-sigma errors across all of the setups were within ±0.1 °C in the critical temperature range of 75 °C to 95 °C and within +1.29 °C/−1.08 °C (±3σ) outside this range. These results affirm the sensor's capability to meet the stringent accuracy requirements crucial for thermal management applications in data centers and other high-performance environments.

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