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Investigation of $1/f$ and Lorentzian Noise in TMAH-treated Normally-Off GaN MISFETs

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Abstract: A tetramethyl ammonium hydroxide (TMAH)-treated normally-off Gallium nitride (GaN) metal-insulator-semiconductor field-effect transistor (MISFET) was fabricated and characterized using low-frequency noise (LFN) measurements in order to find the conduction mechanism and analyze the trapping behavior into the gate insulator as well as the GaN buffer layer. At the on-state, the noise spectra in the fabricated GaN device were $1/f^\gamma$ properties with $\gamma \approx 1$, which is explained by correlated mobility fluctuations (CMF). On the other hand, the device exhibited Lorentzian or generation-recombination (g-r) noises at the off-state due to deep-level trapping/de-trapping into the GaN buffer layer. The trap time constants (τ_i) calculated from the g-r noises became longer when the drain voltage increased up to 5 V, which was attributed to deep-level traps rather than shallow traps. The severe drain lag was also investigated from pulsed I-V measurement, which is supported by the noise behavior observed at the off-state.

Keywords: GaN; MISFET; normally-off; $1/f$ noise; g-r noise; correlated mobility fluctuations; pulse measurement

1. Introduction

Gallium nitride (GaN) has been well developed as material for power electronics applications due to its wide band gap (3.4 eV) and two dimensional electron gas (2DEG) with large electron density of $\sim 10^{13} \text{ cm}^{-2}$ at the AlGaIn/GaN heterostructure. AlGaIn/GaN-based heterostructure field-effect transistors (HFETs) exhibit a normally-on operation due to the strong accumulation of high 2DEG density in the channel. To successfully achieve a normally-off mode, which plays an important role in applying power switching devices, a recessed-gate GaN metal-insulator-semiconductor (MIS) structure is required by adapting the removal of the AlGaIn layer under the gate region [1–5]. The recessed-gate GaN MISFET with a normally-off operation has several advantages: (i) easy control of the threshold voltage (V_{th}) by varying the recess etch depth, (ii) obtaining a normally-off operation by accomplishing a simple dry etching technique and (iii) achieving low gate leakage by depositing the gate dielectric [1,2]. However, etching damages and protrusions happening during the recess etching process affect the deteriorated device performance. It is necessary to apply tetramethyl ammonium hydroxide (TMAH) wet solution in the damaged GaN surface under the recessed-gate region in order to prevent plasma damage and smooth the surface of etched GaN channel layer [2]. Many researchers [2,3,6–9] have

reported enhancements of noise and device performance for the GaN-based devices by applying a TMAH treatment.

Noise source in a normally-off GaN MISFET stems from electron trapping/de-trapping into the interface of Al₂O₃/GaN and/or the buffer traps in the GaN buffer layer [10–12]. Low frequency noise (LFN) can analyze interface traps and also find buffer traps in GaN devices [10–14]. Fabricated GaN-based devices showed typical $1/f$ noise characteristics at the on-state (strong accumulation and subthreshold region), but Lorentzian or generation-recombination (g-r) noise at the off-state (deep-subthreshold region) [10,11]. Flicker noise, or $1/f$ noise, can be explained by two well-known models, one being the carrier number fluctuations (CNF) due to electron trapping/de-trapping from the channel into the gate insulator [15], and the being Hooge mobility fluctuations (HMF) due to fluctuations of electron mobility caused by phonon scattering [16]. On the other hand, g-r noise is originated by electron trapping/de-trapping into deep-level traps in the GaN buffer layer [10–12]. However, no detailed noise behaviors in a normally-off GaN MISFET have been investigated. We here report the $1/f$ noise characteristics at the on- and off-states to find the noise mechanism and investigate the traps in a normally-off GaN MISFET. Then, pulsed I-V measurements were conducted to observe current collapse behavior as well as to match with the noise results.

2. Materials and Methods

The AlGaIn/GaN heterostructure was grown on a sapphire (0001) substrate by metal organic chemical vapor deposition (MOCVD) by the following steps: (1) 2 μm -thick highly-resistive undoped GaN buffer layer, (2) 50 nm-thick undoped GaN channel layer and (3) 16 nm-thick AlGaIn barrier layer. In order to fabricate the recessed-gate GaN MISFET, the gate recess region was defined by photolithography and followed by inductively coupled plasma reactive ion etching (ICP-RIE). The gate region was then fully recessed by etching of a 16 nm-thick AlGaIn barrier layer and the additional overetching of a 20 nm-thick GaN channel layer. Then, wet etching in TMAH solution (5% solution at 90 °C for 60 min) was applied to remove etching damages and protrusions [2]. To make the device isolation, the mesa region was defined and then a 17 nm-thick atomic layer deposited (ALD) Al₂O₃ as a gate insulator was deposited. After ohmic contact hole opening, ohmic metal with a Si/Ti/Al/Ni/Au structure (1/25/160/40/100 nm) was deposited by an electron-beam evaporator and sequentially annealed by rapid thermal annealing at 800 °C for 30 sec in N₂ gas. Finally, the Ni/Al/Ni gate and pad metals were deposited. The schematic epitaxial and device structure with gate length (L_g) of 2 μm and width (W_g) of 50 μm are illustrated in Figure 1a. Cross-sectional transmission electron microscopy (TEM) (Thermo Fisher Scientific, Waltham, MA, USA) and energy-dispersive X-ray spectroscopy (EDX) (Thermo Fisher Scientific, Waltham, MA, USA) elemental mapping images clearly reveal that the fabricated device has the recessed GaN channel under the gate region, deposited with the ALD Al₂O₃ gate insulator and gate metal, as shown in Figure 1b,c.

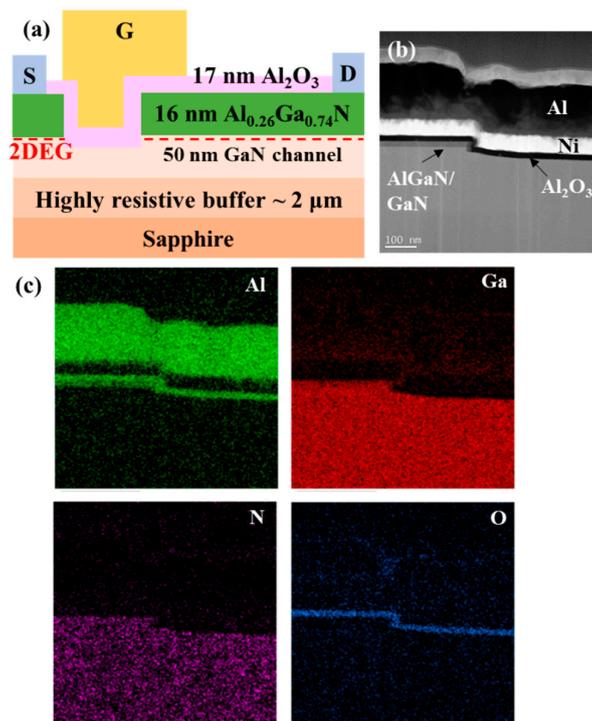


Figure 1. (a) Schematic illustration of a normally-off GaN metal-insulator-semiconductor field-effect transistor (MISFET) including epitaxial and device information. (b) Cross-sectional transmission electron microscopy (TEM) and (c) energy-dispersive X-ray spectroscopy (EDX) images of the recessed-gate GaN MIS structure. Elemental mapping of Al (green), GaN (red), N (purple), and O (blue) in the device structure obtained using the EDX machine.

3. Results and Discussion

Figure 2 shows the transfer and output curves of the fabricated GaN MISFET. The device successfully demonstrates a normally-off operation with a large threshold voltage (V_{th}) of around 3.5 V, which is preferred for power devices, as in the linear region ($V_d = 0.1$ V) of Figure 2a. The fully recessed gate region with etching depth of 36 nm is attributed to the enhanced V_{th} and the degraded on-current. The GaN buffer layer with relatively low resistance also deteriorates the off-state leakage current of the device, which leads to the reduced I_{ON}/I_{OFF} ratio. The I_{ON}/I_{OFF} ratio can be further improved by controlling the gate recess and/or increasing buffer resistance by doping deep-level impurities [17–19]. The gate voltage can sweep up to 10 V without degradation of the drain current, thanks to the high quality of the Al_2O_3 gate insulator. The output curves in Figure 2b present good cut-off and pinch-off properties with a small knee voltage of ~ 3 V.

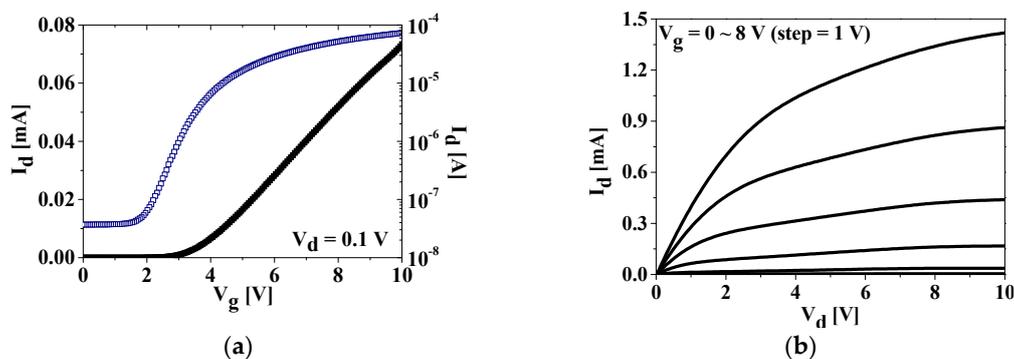


Figure 2. (a) Linear (filled black) and logarithmic (empty blue) scale of I_d versus V_g at $V_d = 0.1$ V and (b) I_d - V_d curves sweeping $V_d = 0 \sim 10$ V in the fabricated GaN MISFET.

LFN measurements were performed using a NOSISYS7 fully automatic noise analyzer (Synergie Concept) [20]. The drain current noise power spectral densities (S_{Id}) are plotted in the frequency ranges from 4 Hz to 10^4 Hz at $V_d = 0.1$ V and two representative gate biases: (i) $V_g = 2$ V (deep-subthreshold region) and (ii) $V_g = 10$ V (strong accumulation region) are shown in Figure 3a. At the on-state, LFNs clearly exhibit a $1/f^\gamma$ shape with $\gamma \approx 1$ from the subthreshold region ($V_g = 2.6$ V) to the strong accumulation region ($V_g = 10$ V). Similar $1/f$ noise curves were obtained for the LFN measured at V_g bias conditions of $2.6 \text{ V} \leq V_g \leq 10 \text{ V}$ (not presented in Figure 3a). The measured S_{Id} values increased at increased V_g , which was attributed to the increased drain current.

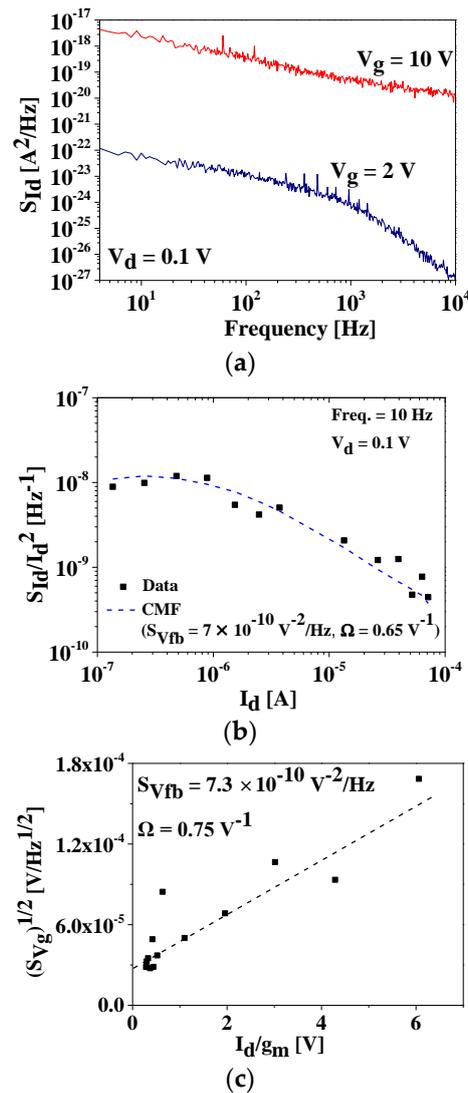


Figure 3. (a) Noise spectral density (S_{Id}) versus frequency at $V_g = 2$ V and 10 V. (b) Normalized S_{Id} (black square) versus I_d matching with the correlated mobility fluctuations (CMF) noise model and (c) variation of the gate voltage noise spectral density (S_{Vg})^{1/2} as a function of (I_d/g_m) in the fabricated GaN metal-insulator-semiconductor field-effect transistor (MISFET), measured at $V_d = 0.1$ V and $f = 10$ Hz. The dashed line in (b) indicates the fitting line.

The normalized S_{Id} (S_{Id}/I_d^2) values are displayed as a function of I_d at $f = 10$ Hz and $V_d = 0.1$ V, as shown in Figure 3b. If LFN follows the correlated mobility fluctuations (CMF) model, which is explained by the CNF noise model plus additional mobility fluctuations, S_{Id}/I_d^2 can be explained as follows [21,22],

$$\frac{S_{Id}}{I_d^2} = \left(\frac{g_m}{I_d}\right)^2 S_{Vfb} \left(1 + \Omega \frac{I_d}{g_m}\right)^2 \quad (1)$$

$$\text{with } S_{Vfb} = \frac{q^2 kT \lambda N_t}{WLC_{ox}^2 f} \quad (2)$$

where S_{Vfb} is the flat-band voltage spectral density, $\Omega = \alpha_{sc} \times \mu_{eff} \times C_{ox}$, is the correlated mobility fluctuation term, which includes that α_{sc} is the Coulomb scattering coefficient, μ_{eff} is the effective carrier mobility, C_{ox} is the gate dielectric capacitance per unit area, q is the electron charge, kT is the thermal energy, λ is the tunnel attenuation distance, N_t is the gate dielectric trap density, WL is the channel area and f is frequency. Considering values of $S_{Vfb} = 7 \times 10^{-10}$ V²/Hz and $\Omega = 0.65$ V⁻¹, S_{Id}/I_d^2 is perfectly matched with $(g_m/I_d)^2$ at the drain current level. It is obvious that the dominant LFN mechanism in the fabricated GaN MISFET is the CMF noise model. According to the Equation (2) with $\lambda = 0.11$ nm [12], the trap density of N_t is acquired as 2.1×10^{19} cm⁻³·eV⁻¹, which is a value one or two orders lower than those of the GaN junctionless FET (JLFET) [12] and the GaN nanowire gate-all-around (GAA) FET [23]. The reason for the decreased N_t in the fabricated GaN MISFET is that the improved quality of the GaN channel layer compared to the n-type doped GaN in GaN JLFET and the smart-cut GaN in GaN GAA FET [12,23].

To further clearly observe the CMF noise model, the gate voltage noise power spectral density, $(S_{Vg})^{1/2}$, is plotted using Equation (3) [24],

$$\sqrt{S_{Vg}} = \frac{S_{Id}}{g_m^2} = \sqrt{S_{Vfb}} \left(1 + \Omega \frac{I_d}{g_m}\right) \quad (3)$$

Figure 3c shows a good linear relationship, which means that the CMF model fits very well with the experimental noise data. From the curves of $(S_{Vg})^{1/2}$ measured at $V_d = 0.1$ V and $f = 10$ Hz, the S_{Vfb} and Ω can be determined from the intercept with the Y-axis and the slope between $(S_{Vg})^{1/2}$ and (I_d/g_m) , respectively. The corresponding S_{Vfb} and Ω values are extracted to be 7.3×10^{-10} V²/Hz and 0.75 V⁻¹, respectively, which are almost consistent with those values obtained in the curves of S_{I}/I_d^2 versus I_d of Figure 3b.

At the off-state (deep subthreshold region), the spectral deformation is clearly acquired, which is totally different from the noise characteristics at the on-state (Figure 3a). The noise spectra at the off-state are observed as $1/f$ noise at low frequency, but suddenly decrease with $1/f^2$ at higher frequency. Generally, the noise spectra consist of two noise sources: one is $1/f$ noise and the other is g-r noise, as in Equation (4) [24],

$$S_I = \frac{K_f}{f} + \sum_{i=0}^N \frac{A_i}{1 + \left(\frac{f}{f_{oi}}\right)^2} \text{ with } \tau_i = \frac{1}{2\pi f_{oi}} \quad (4)$$

where K_f is the coefficient of the $1/f$ noise component, A_i is the plateau value of the g-r component, f_{oi} is the cut-off frequency and τ_i is the trap time constant. To clearly attain the cutoff frequency, the product $S_I \times f$ is displayed according to the increased V_d from 0.1 V to 5 V in Figure 4a. The obtained g-r noise levels are increased at enhanced V_d , which is caused by the increased off-state leakage current. The fabricated GaN MISFET shows a f_{oi} of 700 Hz, which corresponds to a τ_i of 23 msec. Similar results were also obtained from the GaN JLFET with a partially covered-gate structure ($\tau_i = 50$ ms) [12]. The reason for this small trap time constant is that the proposed device exhibits much less trapping effects than that of the reference device [12]. According to the increased V_d up to 5 V, the estimated f_{oi} is attained at 500 Hz (the corresponding τ_i is 32 ms). This confirms that the trapping/detrapping process

in the GaN buffer layer becomes deeper according to the increased drain voltage. This tendency is coincident with the drain lag phenomenon, which is related to current collapse induced by bulk traps in the GaN buffer layer at high drain voltage.

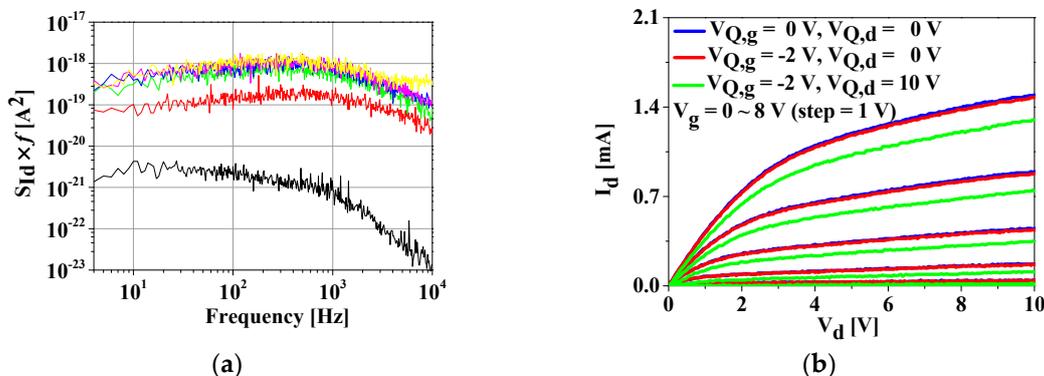


Figure 4. (a) Product $S_{Id} \times \text{frequency}$ as a function of frequency in the fabricated GaN MISFET varied $V_d = 0.1 \sim 5$ V. (b) Pulsed I_d - V_d curves for the device sweeping $V_d = 0 \sim 10$ V.

To check the drain lag of the proposed device, pulsed I-V measurements were conducted as in Figure 4b. The drain voltage is swept from 0 V to 10 V, varying $V_g = 0 \sim 8$ V with step of 1 V. The pulse conditions with pulse width of 1 ms are set at (1) $V_{g,Q} = V_{d,Q} = 0$ V, (2) $V_{g,Q} = -2$ V, $V_{d,Q} = 0$ V, and (3) $V_{g,Q} = -2$ V, $V_{d,Q} = 10$ V. To check the gate lag and drain lag, these pulsed I-V characteristics are compared. From the difference between curves (1) and (2), the fabricated device presents almost negligible gate lag due to the effective surface passivation of the high quality Al_2O_3 gate insulator. However, the severe drain lag from the difference between curves (2) and (3) is demonstrated in the fabricated device (Figure 4b). This is reflected by deep-trapping/de-trapping in the GaN buffer layer, which is well matched with the g-r noise implemented from the noise results at the off-state, as discussed earlier.

4. Conclusions

A normally-off GaN MISFET was investigated through DC, LFN, and pulsed I-V measurements. Normally-off operation with V_{th} of 3.5 V was successfully obtained in the fabricated device using a recessed-gate MIS structure. LFN clearly indicated $1/f$ noise behavior at the on-state, but Lorentzian characteristics at the deep-subthreshold region (off-state). The dominant channel mechanism in the proposed GaN MISFET is a CMF noise model, which was confirmed by both S_{Id}/I_d^2 versus I_d and $(S_{Vg})^{1/2}$ versus (I_d/g_m) curves. The τ_i calculated from f_{oi} measured at the off-state was 23 ms and increased to 32 ms at increased V_d , which clearly explains to the deep-trapping/de-trapping process in the GaN buffer layer. The drain lag observed from the pulsed I-V measurements was also well matched with that of the noise performances at the off-state.

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Conflicts of Interest: The authors declare no conflict of interest.

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