




Article

# High-Speed and High-Power 940 nm Flip-Chip VCSEL Array for LiDAR Application

Kuo-Bin Hong<sup>1,2</sup>, Wei-Ta Huang<sup>1</sup> , Hsin-Chan Chung<sup>3</sup>, Guan-Hao Chang<sup>1</sup>, Dong Yang<sup>1</sup>, Zhi-Kuang Lu<sup>1</sup>, Shou-Lung Chen<sup>3</sup>  and Hao-Chung Kuo<sup>1,2,\*</sup> 

<sup>1</sup> Department of Photonics, College of Electrical and Computer Engineering, National Yang Ming Chiao Tung University, Hsinchu 30010, Taiwan; mos2pss@gmail.com (K.-B.H.); aaronhuang.dop09g@nctu.edu.tw (W.-T.H.); jason860601@gmail.com (G.-H.C.); oemf54321@gmail.com (D.Y.); ld3107@gmail.com (Z.-K.L.)

<sup>2</sup> Semiconductor Research Center, Hon Hai Research Institute, Taipei 11492, Taiwan

<sup>3</sup> iReach Corporation, Hsinchu 30844, Taiwan; Eric\_Chung@ireachcorp.com (H.-C.C.); Scott\_Chen@ireachcorp.com (S.-L.C.)

\* Correspondence: hckuo@faculty.nctu.edu.tw; Tel.: +886-3-5712121 (ext. 56333)

**Abstract:** In this paper, we demonstrate the design and fabrication of a high-power, high-speed flip-chip vertical cavity surface emitting laser (VCSEL) for light detection and ranging (LiDAR) systems. The optoelectronic characteristics and modulation speeds of vertical and flip-chip VCSELs were investigated numerically and experimentally. The thermal transport properties of the two samples were also numerically investigated. The measured maximum output power, slope efficiency (SE) and power conversion efficiency (PCE) of a fabricated flip-chip VCSEL array operated at room-temperature were 6.2 W, 1.11 W/A and 46.1%, respectively. The measured L-I-V curves demonstrated that the flip-chip architecture offers better thermal characteristics than the conventional vertical structure, especially for high-temperature operation. The rise time of the flip-chip VCSEL array was 218.5 ps, and the architecture of the flip-chip VCSEL with tunnel junction was chosen to accommodate the application of long-range LiDAR. The calculated PCE of such a flip-chip VCSEL was further improved from 51% to 57.8%. The device design concept and forecasting laser characteristics are suitable for LiDAR systems.

**Keywords:** vertical cavity surface emitting laser; flip-chip; array; tunnel junction; light detection and ranging



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## 1. Introduction

The vertical cavity surface emitting laser (VCSEL) is considered to be a significant light source for sensing/imaging systems owing to its excellent beam quality [1], low threshold [2], low-energy consumption, low-cost [3], compact size and high reliability. Nowadays, commercial three-dimensional depth sensing applications are ubiquitous, such as for gestures [4], face recognition, autofocus [5] and eye movement tracking [6]. The spectral width of a surface-emitting laser beam is relatively narrow, and the temperature dependence of the wavelength is roughly 0.07 nm/K, which enables VCSELs to be competitive in 3D sensing [7,8]. This functionality allows VCSELs to be utilized with narrowband filters to filter out unwanted ambient signals [9], improve the signal-to-noise ratio (SNR), and increase the accuracy of outdoor sensing.

The majority of VCSEL arrays are almost entirely made up of vertical structures [10–12]. It is worth mentioning that when the VCSEL is operating at a higher injection current, the thick epitaxial substrate produces an enormous amount of heat and a drop in the PCE; additionally, earlier roll-over behaviors and a lower response speed have been observed [13].

Moreover, the conventional vertical device requires an increase in the height of the device to deal with the wire bonding process and this also increases the cost of the package.

A flip-chip like structure can reduce the cost of the sensor module because there is no need for wire bonding and the device is thinner and has less area. By removing wire bonding, the parasitic inductance and resistance of the device can be further reduced, thus improving the rise time [14]. This can provide superior depth resolution under high-frequency operation.

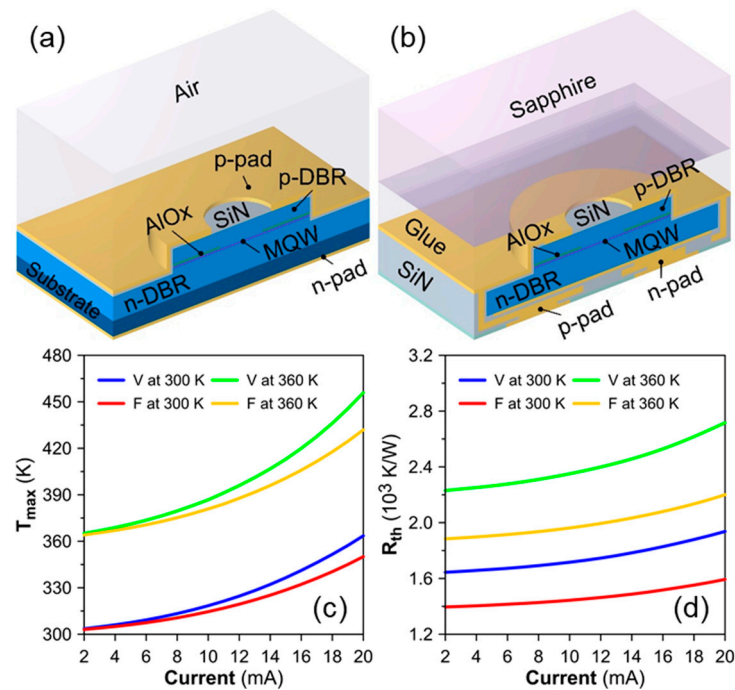
For thermal management challenges, a flip-chip like VCSEL has a high probability of providing greater heat dissipation [15,16], which is beneficial for improving the device's optoelectronic characteristics and response speed.

In this paper, we propose a flip-chip VCSEL with substrate removal and coplanar electrodes, which emits the light directly upward through the transparent sapphire substrate. First, we developed 3D simulation models to examine the thermal and optoelectronic properties of vertical and flip-chip VCSELs, such as the L-I-V curve and response speed. Then, the two kinds of VCSELs and their respective VCSEL arrays were fabricated. Finally, the laser characteristics were measured to verify the design concepts.

Furthermore, a single VCSEL's output power is relatively low for middle and long-distance LiDAR applications due to the small active volume compared to a laser diode and distributed feedback laser [17]. For middle and long-distance applications, the light power of a single VCSEL and VCSEL array must be increased. With regard to the design of a high-power VCSEL, we adopted the highly doped GaAs tunnel junction (TJ) to cascade the two pairs of active regions to numerically demonstrate the advantage of the GaAs TJ in power improvement.

## 2. Device Structure Design and Fabrication

The epitaxial p-i-n structure of a 940 nm VCSEL was composed of a 100  $\mu\text{m}$ -thick GaAs substrate, a distributed Bragg reflector (DBR) composed of 34 pairs of n-doped  $\text{Al}_{0.05}\text{Ga}_{0.95}\text{As}/\text{Al}_{0.95}\text{Ga}_{0.05}\text{As}$ , 3 pairs of multiple quantum wells (MQWs) with a 10 nm GaAs barrier and 8 nm InGaAs quantum well, followed by a DBR composed of 16 pairs of p-doped  $\text{Al}_{0.95}\text{Ga}_{0.05}\text{As}/\text{Al}_{0.05}\text{Ga}_{0.95}\text{As}$ . Then, a 10  $\mu\text{m}$   $\text{AlO}_x$  current aperture was placed at the antinode of the simulated vertical standing wave pattern. The fabrication process was as follows: a p-type ring-shaped metal contact is deposited through electron beam (E-beam) evaporation, and a p-side mesa was created by inductively coupled plasma-reactive ion etching (ICP-RIE). Then, the oxide aperture was formed by the wet oxidation process. After that, a 200 nm  $\text{SiN}_x$  passivation was deposited by plasma-enhanced chemical vapor deposition (PECVD) followed by the deposited of p-pad by E-beam. These steps were used for the vertical VCSEL and the preliminary process of the flip-chip VCSEL. Subsequently, the VCSEL wafer was bonded onto sapphire by adhesive glue, and the original GaAs substrate was removed by wet etching. Then, we used ICP-RIE and E-beam processes to etch an n-side mesa and deposit n-type metal, respectively. After that, PECVD was used to deposit the  $\text{SiN}_x$  insulating layer, metal connections and  $\text{SiN}_x$  passivation, which were deposited in sequence. Finally, the coplanar electrodes p-pad and n-pad were formed to complete the vertical (V) and flip-chip (F) VCSEL structures as shown in Figure 1a,b.



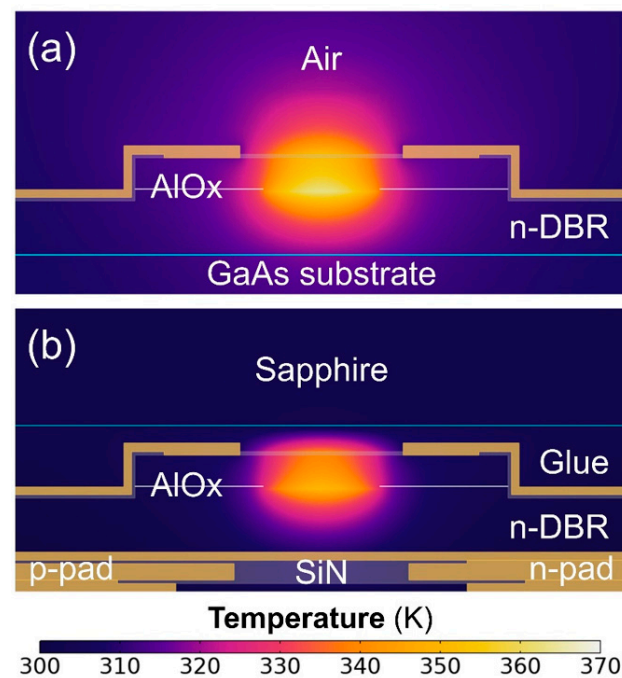
**Figure 1.** The schematics of 940 nm (a) vertical (V) and (b) flip-chip (F) VCSELs. (c,d) are the simulated junction temperature and thermal resistance for cases of vertical and flip-chip VCSELs. The ambient temperatures of 300 K and 360 K were considered.

### 3. Comparison of Vertical and Flip-Chip VCSEL

#### 3.1. Numerical Analysis

We used the commercial device simulation software, photonic integrated circuit simulator in 3D (PICS3D) to calculate the L-I-V curves and rise times of single vertical and flip-chip VCSELs. We also used COMSOL to explore the difference in thermal dissipation between vertical and flip-chip VCSEL structures. The heat sources used in the 3D VCSEL thermal model were taken from simulated L-I-V curves.

The calculated junction temperature ( $T_{max}$ ) and thermal resistance ( $R_{th}$ ) are shown in Figure 1c,d. Obviously, the current-dependent  $T_{max}$  and  $R_{th}$  of sample F at 300 K and 360 K are always lower than that of sample V, implying that the thermal dissipation ability of our proposed flip-chip VCSEL is beneficial for high-current operation, particularly for higher ambient temperatures. The fundamental reason is that the flip-chip VCSEL eliminates the thicker GaAs substrate, allowing heat generated in the active region to be dissipated more effectively through the bottom heat sink. Additionally, the simulated temperature distributions of samples V and F at a current injection of 20 mA and an ambient temperature of 300 K are shown in Figure 2. The thermal conductivities of GaAs-based semiconductors and sapphire used in the simulation model were referenced from previous research [18,19]. Moreover, the thermal conductivities of air and adhesive glue were considered as  $0.0255 \text{ W}/(\text{m}\cdot\text{K})$  and  $0.25 \text{ W}/(\text{m}\cdot\text{K})$ , respectively. Correspondingly, the simulated temperatures at the glue on the top surface of the VCSEL and n-DBR region of sample F are clearly lower than those of sample V. The thermal accumulation for a flip-chip VCSEL can be quickly mitigated, which can be attributed to the substrate removal and the relatively higher thermal conductivity of sapphire compared to air.



**Figure 2.** The simulated temperature distributions of (a) vertical and (b) flip-chip VCSELs at an ambient temperature of 300 K.

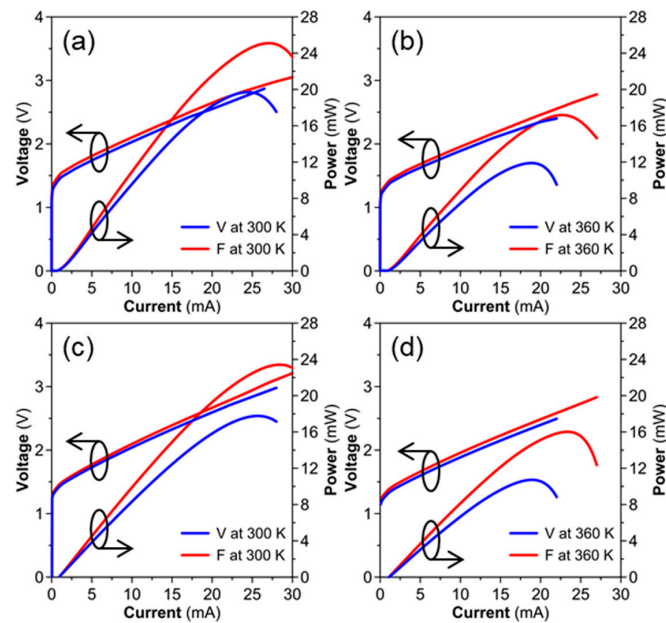
### 3.2. L-I-V Characteristics

On the other hand, the simulated L-I-V curves of vertical and flip-chip 940 nm VCSELs at 300 K and 360 K are shown in Figure 3a,b. We can observe that the flip-chip VCSEL with the GaAs substrate removal process has a higher slope efficiency (SE) and a larger roll-over current at 300 K and 360 K. This improvement can be attributed to the enhanced thermal dissipation of the flip-chip VCSEL. In addition, the carriers will escape from MQW when the injected current increases due to the increase in kinetic energy of carriers as the temperature rises [20–22]. As a result of this effect, slope efficiency and output power will be reduced. However, it can be seen that both vertical and flip-chip VCSELs require a higher current to reach the threshold when the ambient temperature reaches 360 K. This is because the increase in temperature will reduce the gain of the material. The QWs must receive a higher current to provide sufficient gain to overcome the loss and reach the threshold condition [23]. The better thermal dissipation of the flip-chip VCSEL can reduce the rise of the threshold current.

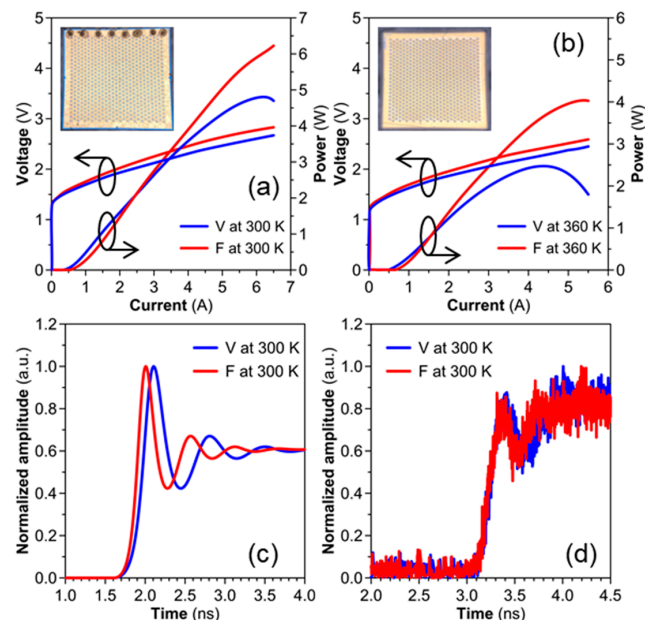
Figure 3c,d show the measured L-I-V curves of fabricated vertical and flip-chip VCSELs with continuous wave (CW) operation. The slope efficiency and power conversion efficiency (PCE) of the vertical VCSEL array are 0.93 W/A and 44%, and in the case of the flip-chip VCSEL array, these two efficiencies are 1.12 W/A, and 49%, respectively. The measurements obviously indicate that although the power characteristics are slightly smaller than the numerical simulation, the trend in the comparison between the vertical and the flip-chip VCSELs is consistent with the simulation results. The flip-chip VCSEL exhibits better heat dissipation and also achieves better SE, PCE, and roll-over current by removing the thick GaAs substrate.

In order to realize higher output power for LiDAR applications, vertical and flip-chip VCSEL arrays were fabricated. Figure 4a,b express the measured L-I-V curves of fabricated vertical and flip-chip VCSEL arrays under CW operation. The number of VCSEL arrays is 621 with a length of 1075  $\mu\text{m}$  and a width of 1060  $\mu\text{m}$ . The maximum output powers (SE, PCE) of the vertical and flip-chip VCSEL arrays operated at 300 K are 4.73 W (0.91 W/A, 41.3%), and 6.2 W (1.11 W/A, 46.1%), respectively. Additionally, under the operating current of 5.5 A, there are 61% and 27% reductions in output power between 300 K and 360 K for vertical and flip-chip VCSEL arrays, respectively. This proves that the flip-chip

VCSEL array possesses significantly better electrical and optical properties than the vertical VCSEL array. Moreover, the small discrepancy between the simulated and measured results is due to the thermal crosstalk effect [24]. Flip-chip VCSEL arrays can be operated at a larger current regardless of whether at room temperature or high temperature.



**Figure 3.** The light–current characteristics for simulation of vertical and flip-chip VCSELs at (a) 300 K and at (b) 360 K. (c,d) are the measured L-I-V characteristics for two kinds of fabricated VCSELs under CW operation at 300 K and 360 K. The arrows in the figures are indicated as the groups of I-V and L-I curves.



**Figure 4.** The measured L-I-V characteristics of vertical and flip-chip VCSEL arrays under CW operation at (a) 300 K and at (b) 360 K. The insets in (a,b) show the optical microscope images of vertical and flip-chip VCSEL arrays, respectively. (c) Simulated and (d) measured modulation responses of vertical and flip-chip VCSELs at 300 K. The arrows in the figures are indicated as the groups of I-V and L-I curves.



### 3.3. Modulation Response

The resolution of LiDAR imaging depends on the light modulation speed and contrast of the device [25]. The excellent thermal dissipation of the flip-chip VCSEL makes it more competitive in high-power applications because it reduces unnecessary losses caused by heat, and even enhances the modulation response speed.

To calculate the modulation response of VCSEL, the built-in temperature-dependent optoelectronic parameters including carrier recombination (radiative and Auger), valence band absorption, QW gain coefficient and refractive index were considered. The simulated modulation responses of samples V and F are shown in Figure 4c. It can be seen that there is a significant difference in modulation response between the two samples. The calculated rise times for samples V and F are 175 ps and 142 ps, respectively. The intrinsic modulation response of the VCSEL is related to internal quantum efficiency and differential gain [26]. The heat generation will cause carrier overflow, thus lowering the internal quantum efficiency and differential gain in D factor [27], and resulting in decreasing modulation speed. Therefore, the thermal dissipation characteristics of the flip-chip VCSEL not only increase the SE, PCE and roll-over current, but also improve the modulation response.

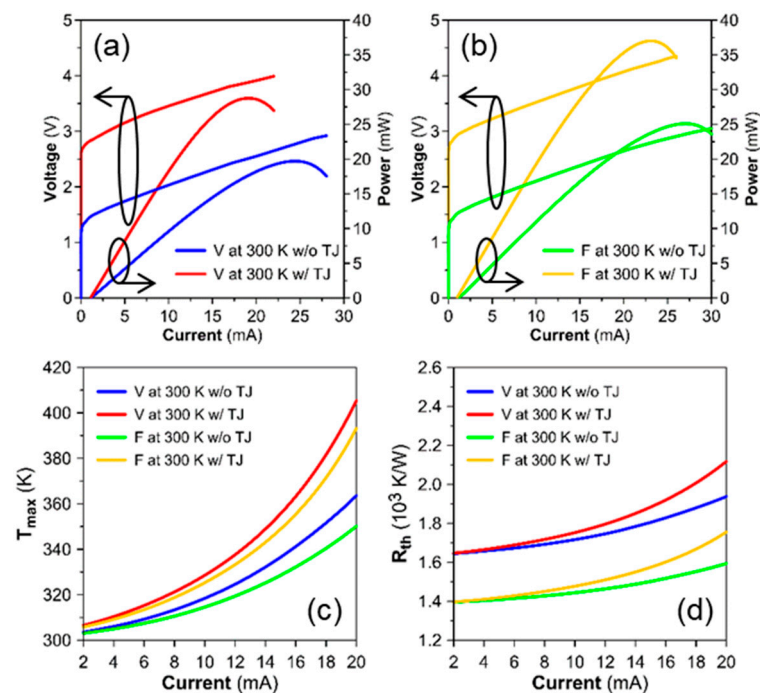
To measure the dynamic characteristics, we used the bias tee and the network analyzer to modulate vertical and flip-chip VCSEL arrays as well as measure the rise times when the bias current was set to 1.3 times the threshold current. The full width at half maximum (FWHM) bandwidths of the signals for two VCSEL arrays were all 1.997 ns, and the signal amplitudes of the vertical and flip-chip VCSEL arrays were 1.725 mV and 1.65 mV, respectively. The normalized modulation responses are plotted in Figure 5d and the measured rise times of the vertical and flip-chip VCSEL arrays were 237.2 ps and 218.5 ps, respectively, under 500 MHz modulation. It is again clearly demonstrated that the flip-chip VCSEL array can obtain a faster rise time due to better thermal dissipation and less parasitic impedance, making it suitable for the development of high-speed and high-power LiDAR.

## 4. Simulation of VCSEL with Tunnel Junction

In order to increase the output power, we applied a high doped GaAs TJ to cascade the two active regions and we analyzed the L-I-V and thermal characteristics of vertical and flip-chip VCSELs.

Figure 5a,b display the simulated L-I-V curves of samples V and F with a GaAs TJ at 300 K. Consequently, the maximum output powers (PCE) of these two samples with GaAs TJ increased from 19.2 mW (46%) and 23.3 mW (51%) to 28.6 mW (53.2%) and 37.1 mW (57.8%), respectively. The use of the tunnel junction will increase the output power; however, this will also slightly increase the junction temperature and accelerate the roll-over current for operating at higher current injection.

Similar to Figure 1c,d, the simulated current-dependent  $T_{\max}$  and  $R_{\text{th}}$  for two samples with a highly doped GaAs TJ are shown in Figure 5c,d, and as a result, the calculated  $T_{\max}$  ( $R_{\text{th}}$ ) for vertical and flip-chip VCSELs operated at 20 mA were 405.8 K (2110 K/W) and 392.1 K (1930 K/W), respectively. Compared to the vertical type, the flip-chip VCSEL with TJ can still maintain better thermal characteristics and it appears that sample F with GaAs TJ is preferable for long-range LiDAR application.



**Figure 5.** The simulated L-I-V characteristics of (a) vertical and (b) flip-chip VCSELs with highly doped GaAs TJ at 300 K. (c,d) are the simulated junction temperatures and thermal resistances for the two samples of interest. The arrows in the figures are indicated as the groups of I-V and L-I curves.

## 5. Conclusions

In this paper, we have numerically and experimentally investigated the thermal and optoelectronic characteristics of vertical and flip-chip VCSELs and the pertinent VCSEL arrays. A 3D VCSEL thermal model based on commercial FEM software was used to analyze the temperature distribution caused by a three-dimensional heat source. Calculated results indicated that the flip-chip VCSEL has superior heat dissipation. The additional improvement in the output power, SE and PCE were achieved by using the GaAs substrate removal technique. Due to the excellent thermal dissipation of our proposed flip-chip VCSEL, as expected, the measured output power, SE and PCE of the flip-chip VCSEL array under CW operation can reach 6.2 W, 1.11 W/A and 46.1%, respectively. In addition, the measured rise time of the flip-chip VCSEL can be reduced from 237.2 ps to 218.5 ps at a small current. In order to further enhance the device characteristics, a simulation model for a single VCSEL incorporated with highly doped GaAs TJ was constructed. The numerical results revealed that the calculated output power and PCE for the proposed flip-chip VCSEL with a GaAs TJ structure increased from 23.3 mW to 37.1 mW and 51% to 57.8%, respectively. The overall results suggest that the high-power and high-speed laser device composed of the array of the proposed flip-chip VCSEL with GaAs TJ can be fully applied for long-range LiDAR applications.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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