

## Article

# A Stable and Efficient Pt/n-Type Ge Schottky Contact That Uses Low-Cost Carbon Paste Interlayers

Pei-Te Lin<sup>1</sup>, Jia-Wei Chang<sup>2</sup>, Syuan-Ruei Chang<sup>2</sup>, Zhong-Kai Li<sup>2</sup>, Wei-Zhi Chen<sup>2</sup>, Jui-Hsuan Huang<sup>2</sup>, Yu-Zhen Ji<sup>2</sup>, Wen-Jeng Hsueh<sup>1,\*</sup> and Chun-Ying Huang<sup>2,\*</sup>

<sup>1</sup> Photonics Group, Department of Engineering Science and Ocean Engineering, National Taiwan University, Taipei 10660, Taiwan; d09525014@ntu.edu.tw

<sup>2</sup> Department of Applied Materials and Optoelectronic Engineering, National Chi Nan University, Nantou 54561, Taiwan; james96068xd@gmail.com (J.-W.C.); s108328001@mail1.ncnu.edu.tw (S.-R.C.); s108328018@mail1.ncnu.edu.tw (Z.-K.L.); s108328036@mail1.ncnu.edu.tw (W.-Z.C.); g37833855@gmail.com (J.-H.H.); s108328031@mail1.ncnu.edu.tw (Y.-Z.J.)

\* Correspondence: hsuehwj@ntu.edu.tw (W.-J.H.); cyhuang0103@ncnu.edu.tw (C.-Y.H.)

**Abstract:** Ge-based Schottky diodes find applications in high-speed devices. However, Fermi-level pinning is a major issue for the development of Ge-based diodes. This study fabricates a Pt/carbon paste (CP)/Ge Schottky diode using low-cost CP as an interlayer. The Schottky barrier height ( $\Phi_B$ ) is 0.65 eV for Pt/CP/n-Ge, which is a higher value than the value of 0.57 eV for conventional Pt/n-Ge. This demonstrates that the CP interlayer has a significant effect. The relevant junction mechanisms are illustrated using feasible energy level band diagrams. This strategy results in greater stability and enables a device to operate for more than 500 h under ambient conditions. This method realizes a highly stable Schottky contact for n-type Ge, which is an essential element of Ge-based high-speed electronics.

**Keywords:** carbon paste; n-type Ge; Schottky diodes; interlayer



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## 1. Introduction

Complementary metal oxide semiconductor (CMOS) technology is still the most common form of semiconductor device fabrication, which is capable of manufacturing sub-10 nm nodes using a traditional Si metal-oxide-semiconductor-field-effect-transistor (MOSFET) [1,2]. High-mobility channels are an effective booster. Germanium (Ge) is a possible alternative for Si for future high-speed applications because it features a high carrier mobility [3–5]. A good Schottky contact is an essential block for electronic circuits and devices. Generally, Ge-based Schottky diodes are affected by strong Fermi-level pinning [6,7]. Many studies try to modulate the Schottky barrier heights of metal/Ge junctions by inserting a thin insulator as an interfacial layer to minimize the effect of Fermi-level pinning [8–10]. Similarly, organic semiconductors that are used as the interfacial layer modify interface electronic states so the Schottky barrier height of the metal/Ge junction is decreased [11–13]. Recently, polymer poly (3,4-ethylenedioxythiophene)/poly (styrenesulfonate) (PEDOT/PSS) has been used for Schottky diodes as an interlayer, because it features high conductivity, solution processing capability, and is low-cost [14]. A. A. Kumar et al. demonstrated that using PEDOT/PSS as an interlayer for Pt/n-type Ge Schottky junctions increases the Schottky barrier height [13]. However, the semiconductor/PEDOT interface suffers from poor ambient stability because the hygroscopic nature of PSS means that water is absorbed, so it has a relatively weak tolerance to water [15]. Therefore, this obstacle limits its real application as an interlayer for high-speed Schottky diode.

Carbon is a cheap and accessible element on Earth [16]. Commercially available carbon paste (CP) is a low-cost electrical conductive printing ink with high conductivity and stability [16]. It contains conductive carbon particles and thermoplastic resins [17]. The

CP films are easily deposited using low temperature printing deposition processes, such as spin-coating, doctor-blading, inkjet-printing, and drop-casting [17,18]. The CP film is not easily oxidized after the sintering process, so it is resistant to high-temperature resistance and corrosion and is not subject to thermal shock [17,18]. Low-cost CP is widely found in applications in industry [17]. However, there are few related studies reporting a Schottky diode with a CP interlayer.

This study reports the fabrication of Pt/CP/n-Ge Schottky diodes. A low-cost CP is used as an interlayer to modify the metal/semiconductor interface. These diodes exhibit remarkable rectified performance, with a Schottky barrier height of 0.61 eV and a rectification ratio of 234 at  $\pm 1$  V. These diodes also exhibit excellent long-term stability without encapsulation.

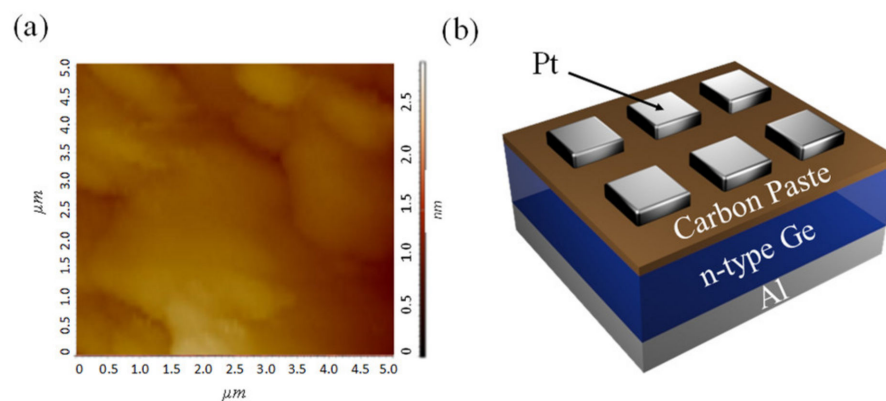
## 2. Materials and Methods

### 2.1. Materials

This study uses commercial CP from Alfa Aesar Co., Ltd. (Haverhill, MA, USA) (42465, alcohol-based) and n-type Ge (100) substrates, having a carrier concentration of  $5.0 \times 10^{15} \text{ cm}^{-3}$ . The CP films were then spin-coated at 5000 rpm for 60 s, followed by pre-baking at 60 °C in an ambient atmosphere for 15 min on a hotplate. The sample was then sintered in a furnace in an Ar atmosphere at 300 °C for 30 min.

### 2.2. Characterization

The thickness of the CP film was  $\sim 70$  nm, as measured using a profilometer. Atomic force microscopy (AFM) was used to determine the surface morphology of the CP films. The surface morphology of a CP film is quite smooth, as shown in Figure 1a. The root-mean-square (rms) roughness value for a CP film is 0.915 nm. Pt electrodes ( $300 \times 300 \mu\text{m}^2$ ) were produced by means of sputtering through a shadow mask. The structure is shown in Figure 1a. For comparison, a reference device without a CP interlayer was fabricated using the same process conditions. The current–voltage ( $I$ – $V$ ) curves for the Schottky diodes were measured using a Keithley 2400 sourcemeter. The capacitance–voltage ( $C$ – $V$ ) plots for the Schottky diodes were recorded using an Agilent E4980A impedance analyzer.



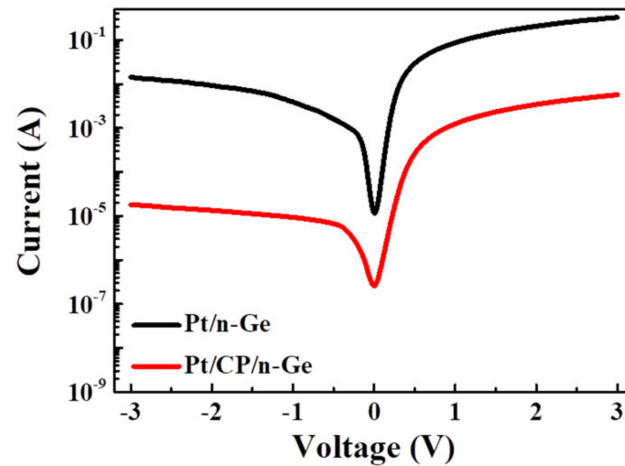
**Figure 1.** (a) Atomic force microscopy (AFM) image of a carbon paste (CP) film and (b) device structure of a Pt/CP/n-Ge Schottky diode.

## 3. Results and Discussion

### 3.1. $I$ – $V$ Characteristics

The effect of an interfacial layer on the electrical characteristics is considered. Figure 2 shows the experimental semi-logarithmic  $I$ – $V$  characteristics for Pt/n-type Ge Schottky rectifiers with and without a CP interlayer in the dark. Both diodes exhibit excellent rectification behavior. The characteristic properties of the rectifying contact behavior mean that a reverse bias current has no significant effect on the voltage and there is an exponential increase in the forward bias current. A higher current rectification ratio is achieved for a

Pt/CP/n-Ge Schottky junction (234) than for its counterpart (20). Figure 2 shows that the leakage current in reverse bias for Pt/CP/n-Ge Schottky junction is less than that for the counterpart, which demonstrates that the CP interlayer creates an effective barrier between Pt and Ge.



**Figure 2.** Experimental I–V curves for Pt/n-Ge Schottky diodes with and without a CP interlayer.

Besides, owing to the existence of bulk resistance of the CP interlayer, there is an obvious decrease at high current for the Pt/CP/n-Ge Schottky junction in the forward bias I–V plot. Standard thermionic emission theory is used to examine the electrical properties for a Schottky diode, which is given as follows [19]:

$$I = AA^*T^2 \exp\left(\frac{-q\Phi_B}{kT}\right) \left\{ \exp\left[\frac{q(V - IR_s)}{nkT}\right] - 1 \right\} \quad (1)$$

where  $A^*$  is the Richardson constant for Ge, which is  $140 \text{ A cm}^{-2}\text{K}^{-2}$ ;  $\Phi_{B,IV}$  is the barrier height;  $k$  is the Boltzmann constant;  $q$  is the electronic charge;  $R_s$  is the series resistance; and  $n$  is an ideality factor [12]. The extracted parameters for Schottky diodes are listed in Table 1. For Pt/n-Ge and Pt/CP/n-Ge Schottky junctions,  $\Phi_{B,IV}$  and  $n$  are 0.57 eV and 1.08 and 0.65 eV and 1.95, respectively. The value of  $\Phi_{B,IV}$  for the studied diode (0.65 eV) is higher than that for the counterpart (0.57 eV). The CP layer produces a higher barrier of 0.08 eV. This result is in agreement with the results of previous reports [11,13]. An organic interlayer prevents direct contact between the metal and Ge surface and significantly changes the interface states, even though the organic/inorganic interface is abrupt and unreactive [20–22]. A conventional Ge Schottky contact generally has a strong Fermi-level pinning effect, which leads to poor device performance (i.e., high  $n$  and low  $\Phi_B$ ). This result is attributed to the metal-induced gap states. Ion bombardment during plasma processing is another possible reason that the surface of the Ge substrate is destroyed, which induces defects and intermixing in the films. The values for  $n$  and  $\Phi_B$  for the reference diode for this study ( $n = 1.08$ ;  $\Phi_B = 0.57$ ) are comparable to those reported by previous studies [11–13]. Further improvement in the future is possible. For a conventional Schottky diode, the value for  $n$  is close to unity. This result shows that the diode current is mainly due to diffusion current and the pure thermionic emission theory fits well. However, the value for  $n$  for a Pt/CP/n-Ge Schottky junction is much higher than unity, possibly because of secondary mechanisms, such as CP of uneven thickness, series resistance, and a non-uniform distribution of dipoles due to the presence of an organic interfacial layer [23–26]. This phenomenon is also noted in previous studies that use an organic interfacial layer for Schottky diodes [11–13]. The exact reason for a higher  $n$  value is unclear. Generally, an interfacial layer is used to modulate the Schottky barrier height using Fermi level depinning. The value for  $\Phi_B$  increases as the  $n$  value increases. The parameters for Pt/CP/n-Ge Schottky diodes could be further optimized.

**Table 1.** Schottky diode parameters derived using various methods. CP, carbon paste.

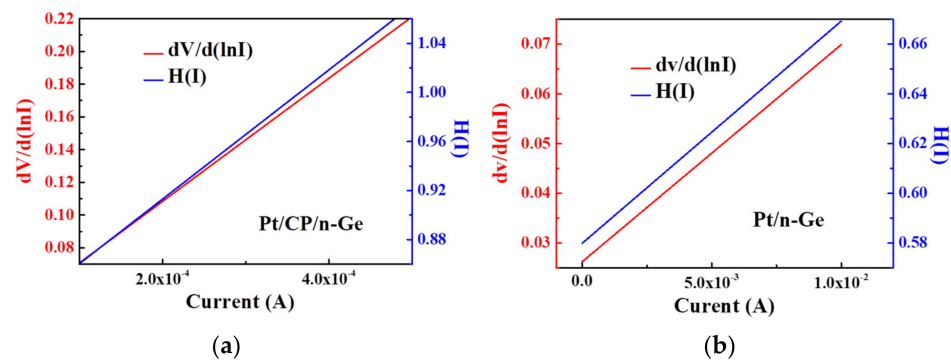
	<i>I</i> - <i>V</i>		<i>dV/d(lnI)</i> vs. <i>I</i>		<i>H(I)</i> vs. <i>I</i>		Norde		<i>C</i> - <i>V</i>
	$\Phi_B$ (eV)	<i>n</i>	$R_S$ ( $\Omega$ )	<i>n</i>	$R_S$ ( $\Omega$ )	$\Phi_B$ (eV)	$R_S$ ( $\Omega$ )	$\Phi_B$ (eV)	$\Phi_B$ (eV)
w/o CP	0.57	1.08	4.37	1.01	8.93	0.57	12.14	0.58	0.82
w/i CP	0.65	1.95	376	1.28	459	0.65	2735	0.72	0.9

The plots of Cheung's function  $dV/d(\ln I)$  versus  $I$  and  $H(I)$  versus  $I$  are used to accurately determine the Schottky parameters,  $\Phi_{B,H(I)}$ ,  $n$ , and  $R_s$ , as shown in Figure 3. Cheung's function is expressed as follows [12,27]:

$$\frac{dV}{d(\ln I)} = \frac{nkT}{q} + IR_S \quad (2)$$

$$H(I) = V - \left(\frac{nkT}{q}\right) \ln\left(\frac{I}{AA^*T^2}\right) \quad (3)$$

$$H(I) = n\Phi_{B,H(I)} + IR_S \quad (4)$$

**Figure 3.** Plots of  $dV/d(\ln I)$  versus  $I$  and  $H(I)$  versus  $I$  using diode Equation (1) for Pt/n-Ge Schottky diodes (a) with and (b) without a CP interlayer.

The plot of  $dV/d(\ln I)$  versus  $I$  is linear with a gradient of  $R_s$  and the y-intercept gives the ideality factor  $n$ . The respective values of  $R_s$  and  $n$  are 4.37  $\Omega$  and 1.01 for the Pt/n-Ge Schottky diode, and 376  $\Omega$  and 1.28 for the Pt/CP/n-Ge Schottky diode. The  $H(I)$  versus  $I$  plot is a straight line and the y-axis intercept gives the value for  $\Phi_{B,H(I)}$ . The gradient of this plot can also be used to determine the value of  $R_s$ . From the  $H(I)$  versus  $I$  plot, the  $R_s$  and  $\Phi_{B,H(I)}$  values are 8.93  $\Omega$  and 0.57 eV for the Pt/n-Ge Schottky junction and 459  $\Omega$  and 0.65 eV for the Pt/CP/n-Ge Schottky junction. The large difference in the values is attributed to a deviation from the ideal model due to the insertion of the CP layer, so the value of  $R_s$  is higher [28]. The higher  $R_s$  limits the forward current, as shown in Figure 2. An additional decrease in voltage across the CP interlayer produces forward current conduction at a high voltage.

The values of  $\Phi_{B,Norde}$  and  $R_s$  for Schottky junctions are also derived using the modified Norde function, which is expressed as follows [29]:

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q} \ln\left(\frac{I(V)}{AA^*T^2}\right) \quad (5)$$

where  $I(V)$  is the current obtained from the  $I$ - $V$  curves and  $\gamma$  is an integer (dimensionless) that is greater than the value of  $n$ . Figure 4 presents the Norde plot as function of applied bias for Pt/n-Ge and Pt/CP/n-Ge Schottky junctions. The minimum point is used to

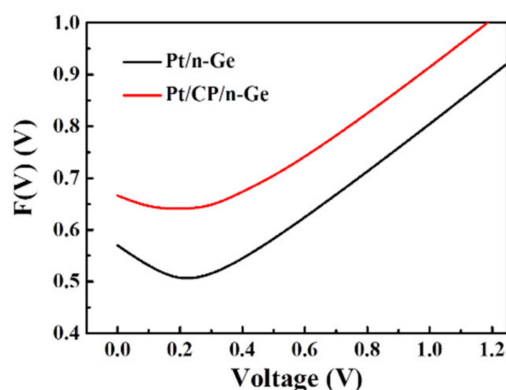
obtain the corresponding voltage that is applied across the device. The value of  $\Phi_{B, \text{Norde}}$  is derived using the following equation [29,30]:

$$\Phi_{B, \text{Norde}} = F(V_0) + \frac{V_0}{\gamma} - \frac{kT}{q} \quad (6)$$

where  $F(V_0)$  is the minimum point of  $F(V)$  and  $V_0$  is the corresponding voltage. The value of  $R_s$  is determined using the following relation:

$$R_s = \frac{kT(\gamma - n)}{qI_0} \quad (7)$$

where  $I_0$  is the minimum point of  $F(V_0)$ . The values for  $R_s$  and  $\Phi_{B, \text{Norde}}$  are calculated as 12.14  $\Omega$  and 0.58 eV for the Pt/n-Ge Schottky junction and 2735  $\Omega$  and 0.72 eV for the Pt/CP/n-Ge Schottky junction, respectively. The  $R_s$  and  $\Phi_{B, \text{Norde}}$  values that are derived using Norde's function are higher than those derived using Cheung's method because different fitting intervals are used for the  $I$ - $V$  curve. Cheung's function focuses on the nonlinear region and the Norde plot considers the whole range of the  $I$ - $V$  curve in forward bias [28,30]. Even if there is a difference in the values for different fitting techniques, Schottky contacts show reasonably good agreement in terms of the value of  $\Phi_B$ .



**Figure 4.** Norde plot for Pt/n-Ge Schottky diodes with and without a CP interlayer, using the diode Equation (1).

### 3.2. C-V Characteristics

The C-V characteristics of the Schottky diodes are shown in Figure 5. The capacitance of the depletion layer is described using a standard Mott-Schottky relationship [31]:

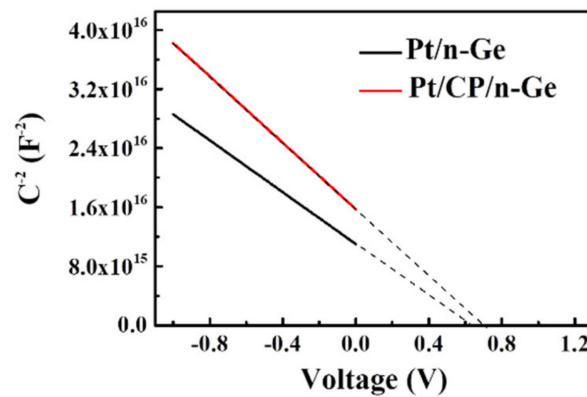
$$\frac{1}{C^2} = \frac{2(V_{bi} - V)}{A^2 q \epsilon_s \epsilon_0 N} \quad (8)$$

where  $A$  is the surface area,  $\epsilon_s$  is the permittivity,  $\epsilon_0$  is the dielectric constant,  $V_{bi}$  is the built-in potential, and  $N$  is the carrier concentration. The x-intercept is  $V_{bi}$ . The gradient is  $N$ . The value of  $\Phi_{B, CV}$  can be calculated as follows [31]:

$$\Phi_{B, CV} = \Phi_{bi} + \frac{kT}{q} \ln\left(\frac{N_C}{N}\right) \quad (9)$$

where  $N_C$  is the conduction band density states of  $1.0 \times 10^{-19} \text{ cm}^{-3}$  [12]. A list of electronic parameters for the Schottky diodes is given in Table 1. The C-V characteristics give a barrier height of 0.90 eV for a Ge Schottky diode with a CP interlayer and 0.82 eV for a Pt/n-type Ge Schottky diode with no CP interlayer. The increase of  $\Phi_{B, CV}$  is consistent with the results of  $I$ - $V$  measurements when there is a CP interlayer. There is a relatively large discrepancy between the value for  $\Phi_{B, IV}$  and  $\Phi_{B, CV}$  because the conduction mechanism in these diodes does not exactly obey the thermionic emission theory. The values of  $\Phi_{B, IV}$

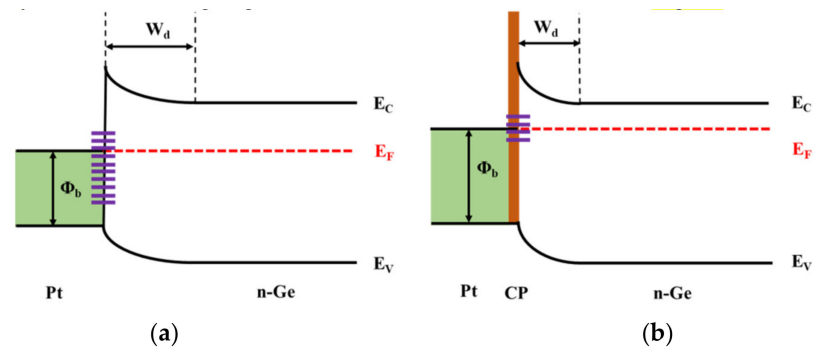
derived from the  $I$ - $V$  curve are sensitive to image force due to the current flow across the barrier [32]. The values of  $\Phi_{B, CV}$  derived from the  $C$ - $V$  curve are insensitive to potential fluctuations because the scale is much shorter than the space charge region [33]. The  $C$ - $V$  measurement gives an average barrier height for the entire diode, but the current flows preferentially through the barrier minima during  $I$ - $V$  measurement [33]. The difference between  $C$ - $V$  and  $I$ - $V$  measurement techniques results in different results for Schottky barrier height [34].



**Figure 5.**  $A^2/C^2$ - $V$  characteristics for Pt/n-Ge Schottky diodes with and without a CP interlayer.

### 3.3. Energy Band Diagrams

The role of the CP interlayer for Pt/CP/n-Ge Schottky diodes is demonstrated using an energy diagram, as shown in Figure 6. At the metal/semiconductor interface, there are many dangling bonds, so there is a strong Fermi level pinning effect, as shown in Figure 6a. CP is an interlayer that conducts charged carriers with tiny resistance. The CP interlayer play a role of a dangling bond terminator at the Ge surface (Figure 6b).

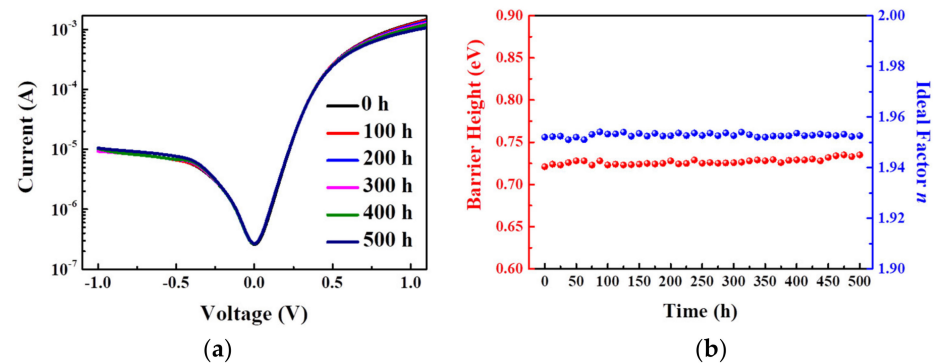


**Figure 6.** Energy band diagrams for Pt/n-Ge Schottky diodes (a) with and (b) without a CP interlayer.

### 3.4. Long-Term Reliability

Long-term reliability is a key factor for a diode for real applications [35–37]. To the best of the author's knowledge, there is no standard specification involving stability tests for Schottky diodes. To determine the long-term reliability of the CP interlayer, a Schottky diode with CP was driven under 0.1 A under ambient conditions, with no encapsulation or humidity control, over a period of 500 h. The fluctuation in  $\Phi_B$  and  $n$  is negligible over the time of the test, as shown in Figure 7a,b. The organic layer is the only source for device degradation because the crystalline Ge and metals are relatively stable in air. Compared with the emerging organic layer for a Pt/n-Ge Schottky diode, such as PEDOT/PSS, the ambient stability for the device is poor because a PEDOT/PSS film contains water soluble ionic PSS [13]. The sheet resistance for pristine PEDOT/PSS film increases by more than 20% after storage in air for 1 week [38]. In addition, the carbon-containing diode exhibits long-term stability under a DC bias, which is attributed to the excellent thermal

stability of CP. When current flows cross a contact, spot heat is generated in the constriction resistance [39], which decreases the performance of an organic semiconductor. CP is primarily composed of graphite powder and graphite is resistant to high temperatures [18]. Therefore, commercially available CP is eminently suited to the fabrication of highly stable and efficient Schottky diodes.



**Figure 7.** (a)  $I$ – $V$  characteristics for a Pt/CP/n-Ge Schottky diode for different DC stress (0.1 A) times and (b)  $\Phi_B$  and  $n$  as a function of stress time, as obtained from the diode equation (1): the measurements were performed at room temperature in ambient conditions.

#### 4. Conclusions

An organic–inorganic structure is formed using a CP thin film as an interlayer for a Pt/n-Ge Schottky diode. To determine the electrical characteristics of the Pt/CP/n-Ge Schottky diodes, the  $I$ – $V$  and  $C$ – $V$  characteristics are measured at room temperature. This structure exhibits better rectifying behavior and results in a higher barrier height than a conventional Pt/n-Ge diode because the effective barrier height is increased when there is a CP interlayer. This study shows that CP is a reliable interlayer for an inorganic–organic hybrid Schottky diode.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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