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# Embedded Silicon Nanoparticles as Enabler of a Novel CMOS-Compatible Fully Integrated Silicon Photonics Platform

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**Abstract:** The historical bottleneck for truly high scale integrated photonics is the light emitter. The lack of monolithically integrable light sources increases costs and reduces scalability. Quantum phenomena found in embedded Si particles in the nanometer scale is a way of overcoming the limitations for bulk Si to emit light. Integrable light sources based in Si nanoparticles can be obtained by different CMOS (Complementary Metal Oxide Semiconductor) -compatible materials and techniques. Such materials in combination with $Si_3N_4$ photonic elements allow for integrated Si photonics, in which photodetectors can also be included directly in standard Si wafers, taking advantage of the emission in the visible range by the embedded Si nanocrystals/nanoparticles. We present the advances and perspectives on seamless monolithic integration of CMOS-compatible visible light emitters, photonic elements, and photodetectors, which are shown to be viable and promising well within the technological limits imposed by standard fabrication methods.

**Keywords:** integrated photonics; silicon light sources; nitride photonics; SRO



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## 1. Introduction

Integrated photonics [1–4] have an ever-increasing relevance from communications to sensing. While much improvement has been achieved regarding passive and active optical light-guiding elements, the historical bottleneck for truly high scale Photonic Integrated Circuits (PICs) has been the lack of an easily integrable light source. The need for either coupling external emitters [5] or for heterogeneous integration of non-MOS compatible light sources [6] is a significant disadvantage in the regard of cost and scalability.

Embedded nanocrystals (ncs) [7–9] and nanoparticles (nps) [10–12] represent exciting possibilities for integrated light emitters due to the quantum phenomena observed at nanometric scale, overcoming the main impediment for Si-based light emitting devices: its indirect bandgap characteristics when in bulk.

The observation of PL at room temperature in porous Si by Canham is widely considered as the first sight of possible light generation in such material for further integration with electronics [13,14]. This triggered the study of a variety of nanometric Si-based materials in pursue of better chemical and structural stability, CMOS-compatible fabrication process, and control of the characteristics of the emitted light [15–17]. One of the most promising compliant materials is the Silicon Rich Silicon Oxide (SRO). This is a SiOx with $0 < x < 2$, in which, after a specific thermal treatment, the silicon atoms not forming dioxide can nucleate to obtain embedded Si-nps [10,18].

The demonstration of Light Emitter Capacitors based on SRO promised the viability of monolithically integrated light emitter using CMOS compatible materials and processes [6,7,19–22]. The further demonstration of emission enhancement by combining

SRO and $Si_3N_4$ [17,23,24] was a step forward which, in addition, opened the door for seam-less coupling of light emitters and waveguides in the same process on standard Si substrates [25], dramatically reducing costs and increasing scalability.

To further advance on this matter, it is necessary to understand the balance between the benefits and disadvantages this novel and exciting technology. The viability of optical components is ascribed to the fabrication limits, such as a reduced variety of materials, maximum thicknesses achievable by standard procedures, lithographic resolution, etc. The characteristics of the light produced by the nanoparticles-based light emitters is also an important matter to consider, as it can significantly differ from the light produced by externally coupled lasers, which currently dominate the integrated photonics field. Finally, integrable light detectors must also be analyzed or designed in order to accommodate the architecture, materials and light characteristics.

In this work, we examine the perspective of a fully integrated electrophotonic Si-based platform with directly embedded light sources based on Si nanoparticles. We briefly review the current advances on the development of discrete elements necessary for an SRO\$Si_3N_4$ integrated photonics platform, and, along with the proposal of previously unreported results, we analyze them from a holistic point of view, taking into consideration the intricate interrelation between light emitters, passive photonic elements, and available light sensing schemes to assess the viability of monolithic integration using standard CMOS.

## 2. Materials and Methods

All the materials and devices here analyzed were obtained using standard CMOS processes and standard crystalline Si wafers as substrate. The active materials and photonic elements are based in $SiO_2$, $Si_3N_4$, polycrystalline Si, and Al.

The SRO and SRO-$Si_3N_4$ films were fabricated using Low Pressure Chemical Vapor Deposition (LPCVD) with silane and nitrous oxide as precursor gases, and Ionic Implantation (II) of Plasma Enhanced Chemical Vapor Deposition (PECVD) $SiO_2$. Details on temperatures, pressures, gas flows, II energies and doses, and thermal treatments, as well as characterization experimental details, can be found in References [9,10,26–29].

Details on the fabrication and characterization of electroluminescent devices with polished and unpolished substrates, can be found in References [16,24,30,31], except for the texturization of substrates obtained using the Metal Assisted Chemical Etching (MACE) technique, which is described in References [32,33].

The fabrication and characterization details on the monolithic emitter-waveguide-detector systems can be found in References [25,34].

The simulation of the passive photonic elements was performed using the tools provided by the software *Lumerical* (Vancouver, BC, Canada). Mode and field propagation simulations were performed using *Mode* and *FDTD*. The S-parameters were extracted from these to calculate losses by means of *Interconnect*. The refractive index of the silicon nitride was the one measured by ellipsometry from samples deposited by LPCVD, which were consistent to Palik data from *Lumerical*. The simulation domains were delimited by perfectly matched layers (PML) in around the cladding limits.

The simulation of the fabrication process of the waveguided sensor was done using the software *Silvaco-Athena* (Santa Clara, CA, USA), accounting for all the steps needed to obtain nanoparticle-based emitters using II-SRO, including thermal treatments as described in Reference [24]. Its electro-optical response was simulated using *Silvaco-Atlas* (Santa Clara, CA, USA), applying 0 V to source and substrate and 5 V in the gate.

## 3. Luminescence from Nanoparticles in a Dioxide Matrix: SRO

As mentioned, one of the most successful materials containing light-emitting silicon nanoparticles is SRO. It can be fabricated using a variety of CMOS-compatible techniques, of which Low Pressure Chemical Vapor Deposition (LPCVD-SRO), Plasma Enhanced Chemical

Vapor Deposition (PECVD-SRO), and Si Ion Implantation into $SiO_2$ (II-SRO) matrices stand out due to their technical simplicity and light emission characteristics [16,26,35].

During the fabrication process of the SRO films, different parameters can be controlled to modify the atomic Si contents in the material. For LPCVD-SRO, the defining parameter is the partial pressures ratio ($R_0 = PN_2O/PSiH_2$) from precursor gasses flow [16], and for II-SRO the Si-ion implantation dose. The posterior thermal annealing can also be tuned for optimal Si-nucleation and consequent nps size and density in order to obtain optimal light emission [10,36]. In addition, the use of multiple layers of SRO with different characteristics, or silicon nitrides stacked to the main active material, can influence the final emission spectra, as well as the conductivity of the stack structure. Despite the material being intended as part of an electronic device, hence, its emission will be electrically stimulated (Electroluminescence, EL), Photoluminescence (PL) characterization is a powerful tool to understand the emission mechanisms and characteristics in the material, which are fundamentally the same as those for EL [24]. In PL, the emission is stimulated pumping higher energy light (usually ultraviolet for SRO) for photons to be re-emitted with lower energies (in the visible range for SRO). Figure 1 shows examples of PL emission spectra for various SRO and SRO\$Si_3N_4$ films when being pumped with UV light. Table 1 summarizes the main characteristics of the emission for active materials with different fabrication parameters. Note that the required times and temperatures by the SRO annealing, while fully available in most CMOS lines, are generally larger than those used for regular processes, such as dopant diffusion or thermal oxidation. Nevertheless, it has been shown that, if the fabrication sequence is adequately planned, the influence by SRO fabrication on electronic circuits, as well as by circuitry fabrication on SRO, are both null [37]. Detailed studies regarding the origin of light emission in SRO can be found in References [9,10,26–29].

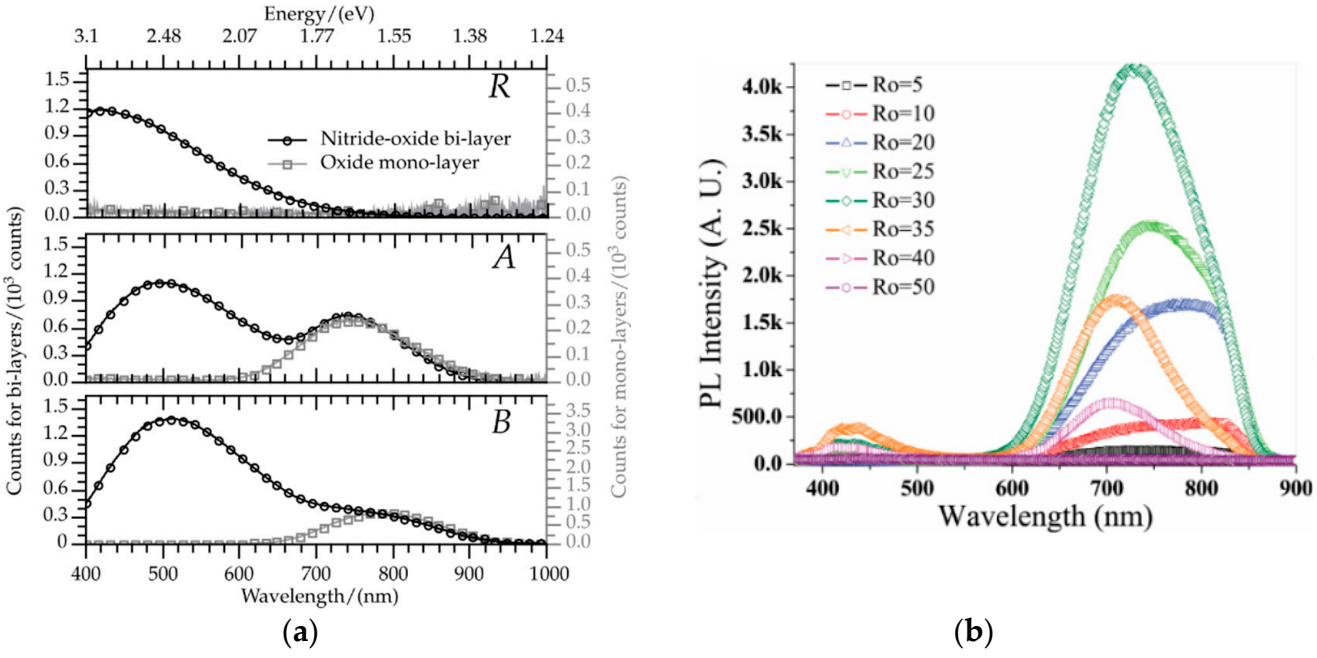



**Figure 1.** (**a**) PL spectra of II-SRO and II-SRO/Si3N4 films [38]; (**b**) LPCVD-SRO films with different precursors gas ratios, $R_0$ [28].

**Table 1.** Fabrication parameters and characteristics of different SRO films.

| Type of Active Layers | Si Contents in SRO (at. %) | Thermal Treatment | PL Spectral Range (nm) | PL Peak Emission (nm) |
|---|---|---|---|---|
| PECVD-SRO [27] | 45<br>40.5<br>37 | 60 min, 1250 °C | from 670 to 885<br>from 354 to 468<br>from 354 to 516 | 775<br>435<br>442 |
| LPCVD-SRO [27] | 44.5<br>38.4<br>37.3 | 60 min, 1100 °C | from 688 to 855<br>from 438 to 939<br>from 438 to 855 | 765<br>765<br>733 |
| II-SRO [38] | 34.6<br>33.8 | 240 min, 1100 °C | from 650 to 940 | 785<br>746 |
| II-SRO\$Si_3N_4$ [38] | 34.6<br>33.8<br>32.7 | 240 min, 1100 °C | from 380 to 940<br>from 380 to 940<br>from 380 to 750 | 509<br>509<br>412 |

As mentioned, in the frame of an electronically-driven PICs, the stimuli to the emitting material are expected to be electrical, and, while the physical phenomena concerning light emission are fundamentally the same for EL and PL, other aspects, such as electronic transport and efficiency, must be considered for integrated EL devices [35], as well as the stimuli of different radiation centers in distinct proportions [21]. When characterizing EL, the need for an electrode on top of the SRO is an added difficulty, which, in the case of external light characterization, it must be conductive, while, at the same time, allow light transmission. Highly doped polysilicon is often the material of choice for this, due to its compatibility with standard CMOS, and its acceptable transmittance characteristics [24]. This results in a Light Emitting Capacitor (LEC) configuration as the one exemplified in Figure 2. In this particular case, a $Si_3N_4$ layer between SRO and electrode is included, as it has been observed to improve efficiency and emission spectrum [17,23,24]. Figure 3 shows examples of EL emission spectra and images of LECs with single SRO layers (a) and with Silicon Nitride-SRO bi-layers (b). When obtaining external EL spectra, optical effects caused by the multi-layer configuration and transmittance characteristics of the electrode material must be considered in the analyses [39].

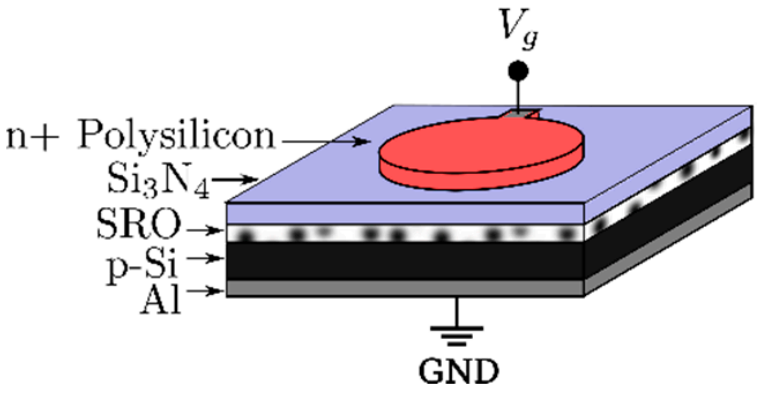
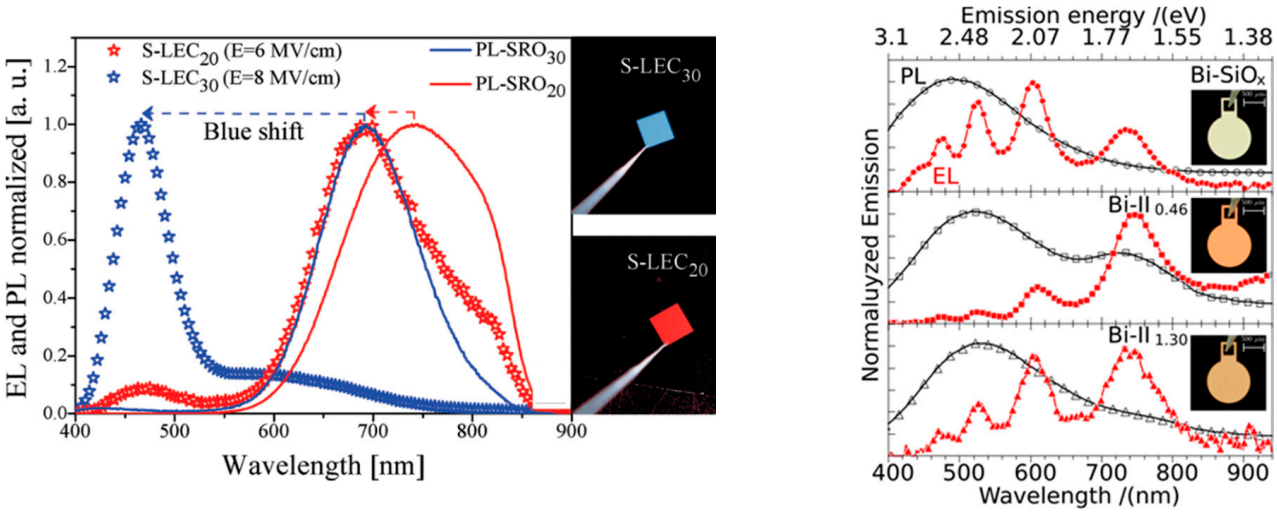



**Figure 2.** Light Emitting Capacitor stack structure based on SRO/$Si_3N_4$ bi-layers (not on scale) [24].




(**a**) (**b**)

**Figure 3.** (**a**) Micrographs and EL spectra of LPCVD-SRO LECs [16]; (**b**) II-SRO/$Si_3N_4$ LECs [24].

Other mono-layer and stack structure configuration have been more recently proposed with aims to improve emission efficiency, such as single SRO layers, multilayers of SRO with different content of silicon, and two types of Si substrates, by using polished or textured surface [30,31].

In general, the EL spectra extend from blue to near infrared, with two mean peaks that vary with voltage applied across the structure, as presented in Figure 4. Cathode-luminescence experiments have shown that the blue side of the emission spectrum is more prominent when higher stimulation energies are used, indicating a pathway to modulate the emission spectra electrically [40].

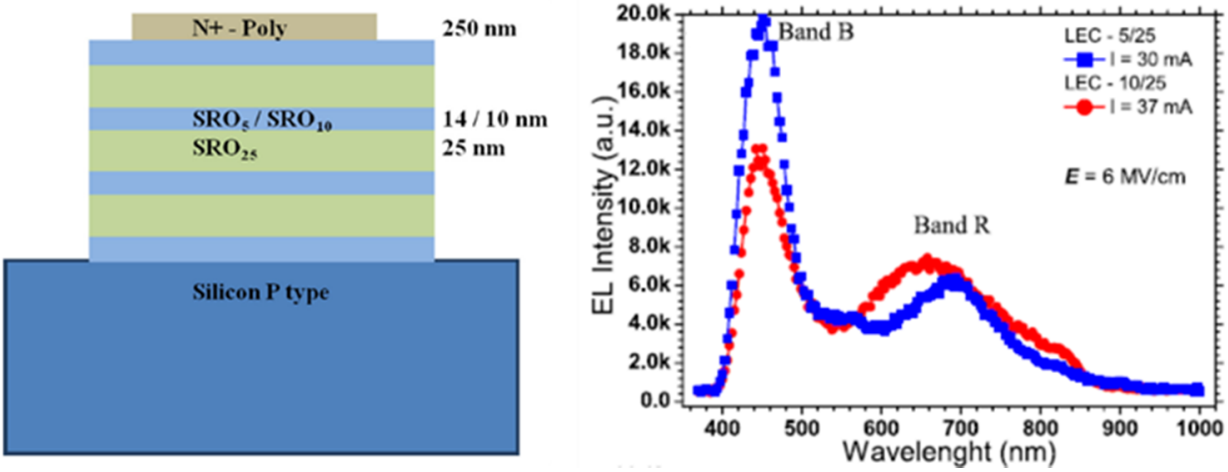



**Figure 4.** Schematic (**left**) and EL spectra (**right**) of multilayered structure made of nanolayers of $R_0$ =25 and $R_0$ = 10. $R_0$ = 10 or 5 improves the conduction properties, and $R_0$ = 25 is used because of high emission properties [31].

Aside from influencing the light emission spectra, Si contents in SRO also plays a significant role in its conductivity. One approach to improve the electrical characteristics of the LEC while achieving desired emission characteristics is to alternate SRO films with different Si contents. Figure 4 left and right, respectively, show a schematic representation of a multilayer structure and corresponding EL emission spectra. The layered structure uses LPCVD-SRO with $R_0$ = 5 or $R_0$ = 10 as high conductive layers, and $R_0$ = 25 as highly emissive layers. As it can be seen, the multilayered structures have similar emission spectra

as those from monolayers, and, due to the presence of higher conduction regions, an improvement in the electrical characteristics is achieved [31].

Another approach to improve electrical injection uses texturized Si substrates. Figure 5 compares maximum achieved EL spectra form LECs based on SRO deposited on polished and textured Si substrates. The textured substrates presented "tips" on the Si surface obtained by reactive ion etching [30]. As can be seen, the spectra present the two characteristic peaks found in single SRO layer LECs, but the structure with textured substrate can achieve emission intensities almost twice as large as compared to the one with polished substrate. Furthermore, electrical power required by the polished substrate for the maximum emission is 2.6 times higher [30].

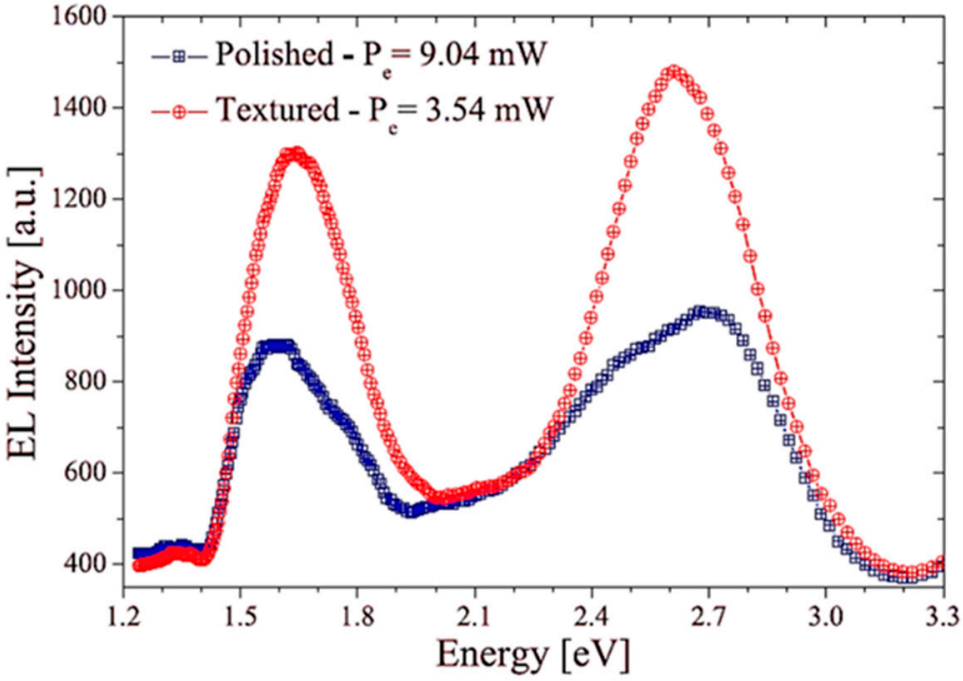



**Figure 5.** EL spectra of LECs with polished and textured Si substrate. The two main peaks expected in single layer SRO LECs are clearly identified. However, an improvement of the emission intensity of almost twice is observed in textured substrate, and lower electric power is required [30].

Additional promising results with texturized substrates were also found in devices in which the process was performed by MACE. In this method, metal particles are deposited on the Si surface followed by an etching process in a HF-oxidant based solution [32,33]. The Si beneath the metal particles is oxidized by the solution and then removed due to the presence of HF, leaving a textured surface with an average roughness of 7.5 nm. Figure 6 displays the integrated EL intensity as function of the electric field applied to the LECs both polished and texturized.

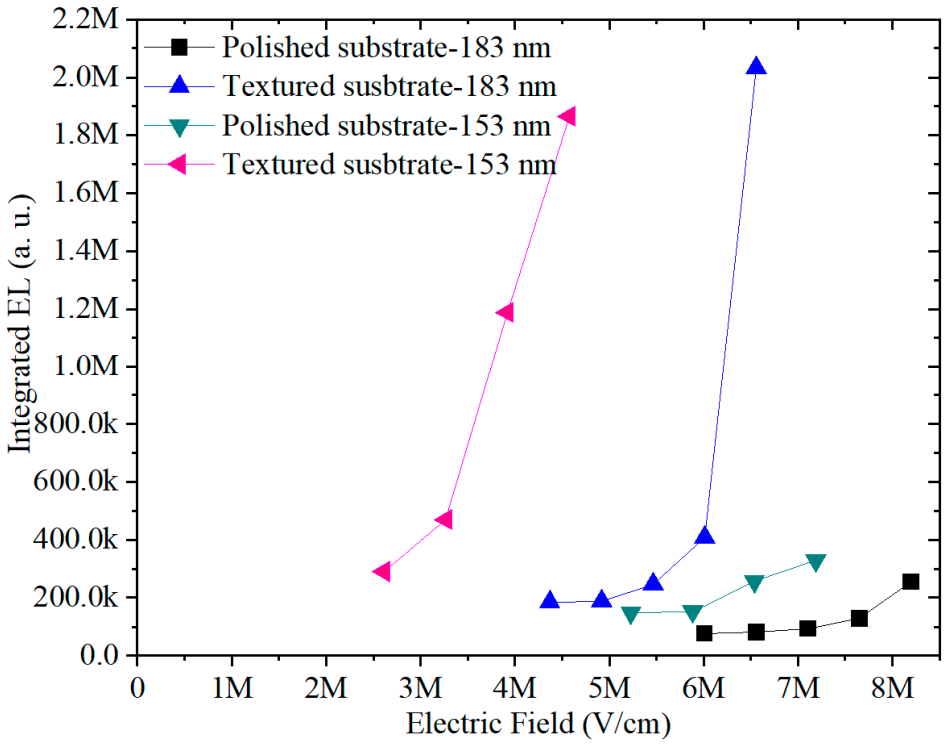



**Figure 6.** Integral of EL intensity as function of the applied electric field for devices with polished (solid symbols) and textured (empty symbols) substrates; 183 nm and 153 nm refer to film thickness.

As it can be seen, LECs with substrate texturized by MACE start emitting at significantly lower electric fields, and higher EL intensities are achieved. The explanation for better EL result in texturized substrates is related to the increment of the electric field intensity on the sharper tips, which promotes an increment in the density of electrons available to move through the LEC and stimulate the emission centers along its way. Despite the potentially higher efficiency of these kind of devices, MACE texturization involves processes not currently available in standard CMOS. Then, while this shows there still are ways to improve emitters, it is well worth the effort to optimize the rest of the components (waveguide, photodetectors) to be coupled to the currently well documented CMOS compatible LECs in standard substrates, provided its performance is adequate.

## 4. SRO\$Si_3N_4$ Systems for Emitter-Waveguide Integration

As mentioned, the inclusion of a $Si_3N_4$ layer can improve the emission of SRO-based LECs. Its use produces devices with higher electrical stability, as it increases the EL intensity at reduced electric fields [17]. In addition, if the active material is II-SRO, a nitride film can assist in the control of the dose and depth of the implanted Si ions [41]. During this implantation process, an interfacial silicon oxynitride can be formed between oxide and nitride, which has been shown to introduce an additional light emission band in the blue side of the visible spectrum [38]. This can be advantageous for applications, such as chemical and biochemical sensing [4,42,43]. Different Si ion implantation doses in $SiO_2$\$Si_3N_4$ systems produce a nitride-oxynitride-SRO stack system with different structural characteristics which, on its turn, can modify the emission spectra of the resulting LECs [38], as observed in Figure 1.

The introduction of Si nitride in the emission enables a significant additional advantage: the possibility of seamlessly embedding the emitter into the waveguide, provided the latter is made of $Si_3N_4$. This means there are no coupling issues to be addressed, as the light is directly produced inside the waveguide, presenting spectral characteristics very similar to the PL from the active layer, and $Si_3N_4$ is suitable for transmission of such

light, as it is transparent for wavelengths (λ) spanning from 0.4 μm to approximately 4 μm, and presents respective refractive index values of 2.1 and 1.9, which represents contrast to $SiO_2$ between 28% and 38%, allowing for reported waveguide losses between 0.001 dB/cm and 0.5 dB/cm [44]. It can also be fabricated using the same standard Chemical Vapor Deposition techniques used for the LECs, and it is very easy to combine with standard $SiO_2$ for core-cladding structures.

The first report of the seamlessly embedded SRO\$Si_3N_4$ light emitter approach was published in Reference [25], in which a standard p-n diode was used as the light detector. A scheme of the system is presented in Figure 7.

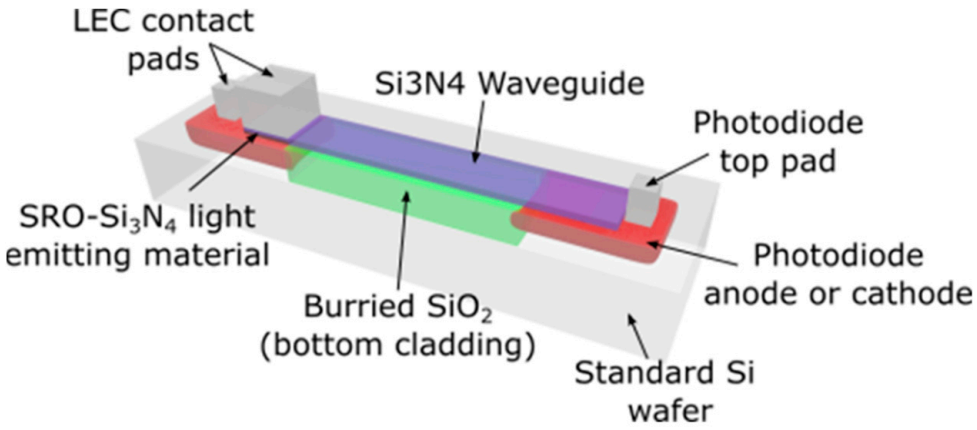



**Figure 7.** Schematic of a monolithic transceiver with light emitting diode based on SRO (LEC), waveguide, and photodiode.

The work proposed a CMOS compatible fabrication process integrating an LEC consisting of a bottom II-SRO layer and a top $Si_3N_4$ film which extended to form a slab waveguide. The bottom cladding was buried $SiO_2$ between photoemitter and photodetector. The thickness of this was designed to prevent the light emitted by the SRO\$Si_3N_4$ from transferring to the much higher refractive index Si substrate. Figure 8a shows simulations obtained using the software LUMERICAL for light with a wavelength of λ = 509 nm being transmitted by a 60 nm-thick nitride core waveguide (WG). This is one of the main emission peaks by II-SRO, as can be observed in Figure 1a. The cross section of the WG core (gray lines) is centered at z = 0. There is no evanescent field at z = −1.5 μm, assuring no leak of light to the substrate.

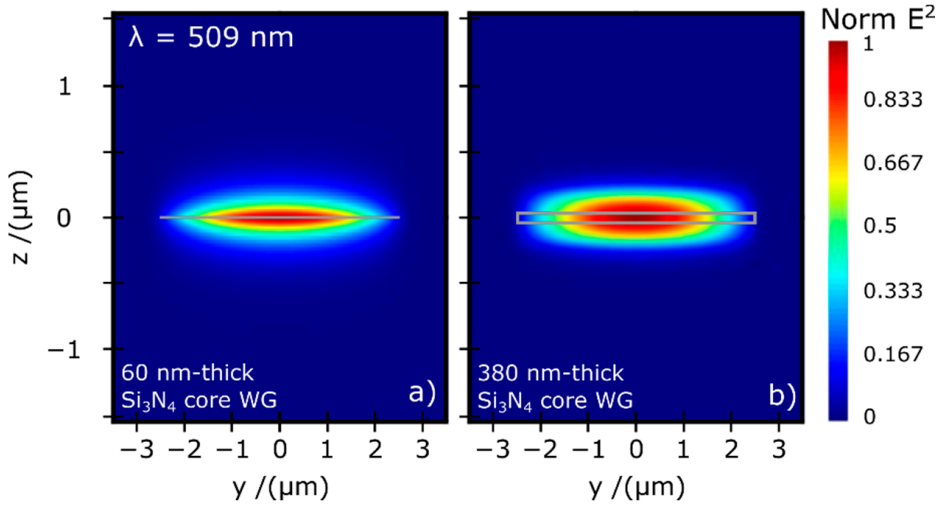



**Figure 8.** $TE_0$ mode distributions for waveguides with core of (**a**) 60 nm-thick and (**b**) 380 nm-thick $Si_3N_4$. The light has a wavelength λ = 509 nm.

This apparently straightforward approach comes with several considerations during the design of the geometries and fabrication processes affecting the size, density, and distribution of the Si nps, as a multitude of factors will influence the behavior of the coupled system. For instance, some of the geometrical parameters of the waveguides are constrained by limits imposed by the emitter, such as the thickness, which has a significant impact in the voltage necessary to drive the emitter. In this regard, there are proposals to decouple this design parameter from emitter and WG, while keeping the nitride seamlessly integrating both devices [45]. This allows for better mode confinements, and consequently thinner cladding layers between core and substrate. Figure 8b shows the simulations for the transmission of the same 509 nm peak but considering a waveguide with core thickness of 380 nm. A clearly larger proportion of the field is transmitted through the core as compared to those with 60 nm-thick cores. However, the core thickness increment is severely limited by tensile stress suffered by $Si_3N_4$ when deposited on Si, limiting its thickness to 700 nm in extreme cases [4,44,46].

In addition, the nature of the emitted light must be well considered in the design of the photonic elements. As mentioned, the emitter based on Si-nps has the great advantage of integrability and CMOS compatibility, but a wide emission spectrum is currently unavoidable, and there is no evidence of specific polarization and coherence of the light. This limits the variety of photonic elements that can be implemented. For instance, interferometers are not straightforward to implement.

However, depending on the application, the photonic elements used to transmit and manipulate the light can be carefully designed to use the specific features of the emitted light as an advantage, e.g., there is great potential for wavelength demultiplexing modulation, or for biophotonic sensing applications, in which the visible spectrum can be of great use [42,43,47].

In this regard, taking the well-known SRO-based LEC as a central element, it is necessary to have a study of the photonic components available and the characteristics they must have to move forward towards complex applications for SRO\$Si_3N_4$ platform.

## 5. Photonic Elements

The differentiating factor of the technology here presented as compared to other well stablished Si-photonics platforms is the seamlessly integrated SRO-based light emitter. Then, the elements of a Photonic Integrated Circuit must be designed considering its characteristics and requirements.

Straight WG, bends, and couplers and junctions are examples of basic blocks for more complex photonic circuits [48–50].

It is necessary to assure the viability of integrating Silicon nanoparticle-based materials on more complex systems, considering constrains imposed by the SRO/Nitride technology which are different from the C-band currently preferred for communications [44,50]. The material thickness and refractive indexes as those used for the transceiver presented in Figure 7 and reported in Reference [25] can be also used to design more complex elements if the transmission of visible wavelengths in which the LECs emit is assured. Characteristics of the mode transmission and losses can be predicted for different parameters and geometries using diverse theories and tools, including very accurate modern numerical methods and simulation software. This allows to improve the design of the photonic elements in order to assure its adequacy for the specificities of the technology prior to fabrication [48,51].

Figure 9 shows examples of the electric field intensity of the $TE_0$ mode of light with $\lambda$ = 509 nm as it propagates through a bent waveguide (BWG), a tapper and a Y-splitter; and for $\lambda$ = 633 nm in a directional coupler. These are some of the basic photonic structures used for more complex PICs, and all simulations considered a 60 nm-thick $Si_3N_4$ core and 1.5 µm-thick $SiO_2$ cladding, same as the transceiver reported in Reference [25].

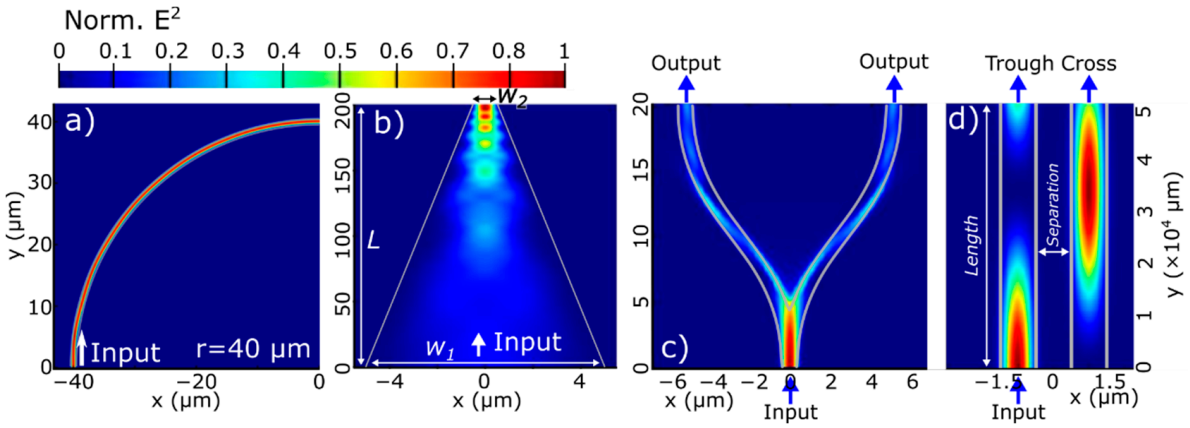



**Figure 9.** Simulations of electric field distribution at the middle of a 60 nm-thick $Si_3N_4$ core with $SiO_2$ cladding for (**a**) a bend with radius of 40 μm; (**b**) a tapper to couple a WG with width $w_1$ = 10 μm to one with $w_2$ = 1 μm; (**c**) Y-splitter, (**d**) Directional coupler. All the results are from FDTD calculations for λ = 509 nm in (**a**–**c**), and for λ = 633 nm in (**d**).

Straight WG exhibit an excellent behavior for most applications, with a mean loss of −0.0003 dB/cm, which is equivalent to ~99.99% of transmission in a 1-cm long WG. However, to keep such low losses, some structures required an important amount of chip area as compared to standard electrical circuits or standard SOI technology (non-seamlessly integrable to photo emitters or detectors). For instance, BWGs (Figure 9a) with a bend radius r = 5 μm (typically used in SOI technology [48]) presented significant losses. In fact, transmittance values were found to be below 65% for radii lower than 10 μm. On the other hand, a 20 μm radius showed that wavelengths below 580 nm present transmission above 95%, while longer wavelengths can be considered poorly transmitted for most applications. Nevertheless, for r = 40 μm, negligible loss across the full LEC emission were observed. Tappers (Figure 9b) used to couple light between waveguides with different widths are also area consuming, since its performance is highly dependent on the of coupling length L. In the case of the proposed technology here, L = 200 μm presented transmission values T > 0.98, indicating low radiation losses or null conversion to higher modes [52]. Regarding Y splitters (Figure 9c), it was found that the power at each output port is around 30% of the total input power, when an ideal of 50% is expected. This is caused by losses due to an unoptimized junction. Techniques, such as parametric optimization or particle swarm optimization [53], can be used to improve this, albeit technological limits, such as the resolution allowed by the lithography or patter transfer methods, must be considered. Directional couplers can be an alternative signal splitter (Figure 9d). In these, the mode being transmitted by a WG can be (partially) transferred to an adjacent one. The amount of transferred power depends on the coupling ratio for a given wavelength, which is dominated by two design parameters: the separation of the adjacent WGs (lower separation, larger mode transfer) and their length (the longest the coupler, the larger the power transfer). For shorter wavelengths, the separation of the WG needs to be smaller, representing a difficulty for visible light as compared to IR, since potentially higher lithographic resolution would be required. The simulations showed that for λ = 633 nm, maximum power transfer is achieved around 3.5 mm for a separation of 1 μm, which can be considered demanding in terms of chip area as compared to the other structures here presented. However, this depends on the desired application, and shorter separations will result in smaller areas.

## 6. Integrated Photodetectors

Important works on the Silicon Photonics portfolio, such as the one by Rahim et al. [44], state that an integrated photodetector is currently not available for silicon nitride platforms. In general, an efficient coupling of the passive photonic elements to photodetectors is also

considered one of the major issues for achieving dense optical integration [14], which adds to the issue of light emitter integration previously discussed.

While it has been shown that the use of an emitter based in Si ncs or nps potentially solves the light source problem, the light-guiding silicon nitride restricts the thickness of the passive elements between 60 nm and 400 nm, adding difficulty to the already complicated issue of coupling of external photodetectors, reverting many of the advantages of light source integration. Then, the monolithic integration of the photodetector is also crucial for the viability of the use of nps-based emitting materials. The generation of visible light by these is in this case an advantage, as it means the light is suitable for photon-electron conversion using bulk silicon. The first works reporting a seamless emitter-transmitter-detector demonstrated photosensing using a simple p-n diode embedded in the support substrate [25,34]. The possibility of using the substrate as detecting layer, apart from being an enormous advantage in terms of CMOS compatibility, eliminates the issue of matching propagation constants of guiding nitride and detecting silicon.

However, the thermal treatments needed for the formation of the embedded nanoparticles have a significant influence in the diffusion of the dopants for p-n junctions, and the resulting affectations to responsivity must be carefully considered. The wide spectrum of the proposed LECs is also convenient in this case, as a sufficient large part of the emitted photons can be absorbed by Si at depths coinciding with the depletion region of the junction [25]. Nevertheless, most of the actual emitted light is not transduced, and there is enormous room for efficiency improvements. Figure 10a illustrates an example of the portion of the spectrum which can be absorbed by silicon within the depletion region of an abrupt p-n junction as the one reported in Reference [25].

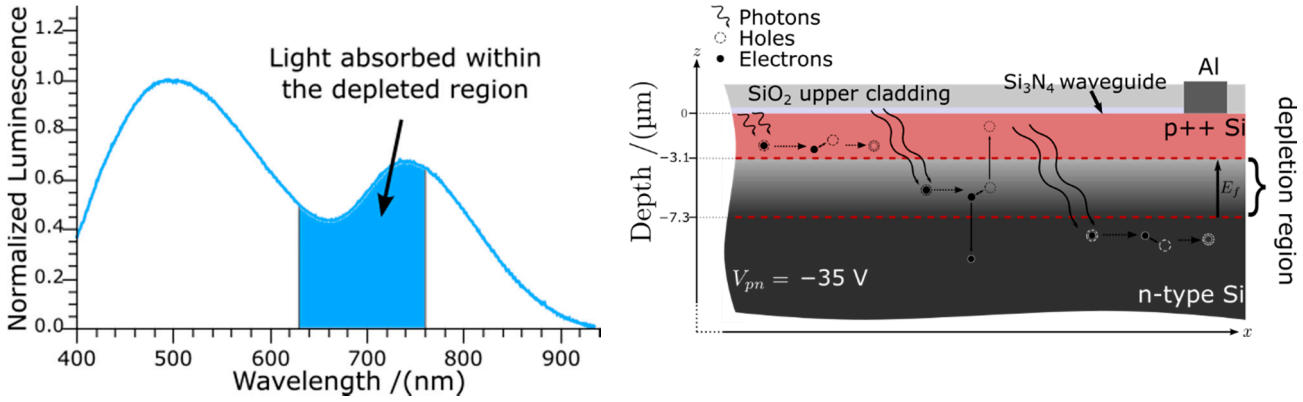



**Figure 10.** (**a**) PL Spectrum of II-SRO. The shadowed portion of the spectrum is what can be absorbed within the depletion region of a p-n photodiode with the parameters detailed in Reference [25] at $V_{pn} = -35$ V; (**b**) schematics of the process of light absorption, e-h pair generation, and separation in the depletion region for a p-n diode with the fabrication parameters as detailed in Reference [25].

In this case, around 23% of the area of the full spectrum will be absorbed within the depletion region of the junction, which is where most of the signal can be converted from photons to photocurrent, as the rest of the photons will generate electron-hole pairs outside of the depletion region, therefore not being separated by an electric field and eventually recombining without contributing to photocurrent. In addition, non-ideal quantum efficiency and other phenomena further reduce the overall efficiency for converting photons into detected electrons. Nevertheless, the combination of integrated sources, visible light, and the use of standard Si-wafers gives a unique opportunity to think outside the box and propose novel approaches to light sensing architectures. In Reference [22], Alarcón et al. suggest concepts taking advantage of conducting the light wherever needed (e.g., directly into the depletion region of a photodiode) and the use of architectures traditionally used

only for electronics, such as a photodetector inspired in a bipolar transistor working in an "backwards" configuration, similar to the Integrated Injection Logic ($I^2L$) [54], but updated and applied to light detection [22].

One promising new approach is the use of silicon nitride simultaneously as optical and electrical material. This is implemented in the Waveguided-sensor (WS) illustrated in Figure 11.

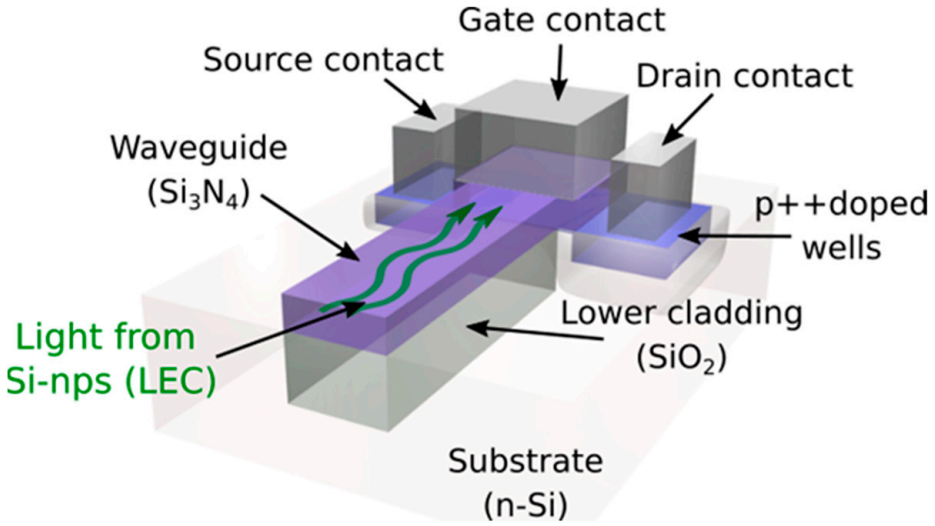



**Figure 11.** Concept of a transistor-like photodetector in which the $Si_3N_4$ waveguide simultaneously acts as dielectric material in a metal-insulator-semiconductor configuration.

In this concept, light from an integrated LEC based in Si-nps is inserted into the waveguide as in the transceptor reported in Reference [25] and illustrated in Figure 7, but, instead of having a regular photodiode at the end, the nitride waveguide acts as the dielectric material in a metal-insulator-semiconductor configuration, in which source and drain regions are also fabricated to generate a transistor-like device. The light is directly guided to the "channel region", where relatively small changes in light power can produce larger changes in gate-source electric current flows, effectively achieving electrophotonic amplification.

This means that current flowing through drain due to photogeneration (i.e., dark current subtracted) $I_{Dopt}$ is larger than what would be possible to obtain by an ideal photodiode with quantum efficiency $\eta = 1$. In an adequate operation point, an electro-optical gain $\beta_{opt} = I_{Dopt}/I_{ph}$ is obtained, where $I_{ph}$ is the number of photons per second multiplied by the charge of the electron.

Figure 12 shows simulation results of $\beta_{opt}$ for a WS with a channel length of 10 μm considering the detection of light with $\lambda = 600$ nm coming from an LEC based on Si-nps.

The simulations of the fabrication process and the resulting device electro-optical behavior show a gain which increases with drain voltage and decreases with optical power is obtained. The full study on this concept is close to publication, but results from simulations confirm that, just as in emitters and photonic elements, there is a fertile field for new possibilities and ingenious architectures for light detection to be developed, thanks to a whole new concept enabled by the possibility of integrating Si-based light sources, ultimately enabled by the synthesis of nanocrystals and nanoparticles in $SiO_2$.

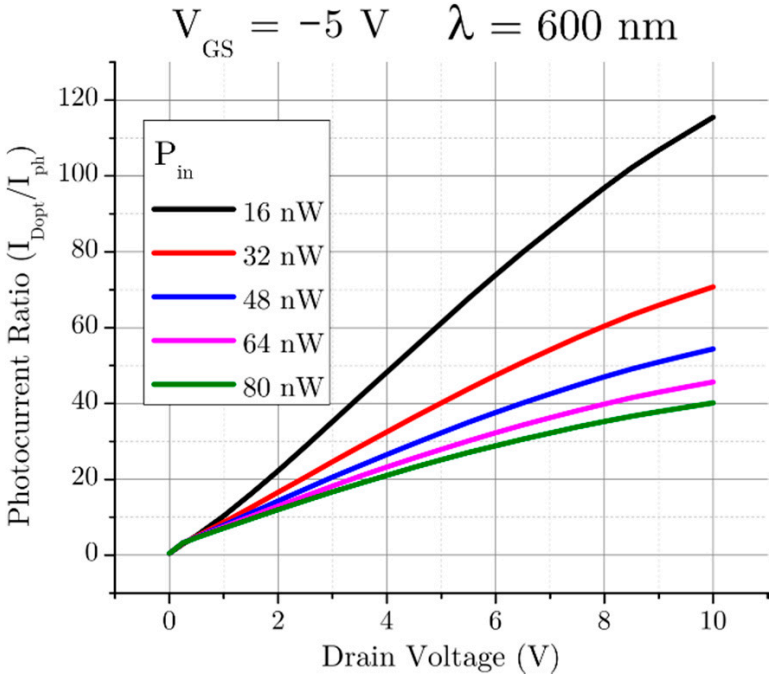



**Figure 12.** Results of simulation for photocurrent gain in the integrated photodetector proposed in Figure 11.

## 7. Discussion

CMOS-compatible materials containing light-emitting silicon nanocrystals or nanoparticles can be obtained by various techniques in which it is possible to tune the emission and conduction parameters. The emitted wavelengths are in the visible range, which is suitable for photodetection by standard bulk Si devices, and transmission by nitride-based light guiding architectures.

The integration of emitters, waveguides and photodetectors built around these materials containing Si nanoparticles has been demonstrated in a monolithic emitter-waveguide-photodiode proof of concept, and new processes and techniques for nitride deposition aim to great improvements confinement of light if required.

Simulations considering the emitted wavelengths, available nitride thicknesses, showed the viability of elemental photonic structures like straight and bent waveguides or tapers, even for very conservative lithographic resolutions. More complicated blocks, such as junctions or directional couplers, were also shown to be viable within this strict technology constrains.

The photonic structures must be optimized for the wavelength of interest λ, which will depend on the specific applications. This can be regarded as an opportunity, since it is a route to filter sections of the broad spectrum emitted by the LECs, avoiding the need for external or more complex filters, and using a single light emitter design for all applications within the visible range. This is particularly useful for sensing and biosensing applications, which in addition, are very well suited for the relatively large areas required by the photonic structures. The pattern transfer resolution significantly influences the required chip area for specific photonic structures. Improved freedom on design can be achieved using novel nitride deposition and high-resolution pattern-transferring techniques. Combining this with the broad luminescence spectra provided by the embedded nps, a wide variety of potential applications with optimized designs can be implemented. Nevertheless, even using relatively low resolutions, the structure features are still within the tenths of microns, which is very well suited for high relevance applications, such as Lab-on-a-chip or other sensing systems.

The proposed platform also showed to tackle the issue of integrated self-coupled photodetectors, offering a variety of innovative architectures enabled by the self-contained seamless integration of all the elements necessary for integrated electrophotonics, taking advantage of the visible range of wavelengths emitted by embedded silicon nanoparticles, as it is suitable for light detection by the bulk silicon used in standard CMOS wafers. A device in which the nitride for the photonic structures is also used as a dielectric in a photodetector is described, showing it presents electro-optic gain for the detection of light with radiant powers in the order of nanowatts, reducing the light emission power requirements for the active materials in integrated emitters. The use of CMOS compatible processes and materials improve the possibilities of monolithically integration of all the elements required for active Photonic Integrated Circuits.

## 8. Conclusions

It has been stablished that a fully monolithic, CMOS compatible, Si-based electrophotonic platform based on SRO/$Si_3N_4$ light emitters directly embedded into $Si_3N_4$ photonic elements is viable. The currently available optical nitride fabrication technology is suitable for the transmission and manipulation of light in a variety of passive photonic elements in the emission range of the nanoparticle-containing material here presented. Already demonstrated monolithically integrated photodetectors, as well as new photo detecting architectures enabled by the monolithic nature of the concept, along with the possibility of integrating electronic circuitry, allow for the exciting development of fully monolithic electrophotonic systems in standard Si-wafers and standard Integrated Circuits fabrication facilities, with potential use in fields ranging from data transfer to laboratory on chip.

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