

Article **Pseudovertical Schottky Diodes on Heteroepitaxially Grown Diamond**

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Abstract: Substrates comprising heteroepitaxially grown single-crystalline diamond epilayers were used to fabricate pseudovertical Schottky diodes. These consisted of Ti/Pt/Au contacts on p[−] Borondoped diamond (BDD) layers (10^{15} – 10^{16} cm^{−3}) with varying thicknesses countered by ohmic contacts on underlying p⁺ layers (10¹⁹–10²⁰ cm^{−3}) on the quasi-intrinsic diamond starting substrate. Whereas the forward current exhibited a low-voltage shunt conductance and, for higher voltages, thermionic emission behavior with systematic dependence on the p^- film thickness, the reverse leakage current appeared to be space-charge-limited depending on the existence of local channels and thus local defects, and depending less on the thickness. For the Schottky barriers $φ_{SB}$, a systematic correlation to the ideality factors n was observed, with an "ideal" $n = 1$ Schottky barrier of $\phi_{SB} = 1.43$ eV. For the best diodes, the breakdown field reached 1.5 MV/cm.

Keywords: diamond; heteroepitaxy; diodes; power electronics; CVD

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1. Introduction

Diamond is a promising material for power electronics and can be applied both in intrinsic form as a dielectric and in doped form as a semiconductor $[1-4]$ $[1-4]$. In particular, its high thermal conductivity would enable the design of electronics with lower cooling requirements and therefore less overall volume [\[5\]](#page-9-2).

Concepts and early demonstrators for diamond devices was already reported quite a while ago, but, especially in the last decade, the development of diamond electronics has begun to gain some momentum, and a great set of devices have been reported, such as Schottky diodes [\[6–](#page-9-3)[10\]](#page-9-4), MOSFETs [\[11–](#page-9-5)[13\]](#page-9-6), FinFETs [\[14](#page-9-7)[,15\]](#page-9-8) or high-voltage power switches [\[16\]](#page-9-9). Most work so far has been conducted on homoepitaxial diamond, i.e., diamond substrates that are usually made by high-pressure–high-temperature (HPHT) synthesis and are, afterwards, overgrown with microwave-plasma chemical vapor deposition (MPCVD), thus introducing functional layers. However, the HPHT method is, when prices should stay within reasonable limits, constricted to substrates with lateral dimensions < 1 cm. While it is possible to merge several HPHT substrates into one bigger piece by mosaic growth [\[17\]](#page-9-10), heteroepitaxial MPCVD growth [\[18\]](#page-10-0), i.e., nucleating and growing diamond on a metal film, is the only method capable of producing wafer-scale (001) substrates so far [\[19\]](#page-10-1).

Over the past few years, a few examples of devices using heteroepitaxial diamond have also been reported: Kawashima et al. [\[20\]](#page-10-2) were, to the extent of our knowledge, the first to report Schottky diodes using diamond grown on $Ir/STIO₃/Si$. A more advanced study applying this system was published by Arnault et al. [\[9\]](#page-9-11). Murooka et al. used diamond grown directly on SiC [\[8\]](#page-9-12), while Kwak et al. used Ir on sapphire as a nucleation substrate [\[21\]](#page-10-3). Sittimart et al. used Ir on yttria-stabilized zirconia (YSZ) on Si for their diodes [\[22\]](#page-10-4), a layer system that, according to finite-element calculations [\[23\]](#page-10-5), should give the best match for large-substrate growth and that has also been used for the largest synthetic diamond so far [\[19\]](#page-10-1). All mentioned diodes had a lateral geometry but, in four cases [\[9,](#page-9-11)[20–](#page-10-2)[22\]](#page-10-4), they can be

classified as pseudovertical since a p⁺ layer was placed underneath the contacting p[−] layer, which means that the current will mostly flow vertically through the p[−] layer and lateral charge transfer will happen through the p^+ layer. To the extent of our knowledge, diodes in which the ohmic contact was placed directly on the $p⁺$ layer have only been realized on homoepitaxial diamond.

The scarcity of realizations using heteroepitaxial diamond is due to the fact that the transfer of overgrowth processes from small HPHT to bigger heteroepitaxial substrates is not fully straightforward since heteroepitaxial substrates usually have strain to some extent [\[24\]](#page-10-6), or the temperature distribution may differ, which both lead to the deformation of the substrates or the formation of defects [\[25](#page-10-7)[,26\]](#page-10-8). In the following, we discuss the properties and limitations of pseudovertical Schottky diodes on our heteroepitaxial diamond substrates.

2. Materials and Methods

The fabrication process is illustrated in Figure [1A](#page-1-0): Ir/YSZ/Si(001) substrates were made on $2^{\prime\prime}$ Si wafers (N++/As) in an Evatec Clusterline sputtering system. After removing the 2 nm native oxide layer by soft Ar ICP etching (inductively coupled plasma), 45 nm YSZ were grown at 1050 K with a 2:1 Ar/O_2 gas mixture and an RF plasma power of 250 W $(4'' Y_{0.15}Zr₀₈₅$ target) following a description by Beshenkov et al. [\[27\]](#page-10-9). Then, 120 nm Ir were grown at 975 K with pure Ar and a DC plasma power of 100 W $(4''$ Ir target) adapting the description by Gsell et al. [\[23\]](#page-10-5).

Figure 1. (**A**): Illustration of the growth process: Dia/Ir/YSZ/Si(001) was grown by BEN and CVD; the resulting substrate was cut into square-shaped pieces and the diamond was separated from the rest of the material. After mechanical polishing, the resulting quasi-intrinsic substrate was overgrown with a p⁺ layer, polished again and overgrown again with a p[−] layer. A tilted mechanical polish allows for access to all layers. The ohmic contact was deposited on the p^+ region, whereas the smaller contacts for Schottky diodes were distributed over the whole substrate. (**B**): Schematic representation of a finished sample. For the characterizations in the further sections, the diodes were indexed by large sectors (SE), small sectors (S) and diode indices (D) within the sectors. The Ohmic contact extends over almost the entire p^+ zone.

Bias-enhanced nucleation (BEN) and initial growth were carried out in a Cornes SDS5200S PECVD reactor with custom adaptations to the sample stage described in pre-vious works [\[28\]](#page-10-10). The BEN was performed at 1050 K with a CH_4/H_2 ratio of 5%, 700 W microwave power and a DC bias of 400 V. The growth into 300 µm thick single-crystalline bulk diamond was performed in an ellipsoid reactor [\[29\]](#page-10-11) at 1100 K and a microwave plasma power of 12 kW using a CH_4/H_2 ratio of 1.7%, 1.5‰ O_2 and 20 ppm N_2 . The nitrogen acts

as growth mediator in the [001] direction, without which, acceptable growth rates cannot be achieved [\[25\]](#page-10-7).

Afterwards, the resulting rough diamond wafers were lasercut into 9 \times 9 mm² squares that were separated from the silicon substrate with KOH. The polishing was carried out in two steps: first, a laserpolishing step was performed in which the roughest features were removed by a commercial laser cutting system. Second, mechanical polishing was applied until a smooth surface was reached. Analysis of the crystals by X-ray diffraction shows rocking curve half-widths of the C004 reflex around 0.35°, which involves contributions from both the high-quality topping layer as well as the lower-quality nucleation zone. Concentrations of N and Si are below the detection limit of secondary ion mass spectrometry (SIMS), but photoluminescence analysis shows a P_1 density, i.e., overall nitrogen concentration, of ca. 8 ppm. Silicon vacancy centers were also observed with varying intensities but could not be quantified.

These quasi-intrinsic diamond squares were then overgrown with another short CVD step, which included a 1.5‰B/C doping ratio at 1100 K with 9 kW resulting in p^+ layers of various thicknesses. After another mechanical polishing step, p[−] layers were deposited at 1100 K with 8 kW. The residual doping of the p- layer stems from the in situ pre-treatment of the p^+ layers with a H_2 plasma prior to growth, and no further boron was added via the gas phase. After that, a tilted polishing step followed, which allowed for direct access to both p-doped layers. In order to remove hydrogen termination from all areas, which would enable surface conductivity [\[13\]](#page-9-6), and to create a well-defined oxygen-terminated surface, all samples were treated with nitrating acid.

On the p^+ region, ohmic Ti/Pt/Au contacts were fabricated by sputtering through a sample-specific handcut shadowmask and subsequently annealing at 1120 K. The Schottky contacts were realized with the identical metal combination with diameters of 100, 150, 200 and 300 µm. They were fabricated via optical laser lithography (Heidelberg Instruments DWL66+), electron beam evaporation and a subsequent lift-off step. In this case, no annealing of the contacts was performed. A schematic end result of this procedure is shown in Figure [1B](#page-1-0). For this tilt geometry, the material was barely polished in the bottom left corner, which is why remainders of truncated pyramids are observed there. If the tilt is parallel to the sample edge, there may also be two unpolished corners. For the characterization, diodes will be referred to as "large sector" (SE), "small sector" (S) and the diode number (D) within the corresponding small sector.

3. Results and Discussion

3.1. Determination of Dopant Concentrations

In order to determine dopant and carrier concentrations, a combination of capacitance– voltage (CV) and SIMS measurements was used. Figure [2A](#page-3-0) shows the CV profile for one diode from a sample as shown in Figure [1B](#page-1-0). From such curves, the profiles of effective acceptor concentrations, N_A - N_D , were extracted by fitting the second derivative of $1/C^2$ with respect to V [\[30\]](#page-10-12). Throughout most of this film, the concentration is in the range of 1.2–1.5 × 10¹⁶ cm⁻³ as demonstrated in Figure [2B](#page-3-0). For lower depths, the concentration increases as we come closer to the p^+ layer.

Boron concentration profiles N_B by SIMS for this particular sample are shown in Figure [2C](#page-3-0),D. The measurement of the p^+ layer taken after the growth, but before the intermediate polishing step, shows a plateau at 4.2×10^{19} cm⁻³. A second SIMS measurement taken after the full fabrication in a different location of the same sample also has a plateau corresponding to the p $^-+$ layer, but, in this case, it is at 5.7×10^{19} cm $^{-3}.$ While SIMS has an uncertainty of 10–20%, this is to some extent an actual concentration inhomogeneity caused by locally different growth rates, i.e., by a late coalescence of the initial crystal grains. As the spectrum in panel C was measured on an unpolished surface, it may be speculated that this also contributed to an uncertainty, but since the plateau is on a rather constant height for lower depths, the influence of this may be negligible. Mild differences in the carrier concentrations determined by the CV measurements of the p^- layers may also be explained

by locally differing growth rates in the p^+ growth since the boron concentration differences from the p^+ layer may be propagated upwards to some extent. When it comes to the overall thickness, SIMS and CV show a decent enough agreement so that no correction factor has to be applied to CV thicknesses.

Figure 2. (**A**): CV measurement for diode SE1S3D11 on a sample (denoted I in Table [1](#page-3-1) below) prepared as shown in Figure [1A](#page-1-0); (**B**): carrier concentration determined from fitting the second derivative of the CV measurement; (C): SIMS after the growth of the p^+ layer before polishing; (D): SIMS at the final stage in one of the least polished locations.

Building on the combined CV+SIMS analysis, the three samples that will be discussed have the specifications given in Table [1.](#page-3-1)

Sample ID	$N_{B,p+}$ (cm ⁻³)	$N_A - N_{D,p}$ (cm ⁻³)
	5×10^{19}	1.4×10^{16}
	7×10^{19}	8×10^{15}
	1×10^{20}	5×10^{14}

Table 1. Key parameters of the three samples referenced in this work

3.2. General Conducting Properties

The current–voltage (I–V) characteristics were investigated for a large set of fabricated diodes. Figure [3A](#page-4-0) shows the I–V curves for all diodes in one SE of sample II. It is rather apparent that there is a grand variety in the conduction behavior, which, especially due to the variety of the p[−] layer thickness that is discussed later, is no surprise for the forward direction, but, in addition, the reverse direction shows a variation in the leakage currents. On this particular sample, no diode has a leakage current below the detection limit; such diodes were only found on sample I.

Figure 3. (**A**): Current–voltage plot for all characterized diodes in SE4 on sample II. If not specified otherwise, a positive voltage will be the forward direction and a negative voltage the reverse direction for all following data; (**B**): TEM model fit for diode SE3S7D1 on sample I; (**C**): correlation of the Schottky barrier *φSB* and the ideality factor n for all investigated diodes on all samples; (**D**): double logarithmic plot for the low-voltage region for a set of diodes on sample II exhibiting an almost linear behavior; (**E**): plot of *RsA* vs. the shunt resistance for all 100 µm diodes on the same sample; (**F**): plot of the leakage current density at -1.5 V J -1.5 for the same diodes exhibiting a linear correlation between low-voltage forward and reverse conduction.

The key parameters of the diodes in the forward direction were determined by fitting the current density J in a voltage region selected for each diode individually with the implicit thermionic emission (TEM) current transport model, including series resistance *R^s* [\[31\]](#page-10-13), which also showed a good agreement for fully vertical diodes on homoepitaxial diamond from our institute [\[10\]](#page-9-4):

$$
J_{TEM} = A^* T^2 e^{-\frac{e\phi_{SB}}{k_B T}} \left(e^{-\frac{e(V - J R_S A)}{nk_B T}} - 1 \right)
$$

in which, $A^* = 90 \text{ Acm}^{-2} \text{K}^{-2}$ is the Richardson constant for diamond [\[32\]](#page-10-14), ϕ_{SB} the Schottky barrier, T is the temperature, A is the diode area and n is the ideality factor. k_B represents the Boltzmann constant and e represents the elemental charge. The first three voltage-free factors may be gathered into one prefactor j_0 . The lower voltage boundary for which this models yields good agreement varies from diode to diode in the range of 0.7–1.1 V, whereas the upper boundary is less fixed. Figure [3B](#page-4-0) shows the fit for one of the best rectifying diodes on sample I with an ideality factor of 1.06, a Schottky barrier of 1.39 eV and a series resistance R_sA of 13.6 Ω cm².

When the *φSB* is plotted against n as shown in Figure [3C](#page-4-0) for all >200 diodes analyzed for this work, a correlation is apparent. The simplest function used to fit this behavior would be of the shape $\phi = \phi_1 n^p$, in which, ϕ_1 would be the ideal barrier at n = 1 that, with the test set used here, would be 1.43 eV, which is within the frame found for our Schottky diodes on homoepitaxial diamond [\[10\]](#page-9-4). In the homoepitaxial work, the data appeared to be following a linear dependence, whereas the exponent $p = -0.54$ would be rather close to a $1/\sqrt{n}$ dependence. If we follow the argumentation by R. Tung [\[33\]](#page-10-15) (see subsections 5.3 and 9.3 therein), the existence of ideality factors \gg 1 and a dependence of ϕ_{SB} on n indicates that the Schottky barrier itself is, to some extent, voltage-dependent. Tung's argumentation was derived assuming a combination of image-force barrier lowering and carrier tunneling; in our case, either the underlying physics or at least the barrier shape changes would have to be attributed to a different effect.

At lower voltages, the curve shows significant deviations from the TEM model. A double logarithmic plot as shown in Figure [3D](#page-4-0) exhibits a mechanism transition just below 1 V forward voltage. The shape is almost linear since the fitting of the double logarithmic graphs yields slopes in the range of 1.1–1.2. Such a behavior indicates the existence of shunt conductance $[34,35]$ $[34,35]$. In the case of our homoepitaxial diodes $[10]$, this had been considered an option, but the low-voltage behavior there had exhibited a better match with a second-barrier mechanism, which, in this case, seemed less fitting.

Relations between the shunt conductivity and other material parameters can be observed. While the series resistance R_sA has no functional correlation to the shunt conductivity as depicted in Figure [3E](#page-4-0), there seems to be some sort of material limit line. This indicates two things: first, the shunt conduction, in principle, occurs via different channels to the conduction at higher voltages, which is dominated by the bulk of the p[−] layer; second, when the shunt conduction channels become powerful enough to cross a certain limit, they prevent the series resistance from developing the potential value, which it would have for a close-to-ideal crystal. While the shunt conductivity has no functional correlation to *RsA*, there is a clear linear relation to the leakage currents as illustrated by Figure [3F](#page-4-0). Therefore, both shunt and leakage conduction probably go through the same channels; a more thorough discussions of the leakage phenomena follows below.

The serial resistance $R_s A$ shows a great variety ranging from 0.03 to 25 Ω cm², but no correlation to any of the other fitting parameters can be found. However, it shows an expectable dependence on the film thickness as shown by Figure [4A](#page-6-0),B: in the regions in which the p[−] layer was partially polished off, it is lower than in the regions in which it remained essentially untouched. A plot of current densities at a random forward voltage would logically exhibit the diametrical behavior.

A mapping of leakage currents at −1.5 V reverse voltage as shown in Figure [4C](#page-6-0) shows no fully systematic behavior with respect to the position. While there are some highly leaky diodes directly at the p−/p⁺ border, there is no systematic decay towards the thicker p⁻ layer, but there are randomly distributed local maxima in all areas of the sample. For the larger diameters, the occurence of highly leaky behavior seems to be more abundant. This indicates that the leakage current is not determined by the thickness or a potential surface conductivity by eventual incomplete hydrogen removal, but rather by local defects. It has to be stated that the incompletely polished regions in the sample corners must not be considered as defected in this regard since no outstanding leakage phenomena were observed in these areas.

Therefore, we looked deeper into the leakage phenomena. Figure [5A](#page-7-0) displays the leakage current density for two formally similar diodes, which shows a substantially higher J for the upper diode SE1S3D7, which is formally further away from the p^+ region. The obvious reason for this can be found in the micrograph: this diode is located over the boundary of a penetration twin. These entities often occur in the growth of heteroepitaxial diamond as we have discussed in previous works [\[25](#page-10-7)[,36\]](#page-10-18). Their incoherent boundary is

a good channel for leakage current to go through. Such twins were also reported in the work by Sittimart et al. [\[22\]](#page-10-4), leading to similar issues. It is obvious that the growth requires further optimization in order to get rid of these channels.

Figure 4. (**A**): Interference contrast micrograph of SE1 + SE2 sample III. The red line roughly marks the border at which the p^+ and p^- regions are exposed after the polishing. The x markers correspond to the markers in panel C. (**B**): Mapping of *RsA* for all diodes measured on this sample with a clear thickness dependence; the arrangement on the chart exactly matches the arrangement of the diodes above. (**C**): Mapping of leakage current densities at −1.5 V reverse voltage showing no systematic regional dependencies.

Figure 5. (**A**): Comparison of two diodes from sample III, where the upper diode on the penetration twin has a much stronger leakage current despite being further away from the p^+ region; (**B**): temperature-dependent leakage current density measurements of one of the diodes on sample II with a low-voltage ohmic regime and a space-charge regime at higher voltages; (**C**): breakdown measurement for the diode on sample I from Figure [3B](#page-4-0).

In our previous work [\[25\]](#page-10-7) we also discussed the appearance of other defects, such as (111) stacking faults or edge-type 1/2[100]|(100) threading dislocations. Particularly for the latter, it is often speculated that they may locally harbor $sp²$ hybridized carbon moieties, which would be a good candidate for promoting enhanced vertical electrical transport, causing a higher level of the leakage current.

We also checked the conduction mechanism of the leakage: as Figure [5B](#page-7-0) shows, there is a transition. The slope in the double logarithmic plot is ca. 1 for low voltages and transitions to values of around 2 at a certain point. Such behavior is typical for space-charge limited conduction [\[37](#page-10-19)[,38\]](#page-10-20). We also checked at higher voltages whether a transition to a trap-filled behavior occurs, which would have a characteristic temperature dependence, but we did not observe that.

Finally, for sample I, which is the only one that has diodes without any detectable leakage current at low voltages, breakdown measurements were performed. For the longest-lasting diodes, a breakdown curve as shown in Figure [5C](#page-7-0) was obtained. Since there is no hard breakdown, a well-defined breakdown voltage is hard to assign, but the increase at 105 V, which also marks the crossing of the 1 $A/cm²$ mark, can be seen as a reasonable assignment for the breakdown voltage V_{BD} of this particular diode. If this diode would actually be operated, 60 V would probably be the maximum recommendable voltage. At the location of this particular diode, the p[−] layer is ca. 0.7 μ m thick, which yields a breakdown field of 1.5 MV/cm, which would be similar to the value reported by Kwak et al. [\[21\]](#page-10-3). With these measurements, it is also possible to calculate a Baliga Figure of Merit [\[39\]](#page-10-21) BFOM = $V_{BD}^2/(R_sA)$ of 810 W/cm², which, of course, is still much below any value of recent works for homoepitaxy. In addition, at the moment, such a behavior is only observed for the best analyzed diodes, while many already exhibit significant leakage between 20 and 50 V.

Therefore, it is an obvious objective to reach a decent breakdown field for the majority of diodes instead of the current fraction. It would also be desirable to increase the layer thickness in order to reach higher absolute breakdown voltages. Since our growth parameters involve a fast growth in the [111] direction, pre-existing penetration twins with a topping (111) facet will outgrow the rest of the material very fast. In order to move to more advanced devices, eliminating these twins at an earlier growth stage is also a requirement.

4. Conclusions and Outlook

We have demonstrated the fabrication of pseudovertical Schottky barrier diodes based on heteroepitaxially grown diamond substrates. In-depth characterization were undertaken with respect to diode characteristics, such as rectification and breakdown voltage, which, for the best diodes, reached suitable values. Shunt conductance in the forward direction and associated leakage in the reverse direction could be related to crystal defects such as twins and boundaries.

While the first functional devices have been successfully implemented, future efforts are needed for the improvement of the underlying material properties. Besides the reduction in impurities and defects, novel processes will be implemented. A scalable technology could proceed via etching for contacting the p^+ layers instead of the tilted polishing step. Once that is achieved, targeting more sophisticated devices will be enabled in the future.

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Abbreviations

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