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Channel Mobility Model of Nano-Node MOSFETs Incorporating Drain-and-Gate Electric Fields

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Abstract: A novel channel mobility model with two-dimensional (2D) aspect is presented covering the effects of source/drain voltage (V_{DS}) and gate voltage (V_{GS}), and incorporating the drift and diffusion current on the surface channel at the nano-node level, at the 28-nm node. The effect of the diffusion current is satisfactory to describe the behavior of the drive current in nano-node MOSFETs under the operations of two-dimensional electrical fields. This breakthrough in the model's establishment opens up the integrity of long-and-short channel devices. By introducing the variables V_{DS} and V_{GS}, the mixed drift and diffusion current model effectively and meaningfully demonstrates the drive current of MOSFETs under the operation of horizontal, vertical, or 2D electrical fields. When comparing the simulated and experimental consequences, the electrical performance is impressive. The error between the simulation and experiment is less than 0.3%, better than the empirical adjustment required to issue a set of drive current models.

Keywords: channel mobility; drift current; diffusion current; nano-node process; device model; MOSFET

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1. Introduction

In conventional device models for metal-oxide-semiconductor field-effect transistors (MOSFETs), the drive current (ON current) [1,2] mainly considers the moving carriers with the drift effect, as shown in Figure 1a. Due to this simple assumption, the pseudo-ideal device models can easily and quickly be assigned to the design houses. For the long-channel devices, this strategy is commercially acceptable. As the channel length of a MOSFET decreases, the saturation current of MOSFETs increases with the increase in the drain voltage or decrease in the channel length, which is known as channel length modulation [3–5] or velocity overshoot [6–9]. However, the proposed conduction mechanisms do not seem to entirely fit the physically measured current-voltage results. The device models in semiconductor foundries usually assist in making an empirical adjustment to compensate for this drawback, but have no physical meaning. Previously, a new concept incorporating the diffusion effect at each channel point was proposed due to the gradient of inversion charge density, especially near the pinch-off point [10]. At this pinch-off point, the inversion charge density approaches zero, indicating zero drift current, but the real drive current is not zero.

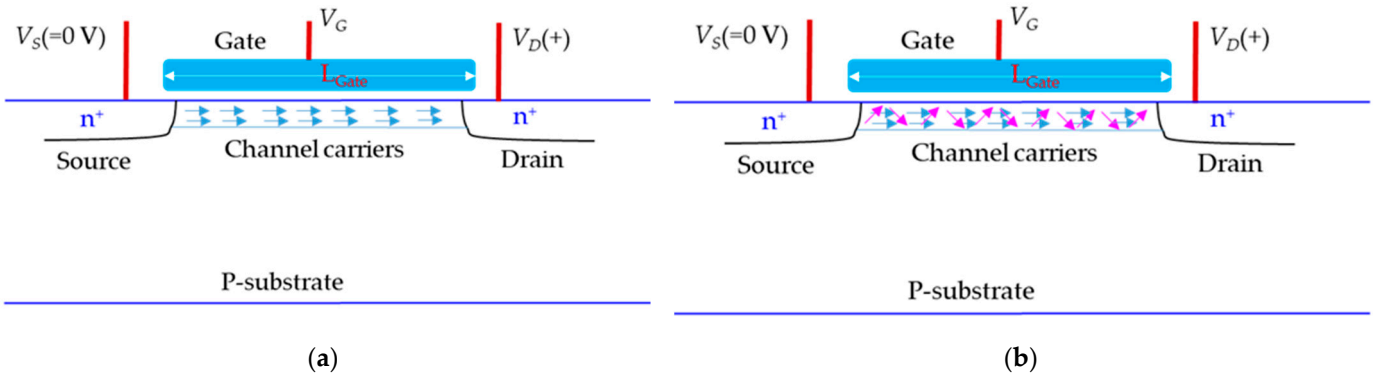

Figure 1. Channel carrier conduction due to drift effect in n-channel MOSFET (nMOSFET): (**a**) without gate bias or with smaller gate bias, and (**b**) with gate bias as a variable for long-channel device.

As a result, the drive current rises as the drain voltage increases for a nano-scale MOSFET. Adding the diffusion effect to the drive current model, the contribution of the diffusion current to the entire drive current is distinctly enhanced, especially in the current behavior of short-channel devices [11,12]. In other words, a larger source/drain voltage V_{DS} will make a larger gradient of inversion charge density, causing a larger surface diffusion current. However, as the V_{GS} was fixed, the previous work [11] only changed one parameter (V_{DS}), in long- or short-channel devices, to fit the equivalent mobility μ_{eq} accurately. The previous work treated it as a one-dimensional (1D) issue. In terms of the real operation of MOSFETs, the electrical field with gate bias V_{GS} still and strongly influences the channel mobility dominating the drive current. Thus, it is necessary to give this deeper consideration, modulating all the parameters (V_{DS}, V_{GS}, and L_{mask}) at once to fully satisfy the μ_{eq} correlated to the V_{DS}, V_{GS}, and channel length on drawn mask L_{mask}. Moreover, by consolidating the adjustment of V_{DS} and L_{mask} correlated to the horizontal electric field and V_{GS} influencing the vertical electric field, the drive current of MOSFETs can be more meaningful and beneficial in providing a set of accurate nano-node device models, especially beyond 28-nm node fabrication or entering 3-nm node processes [13–16]. The gate bias, which conducts the moving carriers in the channel, induces more carrier scattering, especially in surface roughness. This paper presents a 2D investigation, as shown in Figure 1b.

Furthermore, the dielectric gate in this work was a sandwich stack of high-k (HK) materials $HfO_x/ZrO_y/HfO_z$ [17–20] deposited with atomic layer deposition (ALD) technology [21–23]. The physical thickness deposited with ALD technology was about 2.4 nm. The gate electrode was made of low-resistance aluminum, also called a metal gate (MG) [24,25], as shown in Figure 2, where L_{Gate} is the real gate length on the wafer. ΔL_E is the error of L_{mask} and L_{Gate}. L_{OL} is the overlap difference of L_{Gate} and the end of the n^- doping region at the source site. L_{met} and L_{Dep} are the distances between both n^- regions and the depletion width due to the V_{DS} bias. L_{Real} equivalent to ($L_{met} - L_{Dep}$) is the really effective inversion channel length. The orders of p-well, n^-, and n^+ in doping levels with unit $1/cm^2$ are 13, 14, and 15, respectively. The physical extraction and fitting metrology of equivalent channel mobility is demonstrated in Section 2. The measurement and simulation characteristics of drive current for long-and-short channel MOSFET devices are illustrated in Section 3. The discussion of this equivalent mobility model in precision investigation and the possible extension applications beyond the 28-nm node is demonstrated in Section 4. In the end, we did a conclusion in Section 5.

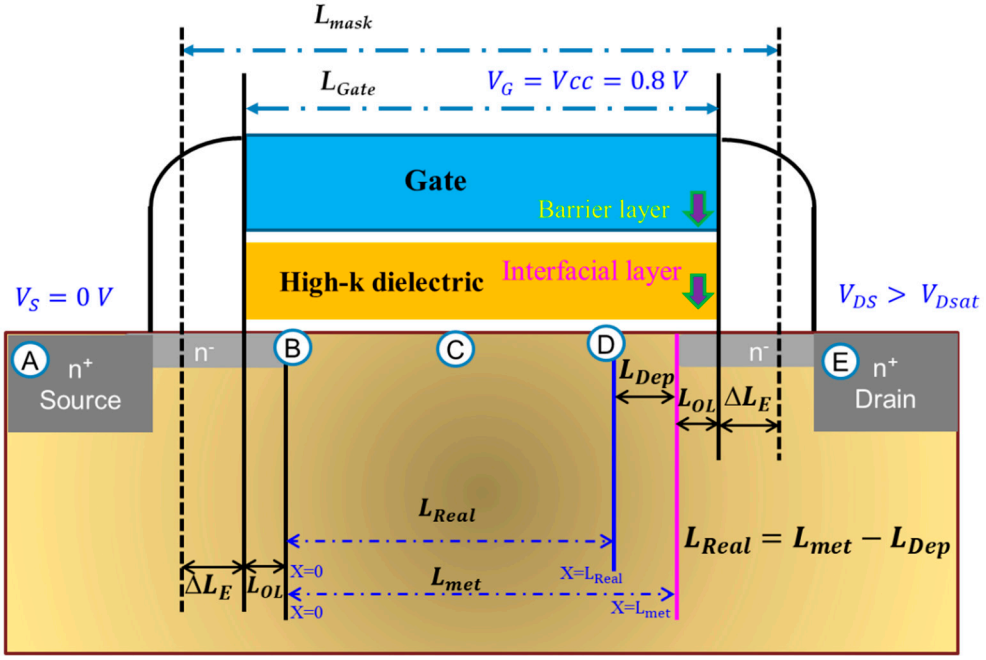

Figure 2. Schematic cross-section diagram of an nMOSFET with the definition of channel lengths.

2. Experimental and Mobility Fitting

Based on the previous work [11], five checking points ***A***, ***B***, ***C***, ***D***, and ***E***, as shown in Figure 3, were utilized to expose the carrier mobility $\mu(x)$ and the drift current (see Figure 3), where $\mu(x)$ was the function of the position x in the surface channel and the range of position x was from point ***B*** to point ***D***. However, it was not enough to describe the whole behavior of an equivalent mobility μ_{eq} correlated to V_{DS}, V_{GS}, and L_{mask}, independent of position x.

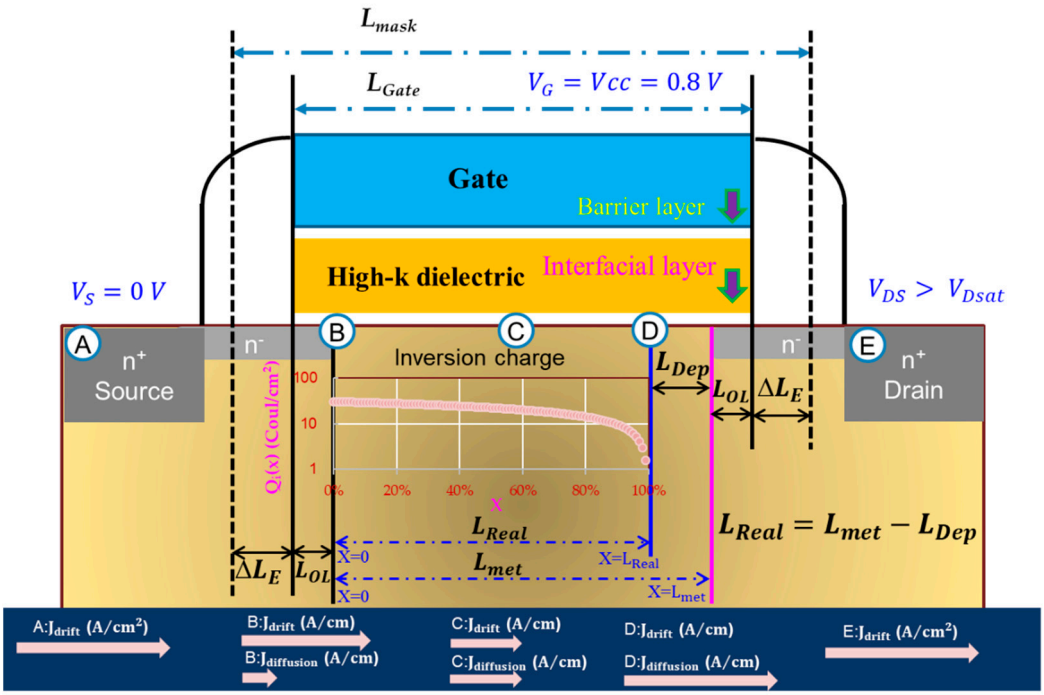

Figure 3. Distribution of inversion charge from checking points ***B*** to ***D***.

We incorporated various conditions with V_{DS}, V_{GS}, and L_{mask} to reasonably describe the whole drive current and fit μ_{eq} in Equations (1)–(6),

$$I_{\text{Drift}} = WQ_i(x)v_d(x) \tag{1}$$

$$I_{\text{Diff}} = D_n W \frac{dQ_i(x)}{dx} \tag{2}$$

$$\text{where } D_n = \mu_{eq}\frac{kT}{q} \tag{3}$$

$$I_{\text{total}} = I_{drift} + I_{diff} \tag{4}$$

$$\frac{I_{\text{total}}}{W} = -Q_i(x)v_d(x) + D_n\frac{dQ_i(x)}{dx} \tag{5}$$

$$\frac{I_{\text{total}}}{W} = \frac{\mu_{eq}E_{ast}Q_i(x)\frac{dQ_i(x)}{dx}}{mc_{ox}E_{ast} + \frac{dQ_i(x)}{dx}} + D_n\frac{dQ_i(x)}{dx} \tag{6}$$

where $Q_i(x)$ is the inversion charge at position x with unit Coulomb/cm^2, q is the unit charge, W is the channel width, v_d is the carrier drift velocity, D_n is the diffusion coefficient of the electron carrier, E_{sat} is the horizontal electric field at saturation, k is the Boltzmann constant, T is the absolute temperature, and m is the body factor.

Under specific conditions, such as fixing a channel length and tuning the gate voltages to sense the $I_{DS} - V_{DS}$ characteristics, the relationship between μ_{eq} and the drain bias can be derived, as shown in Figure 4. When changing the fixed channel length and the drain bias, the drain current conducted at the linear or saturation region is obviously represented for any tested channel device. We seek to accurately determine the relationship between the μ_{eq} and these three parameters, V_{DS}, V_{GS}, and L_{mask} to establish a set of more precise device models for high-end design customers. Considering these measurement results, the equivalent mobility should contain the drift and diffusion effects and the contributions of both have usually changed at position x. In this work, there were four separate sections (*a*, *b*, *c*, *d*), illustrating the long-and-short channel devices and the split of electrical characteristics at linear and saturation regions as L_{mask} = 120 nm. Under a series of tested devices, L_{mask} = 0.033, 0.05, 0.09, 0.12, 0.5, and 1 µm when the channel width was fixed as W = 10 µm. Two distribution trends of equivalent mobility were seen, related to the V_{DS} and V_{GS} variables. Choosing this device as a dividing crest was similar to the observation of a roll-off effect of threshold voltage in the pilot-run stage. The classification of electrical measurement is demonstrated at Table 1.

Table 1. Four separated sections are classified as long-short devices and linear-saturation regions.

Channel Length	Operation Mode	Section
Long (>120 nm)	Linear region	X = *a*
Long (>120 nm)	Saturation region	X = *b*
Short (<120 nm)	Linear region	X = *c*
Short (<120 nm)	Saturation region	X = *d*

First of all, μ_{eq} is written as a function of V_{DS} in terms of different V_{GS} at a fixed L_{mask}, which is described by a third-order polynomial using Taylor's expansion in Equation (7), where X_i is the coefficient of the ith polynomial with i = 0, 1, 2, 3.

$$\mu_{eq}(V_{DS}) = \sum_{i=0}^{3} X_i \times (V_{DS})^i \tag{7}$$

X is attributed to each section (a, b, c, or d). X_i is strongly related to the gate voltages as L_{mask} is fixed. This is given in Equation (8) by using Taylor's expansion, where X_{ij} is the coefficient of V_{GS} polynomials with j = 0, 1, 2, 3.

$$X_i(V_{GS}) = \sum_{j=0}^{3} X_{ij} \times (V_{GS})^j \quad (8)$$

Ultimately, if the impact factor L_{mask} to the coefficient X_{ij} is observed, it can be entirely represented as Equation (9), where X_{ij} is the coefficient of the L_{mask} variable with k = 0, 1, 2.

$$X_{ij}(L_{mask}) = \sum_{k=0}^{2} X_{ijk} \times (L_{mask})^k \quad (9)$$

The flow charts of the X-coefficients in the simulation and the μ_{eq} values in the extraction are demonstrated in Figures 5 and 6 with section $X = a$ as an example, respectively. The other sections in the parameter extraction also follow the same procedures to determine accurate μ_{eq} values correlated to the V_{DS}, V_{GS}, and L_{mask} variables. Table 2 exhibits the whole relationship between parameters and X-coefficients. After extracting the equivalent channel mobility and replacing it into Equations (5) and (6), the inversion charge $Q_i(x)$ can be quantitatively achieved and exhibited in the central zone of Figure 3.

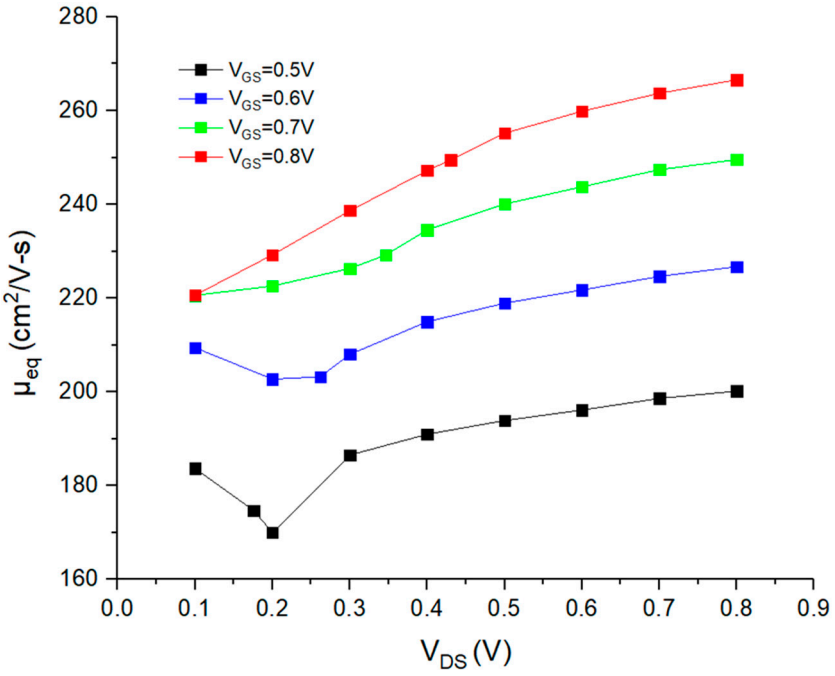

Figure 4. μ_{eq} vs. V_{DS} characteristics under different V_{GS} at L_{mask} = 500 nm in section X = a.

Table 2. The relationship between each parameter and the coefficient in Taylor's expansion.

Coefficient Type	Variables X_i, X_{ij}, and X_{ijk}	Index Range
μ_{eq} (V_{DS})	X_i: functions of V_{GS}	i = 0, 1, 2, 3
X_i (V_{GS})	X_{ij}: functions of L_{mask}	j = 0, 1, 2, 3
X_{ij} (L_{mask})	X_{ijk}: fitted constant	k = 0, 1, 2

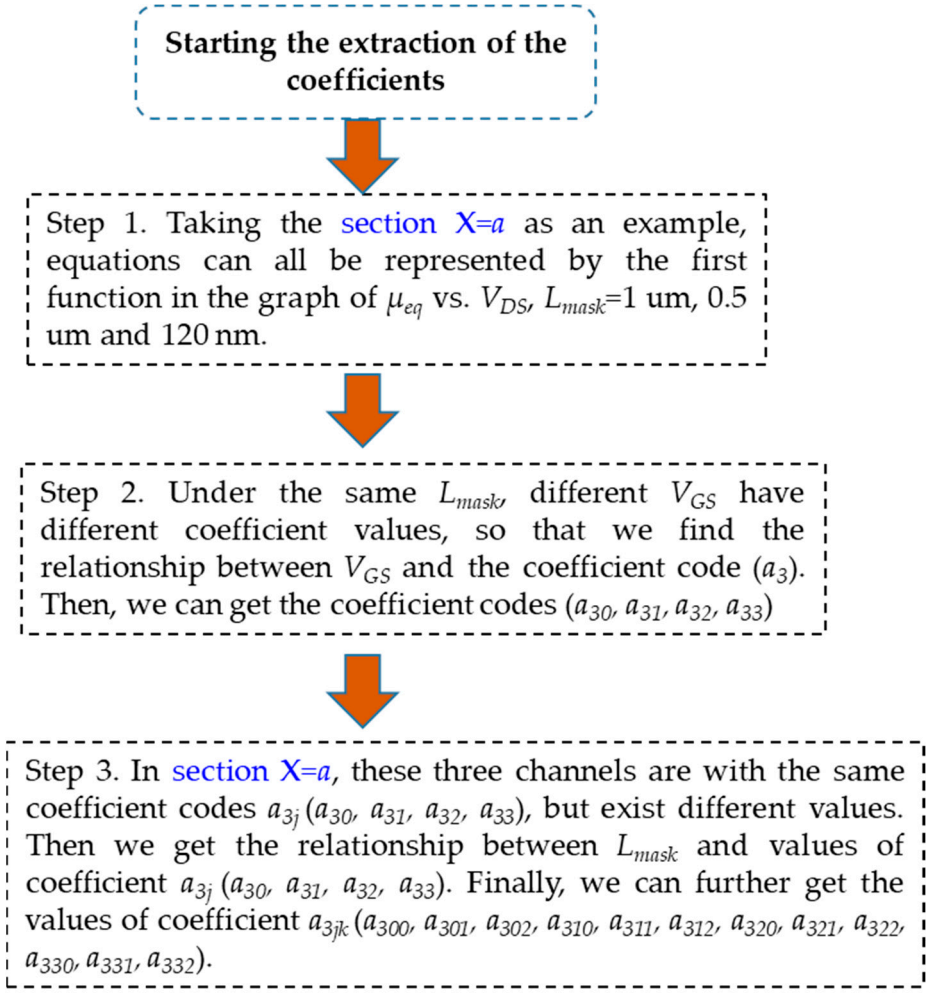

Figure 5. Flow chart for extracting the coefficients of X_i and X_{ij}, in section $X = a$.

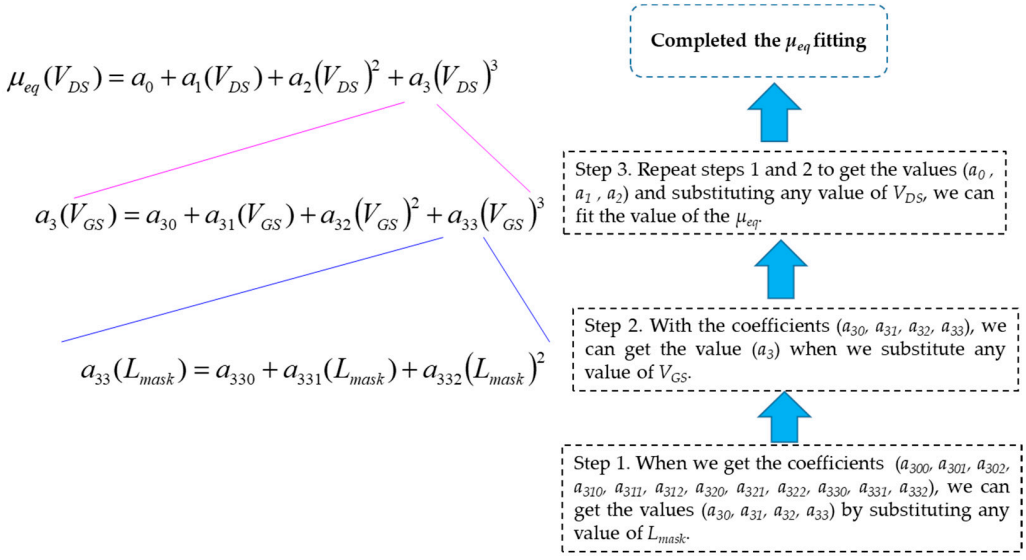

Figure 6. Fitting the coefficients of μ_{eq} in section $X = a$ as an example. On the left-hand side, the expansion relationship between a_3 and a_{33} is illustrated.

3. Results

Following the previous flow charts to obtain the coefficients of X_i, X_{ij}, and X_{ijk}, the $\mu_{eq}(V_{DS}, V_{GS}, L_{mask})$ at a variable perturbation could be effectively and meaningfully extracted. The equivalent mobility was immediately substituted into Equation (5) to simulate the corresponding drive current. The simulated and experimental results of curves I–V with long-and-short channel devices are shown in Figure 7a–d.

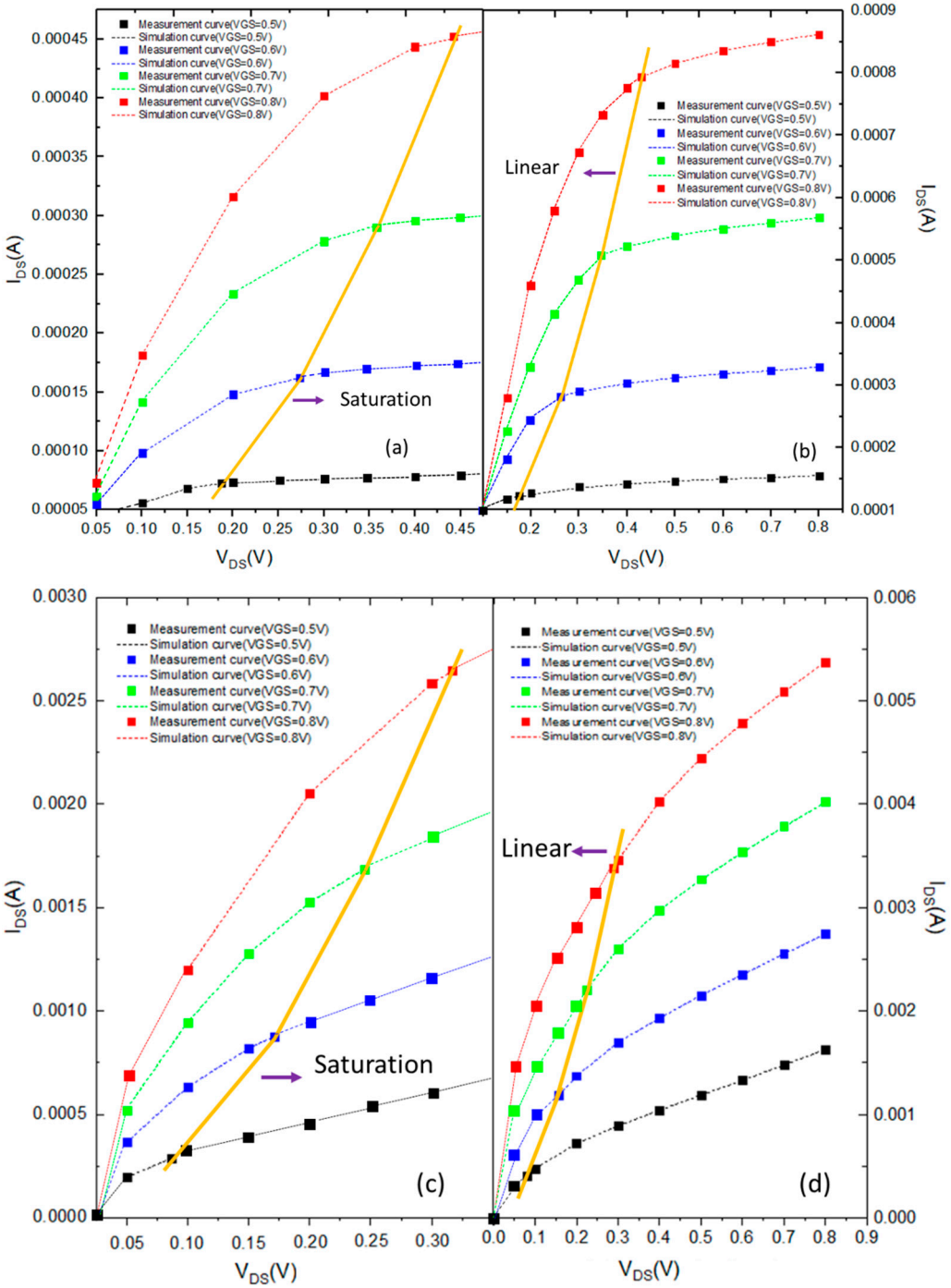

Figure 7. I_{DS} vs. V_{DS} curves for long-channel devices: (**a**) at L_{mask} = 1 µm in section $X = a$, and (**b**) at L_{mask} = 500 nm in section $X = b$; for short-channel devices: (**c**) at L_{mask} = 50 nm in section $X = c$, and (**d**) at L_{mask} = 33 nm in section $X = d$. The yellow lines mean the pinch-off boundary at $V_{Dsat} = V_{GS} - V_T$, where V_T is the threshold voltage.

For precise observation of the contribution of μ_{eq} correlated to V_{DS}, V_{GS}, and L_{mask}, one three-dimensional (3D) plot was established, as shown in Figure 8, incorporating all of these extracted data linked as lines and extending these lines as a continuous plane.

In this work, the tested channel-length devices were 33, 50, 90, 120, and 500 nm, as well as 1 µm. When the channel length L was greater than 120 nm, the section was defined as a long-channel section. Thus, the plot in Figure 8a with L = 500 nm is a long-channel section and L = 33 nm is a short-channel one. The equivalent mobility of the other devices with V_{DS} and V_{GS} variables are exhibited in Figure 8b–e. Furthermore, the V_{DS} and V_{GS} we sensed range from 0.1 to 0.8 V and from 0.5 to 0.8 V with a step voltage 0.1 V, respectively. The error between simulated and real measurement data is less than 0.3%, no matter what channel-length devices and whether there is a linear or saturation region operation mode. Table 3 provides an example of extracting the coefficients in section $X = a$ under V_{GS} = 0.8 V and L_{mask} = 500 nm.

Table 3. The values of the coefficients in section X = a under V_{GS} = 0.8 V and L_{mask} = 500 nm.

Coefficient Value	Extracted Sub-Coefficients
The value of a_3	$a_3 = -247.999$
The values of a_{3j}	$a_{33} = 19{,}833.33$
	$a_{32} = -5150$
	$a_{31} = -29{,}383.3$
	$a_{30} = 16{,}400$
The values of a_{3jk}	$a_{332} = -3{,}283{,}858.592$
	$a_{331} = 5{,}452{,}922.151$
	$a_{330} = -1{,}885{,}663.094$
	$a_{322} = 6{,}422{,}679$
	$a_{321} = -10{,}725{,}100.45$
	$a_{320} = 3{,}751{,}730.477$
	$a_{312} = -4{,}094{,}362.073$
	$a_{311} = 6{,}889{,}789.134$
	$a_{310} = -2{,}450{,}687.382$
	$a_{302} = 840{,}872.7189$
	$a_{301} = -1{,}430{,}708.191$
	$a_{300} = 521{,}535.9158$

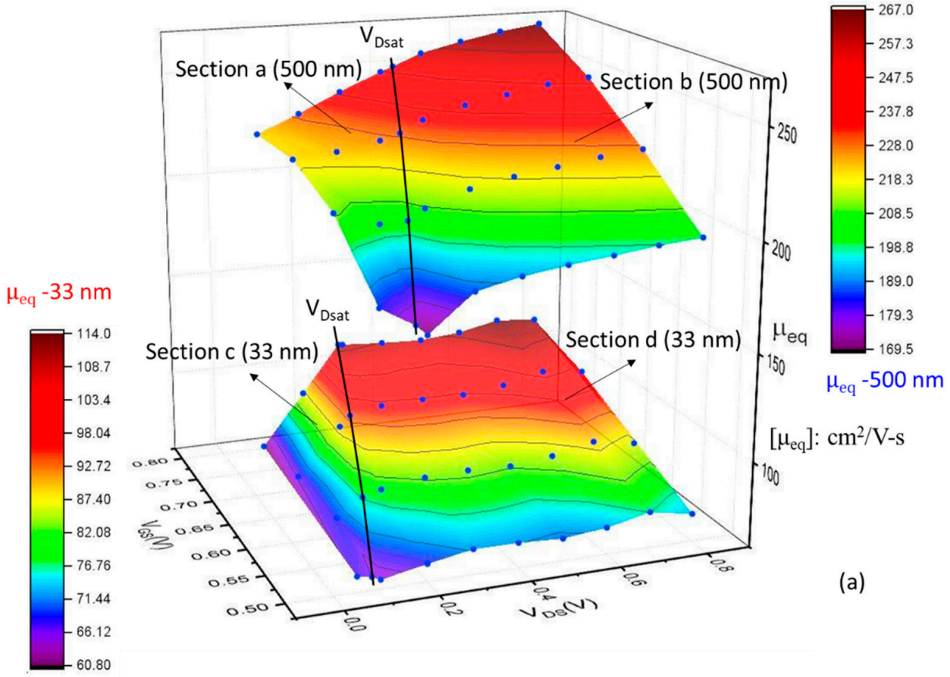

Figure 8. *Cont.*

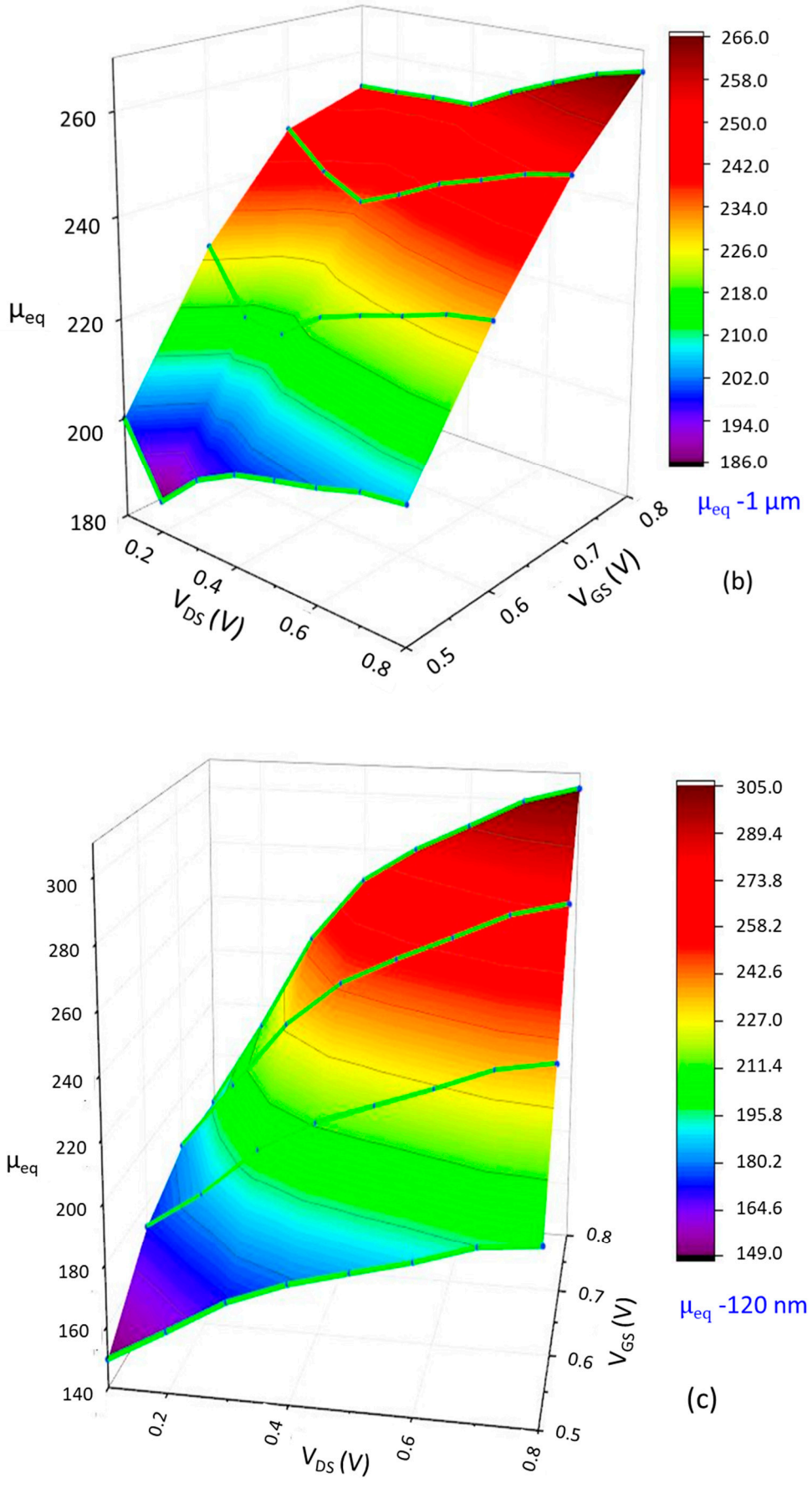

Figure 8. *Cont.*

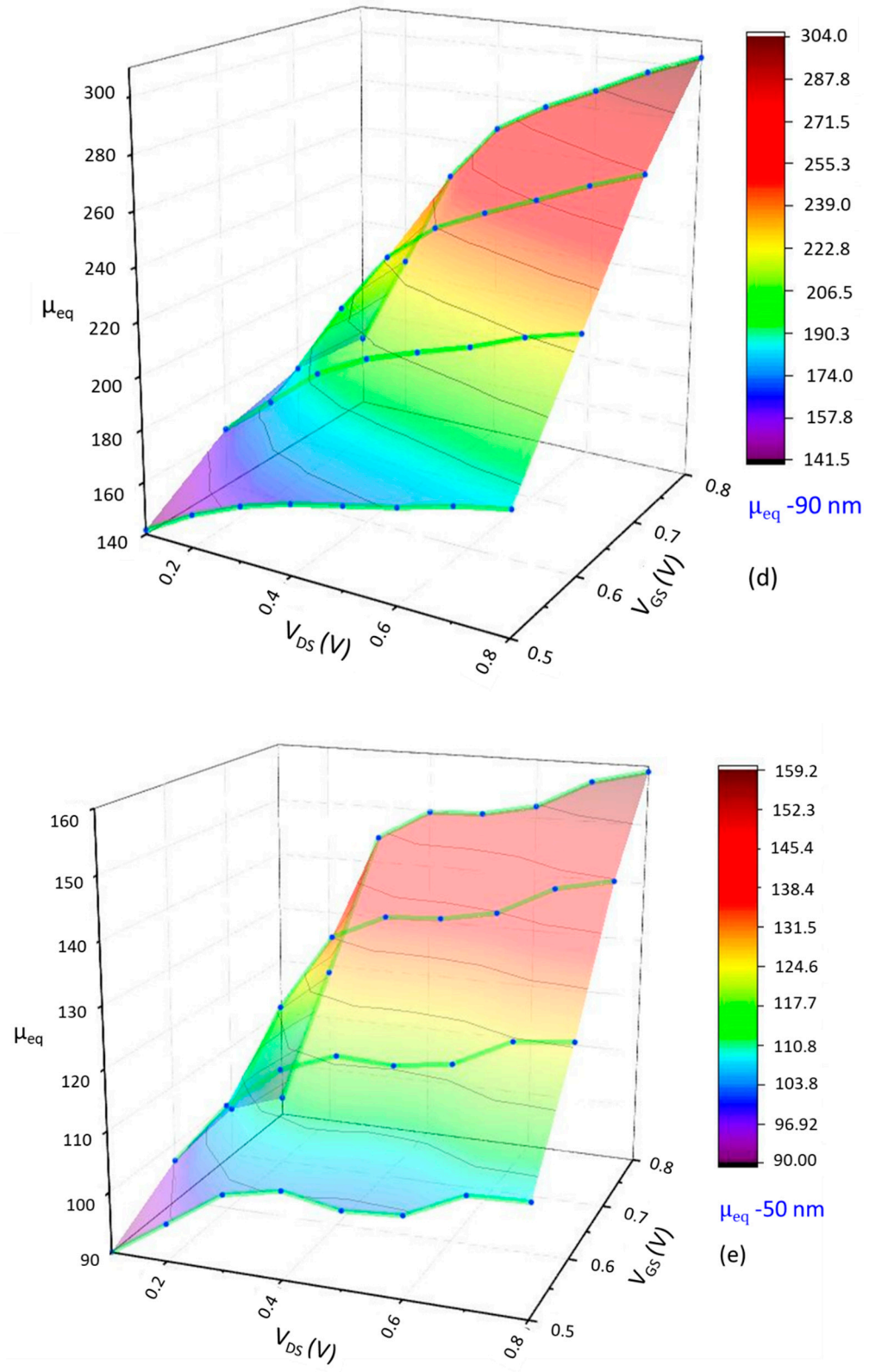

Figure 8. Three dimensions of μ_{eq} versus V_{DS} and V_{GS} at: (**a**) L_{mask} = 500 nm (long-channel) and 33 nm (short-channel), (**b**) L_{mask} = 1 μm, (**c**) L_{mask} = 120 nm, (**d**) L_{mask} = 90 nm, and (**e**) L_{mask} = 50 nm.

4. Discussion

For 1D model of MOSFET, it was developed in the late 1960s [26]. Nevertheless, including the vertical field V_{GS} factor to promote the accuracy of device models for high-

performance-computing (HPC) IC products is less exposed, especially in deep nano-node logic devices. This benefit is similar to silicon purification. If the wafer is metallurgic-grade silicon, the purity is about 98–99% [27], applied to solar panels. However, as the purity is enhanced to 99.9999999%, treated as electronic-grade silicon, this silicon material can be applied to submicron or nano-node wafers to form advanced performance ICs. In Huang's team [11], the device performance could achieve simulated and physical measurement data errors of around 1–2%. This kind of device model essentially satisfies most of the design houses in nano-node manufacturing. However, considering the lower power consumption and higher electrical performance needed for some advanced products, it seems the device model should be more precise. Here, considering the gate-field variable and interaction with V_{DS}, the error was fantastically reduced to 0.3% or below, which meant the accuracy in simulation reached 99.7% or more. Generally, this accuracy was sufficient to fit the requirements of HPC products with planar MOSFETs. In Figure 8, as V_{DS} increases, μ_{eq}(x) is also increased, but not linearly. This phenomenon is also observed as V_{GS} increases. As the gate field increases, the entire channel field also increases. Hence, the equivalent mobility is increased, no matter what the increase in gate voltage or drain voltage. However, the threshold voltage V_T is not a constant as the V_{DS} is scanned from 0 to Vcc (=0.8 V). Due to this effort, compared with the conventional method treated V_T as a constant, this equivalent mobility model provides a more precise consequence. The range of V_T extracted with constant current metrology is from 0.296 to 0.271 V as V_{DS} set from 0.05 to 0.8 V at L_{mask} = 1 µm. The drain-induced barrier lowering (*DIBL*) value defined as $(V_{T\_lin} - V_{T\_sat})/(\mathrm{Vcc} - 0.05)$, a good index to expose the short-channel effect, is 33.36 mV/V, where V_{T_lin} is the threshold voltage at the linear region and V_{T_sat} at the saturation region. All of *DIBL* values in these tested devices are shown at Table 4. The *DIBL* values are increased and, in the meanwhile, the short-channel effect is more significant. In addition, while the V_{GS} is lower and the I_{DS} characteristics are located at the linear region, the equivalent mobility decreases due to the contribution of scattering effect of channel surface roughness, as shown in Figure 4. Thus, as the V_{DS} increases, the μ_{eq} decreased distinctly until at the pinch-off point $V_{DS} \approx V_{GS} - V_T$. However, as V_{DS} increases more, entering the saturation region, the conducted carriers gain more energy and the moving speed of the carriers increases. Thus, the μ_{eq} increases. Furthermore, as the V_{GS} is increased, the channel depth of inversion charge is also increased. Most of the conducted carriers in channel choose the low-resistant path. Therefore, the contribution ratio of channel surface scattering effect is slightly reduced. The sunken phenomena are gradually unapparent as the V_{GS} is increased.

Table 4. The *DIBL* effect with different channel lengths.

L_{mask}	V_{T_lin} (V)	V_{T_sat} (V)	*DIBL* (mV/V)
1 µm	0.296	0.271	33.36
500 nm	0.307	0.277	39.01
120 nm	0.332	0.298	46.12
90 nm	0.353	0.306	62.87
50 nm	0.395	0.305	120.38
33 nm	0.384	0.228	208.09

Continuously, establishing a full model incorporating the diffusion and drift effects is a huge challenge. The alternative, describing the equivalent mobility related to V_{GS} and V_{DS} with a linear relationship, is also tough. In the short-channel device, the difference of equivalent mobility between sections $X = c$ and $X = d$ can be up to 54 cm^2/V-s. For the long-channel device, the maximum difference between the two sections is around 97 cm^2/V-s. The minimum difference between linear sections $X = a$ and $X = c$ is about 109 cm^2/V-s. However, the maximum difference at these two saturation sections is approximate 153 cm^2/V-s. These interesting values are beneficial to the establishment of device models or to process improvement if needed.

The distribution of inversion charge coming from the drift effect under checking points ***B*** to ***D***, with a percentage variation related to position x, is shown in Figure 3. The inversion charge is not uniform in each position, and the diffusion current is turned on as the drain voltage is triggered. Thus, the inversion charge with a log scale at $x = 0$ is not 100%. This consequence opportunely reflects the equivalent mobility contributed by the drift and diffusion effects similarly to a leverage. However, the drift effect at the smallest channel-length device is unapparent, and the diffusion effect is dominant, similarly to ballistic carrier behavior [28,29]. This phenomenon at L_{mask} = 33 nm is similar to the depletion effect coming from the channel punch-through, not the enhancement effect [1]. Although the importance of the diffusion effect is enhanced, the degradation of channel surface roughness or surface scattering is increasing, which impacts the channel mobility. This effect is probably due to the increase in gate field slightly retarding the flowing of surface current. From checking points ***B*** to ***D***, the current density is treated as line density (A/cm). At checking points ***A*** and ***E***, there is no diffusion or drive current dominated by the drift effect. The unit of current density is recovered as A/cm^2.

Extension work to establish the precise device models for 3D devices such as FinFETs [30–32] or gate-all-around FETs [33,34] is still outstanding. Even though the device format is multi-nano-sheet (mNS) or multi-bridge-channel [16,35–37], this concept of providing a great set of device models considering the contribution of the gate field is rather feasible. Of course, entering the 10-nm process or beyond, the current performance can be disturbed by quantum confinement effects [38–40]. These effects are useful to consider in modelling 5-nm FinFET devices or beyond as the device dimension of semiconductors approaches near to or moves below the exciton Bohr radius (EBR) of bulk semiconductors [41], where EBR is defined as the separation distance between the hole and electron around 1–10 nm. The charge carriers can freely move in a bulk semiconductor, and, thus, the wave function is similar to a hydrogen atom. In addition, Dr. Mark Liu, president of TSMC, in February 2021 [13], addressed the manufacturing products adopted the FinFET structure at the 3-nm process era. Hence, this extension task from 1D to 2D device-model improvement is impressive. In the future, separately considering the channel-length modulation and overshoot of drift velocity in the device model should enable us to obtain accurate device models beyond 10-nm field-effect transistors. Here, these two factors were temporarily incorporated into equivalent mobility in calculation, not separated as variables in discussion. For the new devices, such as mNSFETs or complementary FETs (CFETs) in the 1- or 2-nm process [42–44], advanced device models will be more complicated and the quantum mechanics effect in carrier movement [2] must be included in calculation. Ultimately, the contribution of the channel length as a variable can probably be considered if needed.

5. Conclusions

Integrating the effects of channel length modulation and drift velocity overshoot into the equivalent mobility, the mixed current model, including surface drift and diffusion current, has been created to describe the electrical behavior of the drive current of nano-node MOSFETs. The existence of a diffusion current addresses why the drive current enters the saturation region but does not reach zero at the pinch-off point. The diffusion contribution to the drive current becomes more apparent, especially for short-channel MOSFETs. For devices operating normally, the parameters (V_{DS}, V_{GS}, and L_{mask}) independent of channel position are strongly correlated to the μ_{eq} variable. It is thus necessary to investigate the mutual interaction among them. This work successfully determined the physical and meaningful consequences for nano-node HK/MG MOSFET devices fabricated with ALD technology. The error between simulated and experimental results was less than 0.3%, which is suitable for 28-nm devices or beyond to build up a more accurate set of device models in circuit design consideration. This performance is also better than that achieved in a previous project [11]. In the future, this methodology can be employed for the device model of 3D FinFETs or gate-all-around FETs for sub-10-nm manufacturing technology.

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References

1. Streetman, B.G.; Banerjee, S.K. *Solid State Electronic Devices*, 7th ed.; Pearson: Hoboken, NJ, USA, 2016; pp. 290–350.
2. Hu, C. *Modern Semiconductor Devices for Integrated Circuits*, 1st ed.; Pearson: Hoboken, NJ, USA, 2010; pp. 213–265.
3. Nguyen-Duc, C.; Cristoloveanu, S.; Ghibaudo, G. A three-piece model of channel length modulation in submicrometer MOSFETs. *Solid-State Electron.* **1988**, *31*, 1057–1063. [CrossRef]
4. Lim, K.Y.; Zhou, X. An analytical effective channel-length modulation model for velocity overshoot in submicron MOSFETs based on energy-balance formulation. *Microelectron. Reliab.* **2002**, *42*, 1857–1864. [CrossRef]
5. Moon, B.J.; Park, C.K.; Lee, K.; Shur, M. New short-channel n-MOSFET current-voltage model in strong inversion and unified parameter extraction method. *IEEE Trans. Electron. Dev.* **1991**, *38*, 592–602. [CrossRef]
6. Shasidl, G.G.; Antoniadis, D.A.; Smith, H.I. Electron velocity overshoot at room and liquid nitrogen temperatures in silicon inversion layers. *IEEE Electron. Dev. Lett.* **1988**, *9*, 94–96.
7. Thornber, K.K. Current equations for velocity overshoot. *IEEE Electron. Dev. Lett.* **1982**, *3*, 69–71. [CrossRef]
8. Kobayashi, T.; Saito, K. Two-dimensional analysis of velocity overshoot effects in ultrashort-channel Si MOSFET's. *IEEE Trans. Electron. Dev.* **1985**, *32*, 788–792. [CrossRef]
9. Chou, S.Y.; Antoniadis, D.A.; Smith, H.I. Observation of electron velocity overshoot in sub-100-nm-channel MOSFET's in silicon. *IEEE Electron. Dev. Lett.* **1985**, *6*, 665–667. [CrossRef]
10. Chamberlain, S.G.; Husain, A.; Gaensslen, F.H. Nonuniform displacement of MOSFET channel pinchoff. *IEEE Trans. Electron. Dev.* **1984**, *31*, 252–256. [CrossRef]
11. Huang, H.S.; Wang, W.L.; Wang, M.C.; Chao, Y.H.; Wang, S.J.; Chen, S.Y. I-V model of nano nMOSFETs incorporating drift and diffusion current. *Vacuum* **2018**, *155*, 76–82. [CrossRef]
12. Tachiki, K.; Ono, T.; Kobayashi, T.; Kimoto, T. Short-channel effects in SiC MOSFETs based on analyses of saturation drain current. *IEEE Trans. Electron. Dev.* **2021**, *68*, 1382–1384. [CrossRef]
13. Unleashing the Future of Innovation. Available online: https://research.tsmc.com/assets/download/Chairman_2021_ISSCC.pdf (accessed on 20 May 2021).
14. MBCFET—Multi-Bridge Channel FET. Available online: https://samsungatfirst.com/mbcfet/ (accessed on 20 June 2021).
15. Intel Introduces New RibbonFET and PowerVia Technologies. Available online: https://www.youtube.com/watch?v=Rt-7c9Wgnds/ (accessed on 27 July 2021).
16. Seon, Y.; Chang, J.; Yoo, C.; Jeon, J. Device and Circuit Exploration of Multi-Nanosheet Transistor for Sub-3 nm Technology Node. *Electronics* **2021**, *10*, 180. [CrossRef]
17. Lee, J.C.; Cho, H.J.; Kang, C.S.; Rhee, S.; Kim, Y.H.; Choi, R.; Kang, C.Y.; Choi, C.; Abkar, M. High-k dielectrics and MOSFET characteristics. In Proceedings of the IEEE International Electron Devices Meeting, Washington, DC, USA, 8–10 December 2003. [CrossRef]
18. Liao, J.C.; Chang, T.C.; Syong, W.R.; Lu, Y.H.; Liu, H.W.; Lin, C.Y.; Ciou, F.M.; Lin, Y.S. The impact of different TiN capping metal thicknesses on high-k oxygen vacancies in n-MOSFETs. *IEEE Trans. Dev. Mater. Reliab.* **2017**, *17*, 799–801. [CrossRef]
19. Na, S.; Yoon, S. Impacts of HfO_2/ZnO stack-structured charge-trap layers controlled by atomic layer deposition on nonvolatile memory characteristics of In-Ga-Zn-O channel charge-trap memory thin-film transistors. *IEEE J. Electron Dev. Soc.* **2019**, *7*, 453–461. [CrossRef]
20. Ryu, D.; Kim, M.; Yu, J.; Kim, S.; Lee, J.; Park, B. Investigation of sidewall high-k interfacial layer effect in gate-all-around structure. *IEEE Trans. Electron. Dev.* **2020**, *67*, 1859–1863. [CrossRef]
21. Austin, D.Z.; Allman, D.; Price, D.; Hose, S.; Conley, J.F. Plasma enhanced atomic layer deposition of Al_2O_3/SiO_2 MIM capacitors. *IEEE Electron. Dev. Lett.* **2015**, *36*, 496–498. [CrossRef]
22. Zouw, K.; Aarnink, A.A.I.; Schmitz, J.; Kovalgin, A.Y. Conduction and electric field effect in ultra-thin tungsten films. *IEEE Trans. Semicond. Manufact.* **2020**, *33*, 202–209. [CrossRef]

23. Lin, Y.C.; Chung, V.P.J.; Santhanam, S.; Mukherjee, T.; Fedder, G.K. Sidewall metallization on CMOS MEMS by platinum ALD patterning. *J. Microelectromech. Syst.* **2020**, *29*, 978–983. [CrossRef]
24. Hou, Y.T.; Li, M.F.; Low, T.; Kwong, D.L. Metal gate work function engineering on gate leakage of MOSFETs. *IEEE Trans. Electron. Dev.* **2004**, *51*, 1783–1789. [CrossRef]
25. Huang, A.; Zheng, X.; Xiao, Z. Interface dipole engineering in metal gate/high-k stacks. *Chin. Sci. Bull.* **2012**, *57*, 2872–2878. [CrossRef]
26. Foty, D. *MOSFET Modeling with SPICE Principles and Practice*, 1st ed.; Prentice Hall: Upper Saddle River, NJ, USA, 1997.
27. Xiao, H. *Introduction to Semiconductor Manufacturing Technology*, 2nd ed.; SPIE: Bellingham, DC, USA, 2012.
28. Murnal, V.R.; Vijaya, C. A quasi-ballistic drain current, charge and capacitance model with positional carrier scattering dependency valid for symmetric DG MOSFETs in nanoscale regime. *Nano Converg.* **2019**, *6*, 19. [CrossRef] [PubMed]
29. Wojcik, D.K.; Dorfman, J.R. Crossover from diffusive to ballistic transport in periodic quantum maps. *Phys. D Nonlinear Phenom.* **2004**, *187*, 223–243. [CrossRef]
30. Convertino, C.; Zota, C.B.; Caimi, D.; Sousa, M.; Moselund, K.E.; Czornomaz, L. High-performance InGaAs FinFETs with raised source/drain extensions. *Jpn. J. Appl. Phys.* **2019**, *58*, 080901. [CrossRef]
31. Chen, M.L.; Sun, X.; Liu, H.; Wang, H.; Zhu, Q.; Wang, S.; Du, H.; Dong, B.; Zhang, J.; Sun, Y.; et al. A FinFET with one atomic layer channel. *Nat. Comm.* **2020**, *11*, 1205. [CrossRef] [PubMed]
32. Zhang, S. Review of modern field effect transistor technologies for scaling. *J. Phys. Conf. Ser.* **2020**, *1617*, 012054. [CrossRef]
33. Kim, S.; Kim, M.; Ryu, D.; Lee, K.; Kim, S.; Lee, J.; Lee, R.; Kim, S.; Lee, J.H.; Park, B.G. Investigation of electrical characteristic behavior induced by channel-release process in stacked nanosheet gate-all-around MOSFETs. *IEEE Trans. Electron Dev.* **2020**, *67*, 2648–2652. [CrossRef]
34. Park, C.; Yun, I. Degradation of off-phase leakage current of FinFETs and gate-all-around FETs induced by the self-heating effect in the high-frequency operation regime. *IEEE Trans. Nanotechnol.* **2020**, *19*, 308–314. [CrossRef]
35. Bao, R.; Watanabe, K.; Zhang, J.; Guo, J.; Zhou, H.; Gaul, A.; Sankarapandian, M.; Li, J.; Hubbard, A.R.; Vega, R.; et al. Multiple-Vt solutions in nanosheet technology for high performance and low power applications. In Proceedings of the IEEE International Electron Devices Meeting, San Francisco, CA, USA, 7–11 December 2019. [CrossRef]
36. Yoon, J.S.; Jeong, J.; Lee, S.; Baek, R.H. Optimization of nanosheet number and width of multi-stacked nanosheet FETs for sub-7-nm node system on chip applications. *Jpn. J. Appl. Phys.* **2019**, *58*, BA12. [CrossRef]
37. The Nanosheet Transistor Is the Next (and Maybe Last) Step in Moore's Law. Available online: https://spectrum.ieee.org/the-nanosheet-transistor-is-the-next-and-maybe-last-step-in-moores-law (accessed on 26 July 2021).
38. Rama Krishna, M.V.; Friesner, R.A. Quantum confinement effects in semiconductor clusters. *J. Chem. Phys.* **1991**, *95*, 8309. [CrossRef]
39. Borrelli, N.F.; Hall, D.W.; Holland, H.J.; Smith, D.W. Quantum confinement effects of semiconducting microcrystallites in glass. *J. Appl. Phys.* **1987**, *61*, 5399. [CrossRef]
40. Norris, D.J.; Bawendi, M.G. Measurement and assignment of the size-dependent optical spectrum in CdSe quantum dots. *Phys. Rev. B* **1996**, *53*, 16338–16346. [CrossRef]
41. Mushonga, P.; Onani, M.O.; Madiehe, A.M.; Meyer, M. Indium phosphide-based semiconductor nanocrystals and their applications. *J. Nanomater.* **2012**, *2012*, 869284. [CrossRef]
42. Cheng, C.K.; Ho, C.T.; Lee, D.; Lin, B.; Park, D. Complementary-FET (CFET) standard cell synthesis framework for design and system technology co-optimization using SMT. *IEEE Trans. VLSI Syst.* **2021**, *29*, 1178–1191. [CrossRef]
43. Vincent, B.; Boemmels, J.; Ryckaert, J.; Ervin, J. A benchmark study of complementary-field effect transistor (CFET) process integration options done by virtual fabrication. *IEEE J. Electron. Dev. Soc.* **2020**, *8*, 668–673. [CrossRef]
44. Gupta, M.K.; Weckx, P.; Schuddinck, P.; Jang, D.; Chehab, B.; Cosemans, S.; Ryckaert, J.; Dehaene, W. The complementary FET (CFET) 6T-SRAM. *IEEE Trans. Electron. Dev.* **2021**, *68*, 6106–6111. [CrossRef]