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Review

β-Ga_2O_3-Based Power Devices: A Concise Review

Maolin Zhang [1,2], Zeng Liu [1,2], Lili Yang [1,2], Jiafei Yao [1,2], Jing Chen [1,2], Jun Zhang [1,2], Wei Wei [3], Yufeng Guo [1,2,*] and Weihua Tang [1,2,*]

[1] College of Integrated Circuit Science and Engineering, Nanjing University of Posts and Telecommunications, Nanjing 210023, China; zhangml5277@163.com (M.Z.); zengliu@njupt.edu.cn (Z.L.); liliyang@njupt.edu.cn (L.Y.); jfyao@njupt.edu.cn (J.Y.); chenjing1992@njupt.edu.cn (J.C.); zhangjun1991@njupt.edu.cn (J.Z.)
[2] National and Local Joint Engineering Laboratory of RF Integration and Micro-Assembly Technology, Nanjing 210023, China
[3] College of Electronic and Optical Engineering, Nanjing University of Posts and Telecommunications, Nanjing 210023, China; weiwei@njupt.edu.cn
* Correspondence: yfguo@njupt.edu.cn (Y.G.); whtang@njupt.edu.cn (W.T.)

Abstract: Ga_2O_3 has gained intensive attention for the continuing myth of the electronics as a new-generation wide bandgap semiconductor, owing to its natural physical and chemical properties. In this review article, we selectively summarized the recent advances on the experimental and theoretical demonstration of β-Ga_2O_3-based power devices, including Schottky barrier diodes and field-effect transistors, aiming for an inherent comprehending of the operating mechanisms, discussion on the obstacles to be addressed, and providing some comprehensive guidance for further developments. In the short run, Ga_2O_3 may well be promising to lead power electronics.

Keywords: Ga_2O_3; power device; Schottky barrier diodes; field-effect transistors

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1. Introduction

Wide bandgap semiconductors including SiC, GaN, Ga_2O_3, and diamond are promised to construct the next-generation power devices [1], owing to their natural high critical breakdown electric field (E_{br}), thin drift region, and low on-state resistance (R_{on}) [2–4]. Among them, recently, Ga_2O_3 has gained great attention for its high Baliga's figure of merit (BFOM), carrier mobility, dielectric constant, and critical breakdown field [5–8].

The easy availability of the Ga_2O_3 material gives it advantages for device development from a perspective of economic cost [9]. The Ga_2O_3 single crystal substrates can be prepared by using melting methods [10–12], and the Ga_2O_3 thin films can be grown by the laser molecular beam epitaxy (laser-MBE) [13,14], pulsed laser deposition (PLD) [15], magnetron sputtering [16,17], metal-organic chemical vapor deposition (MOCVD) [18–21], mist-CVD [22], atomic layer deposition (ALD) [23,24], and metal-organic vapor-phase epitaxy (MOVPE) [25] techniques. In addition, the carrier concentration and the mobility for Ga_2O_3 could be regulated by doping with shallow dopants and ion implantation [26–34].

Among the five phases of Ga_2O_3, beta-phase Ga_2O_3 (β-Ga_2O_3) is the most chemically and thermally stable allotrope [35], and is extensively employed to investigate and construct electronic as well as optoelectronic devices [36–40]. The comparison of properties for β-Ga_2O_3 and other semiconductors is shown in Table 1. As fundamental criteria, β-Ga_2O_3 has a bandgap of 4.5–4.9 eV, a critical theoretical electrical field of ~8 MV/cm [36,41], and anti-irradiation ability by high-energy particles and beams [36,42,43], catering for the requirements of power devices. Its BFOM is 8× to SiC and 4× to GaN, translating to the promised employment and desired hope to surpass the GaN and SiC (and their alloying materials) power devices [36,44], at least showing a compensation element in their comparatively mature territory.

Table 1. Comparison of properties for β-Ga$_2$O$_3$ and other semiconductors [36,39,45].

Parameters	Si	GaN	4H-SiC	Diamond	β-Ga$_2$O$_3$
Bandgap E_g (eV)	1.1	3.4	3.25	5.5	4.5–4.9
Relative dielectric constant ε	11.8	9.0	9.7	5.5	10
Breakdown electric field E_b (MV/cm)	0.3	3.3	2.5	10	8
Electron mobility (cm^2/V s)	1500	1250	1000	2000	250–300
BFOM ($\varepsilon\mu E_b^3$)	1	846	317	24,660	3444
JFOM ($E_b v_{sat}$)	1	1089	278	1110	2844

Due to the inherent high breakdown electric field, β-Ga$_2$O$_3$-based power devices can sustain the same breakdown voltage rating with a thinner drift region, leading to a reduced specific on-state resistant $R_{on,sp}$ and a lower voltage drop. Consider the DC-AC inverter as an example, Figure 1 plots the ideal power consumption of the low-doped drift region for various power devices with different voltage/current ratings. A duty cycle of 50% is assumed and the bipolar carrier transport is excluded. β-Ga$_2$O$_3$ power devices exhibit a more significant reduction than Si, 4H-SiC, and GaN devices at a greater voltage/current rating, indicating that β-Ga$_2$O$_3$ is suitable for high-power applications such as train traction and electricity transmission.

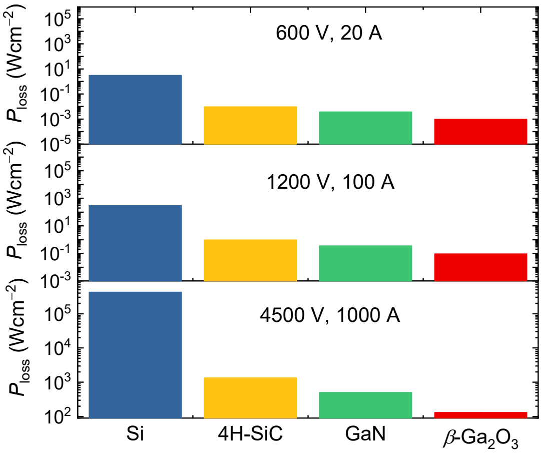


Figure 1. Comparison between the ideal power consumption of low-doped drift region for various power devices with different voltage/current ratings.

In the last decade, β-Ga$_2$O$_3$-based power devices, including field-effect transistors (FETs) and Schottky barrier diodes (SBDs), have been extensively investigated. Crystal quality, process optimization, and device structural engineering are keys to presenting a satisfying performance of β-Ga$_2$O$_3$ devices. Crystal growth and process review can be found in other places [46–48], and thus this paper mainly focuses on structural innovations and their physical insights. In the following sections, we summarize the recent state-of-the-art progress of β-Ga$_2$O$_3$ SBDs and FETs according to their technical characteristics and show some discussions and opinions.

2. Schottky Barrier Diode

Schottky barrier diodes (SBDs) are a core component in rectifying switches. Based on β-Ga$_2$O$_3$ materials, some device structures and technologies are using blending in their power devices for facilitating the progress of corresponding devices [49–64]. In this section, we introduce the advances of the β-Ga$_2$O$_3$-based SBDs. The rectify mechanism of β-Ga$_2$O$_3$ SBD is straightforward: the substrate is depleted, and the barrier is thus formed due to the work function difference between the Schottky metal and the β-Ga$_2$O$_3$ substrate. Ideally, SBD devices are governed by the thermionic emission (TE) theory as follows:

$$I = I_0 \left[\exp\left(\frac{qV}{nkT} - 1 \right) \right], \tag{1}$$

$$I_0 = AA^* T^2 \exp\left(-\frac{q\varphi_\mathrm{b}}{kT} \right), \tag{2}$$

$$\varphi_\mathrm{b} = \frac{kT}{q} \ln\left(\frac{AA^* T^2}{I_0} \right), \tag{3}$$

$$A^* = \frac{4\pi q m^* k^2}{h^3}, \tag{4}$$

where I_0 is the reverse saturation current, q is the electron charge (1.6×10^{-19} C), n is the ideality factor, k is the Boltzmann constant (1.38×10^{-23} J/K), T is the temperature, A is the contacted area for metal electrode and semiconductor, φ_b is the Schottky barrier height (SBH), A^* is the Richardson constant, and m^* is the effective mass of β-Ga_2O_3. m^* is considered to be $0.324\mathrm{m}_0$, where m_0 is the mass of the free electron. For β-Ga_2O_3, A^* is estimated to be ~41 $\mathrm{A/cm^2\ K^2}$ [65,66].

2.1. Optimization for Schottky Barrier Height

One could learn from the TE model that the φ_b plays a vital role in the carrier transport of SBDs as it determines the built-in potential V_bi, forward voltage drop, and reverse leakage current. The understand of φ_b regulation is important to the performance tuning of β-Ga_2O_3 SBDs. Various factors such as the Schottky metal, surface treatment, and surface orientations have shown impacts on the φ_b [67–76]. In 2013, a β-Ga_2O_3 SBD was fabricated on a (010) unintentionally doped substrate [67]. Ti/Au and Pt/Au were deposited on each side of the substrate to form the ohmic and Schottky contact, respectively. The barrier height was measured to be 1.52 eV according to the C-V test. Due to the high-quality β-Ga_2O_3 substrate and the relatively large barrier height, the reverse leakage current was less than 10^{-8} $\mathrm{A/cm^2}$ and the ideality factor was estimated to be 1.04–1.06.

The study of Ni/Au β-Ga_2O_3 SBD revealed the impacts of anode metal on the φ_b [69]. The V_bi of the Ni/Au β-Ga_2O_3 SBD is significantly decreased in comparison with other SBDs, indicating a reduced Schottky barrier height. In addition, in our previous work, a Ni/β-Ga_2O_3/Ti SBD was demonstrated [76]. The φ_b was calculated to be 0.93 eV and the V_bi was 0.52 V based on the J-V curve. The device diagram of the β-Ga_2O_3 SBD with different anode metals can be found in Figure 2a. Recently, a double-barrier β-Ga_2O_3 SBD was proposed to reduce the turn-on voltage as well as the leakage current, shown in Figure 2b [75]. The Schottky contact consists of relatively low work function Ni and high work function metal PtO_x. The ratio of Ni and PtO_x showed effects on the trade-off between the turn-on voltage and the current density. The optimal ratio of Ni:PtO_x = 75:150 was obtained to achieve a competitive leakage current and a low turn-on voltage.

Evidence also shows that the highly asymmetric crystal structure of β-Ga_2O_3 might introduce the anisotropic Schottky property. Researchers examined the surface properties of (010) and ($\bar{2}$01) Sn-doped β-Ga_2O_3 substrates through X-ray photoelectron spectroscopy (XPS) measurements [70]. It is found that the surface barrier height of the ($\bar{2}$01) substrate was 1.14 eV, whereas the (010) surface exhibited a barrier height of 1.63 eV. The existence of the surface barrier is due to the negatively charged surface states and the defects, which contribute to the difficulties in forming ohmic contact. Further, SBDs were fabricated on the (010) and ($\bar{2}$01) substrates with extracted φ_b being 1.05 eV and 1.20 eV, respectively. The difference of φ_b can be well explained by the XPS results.

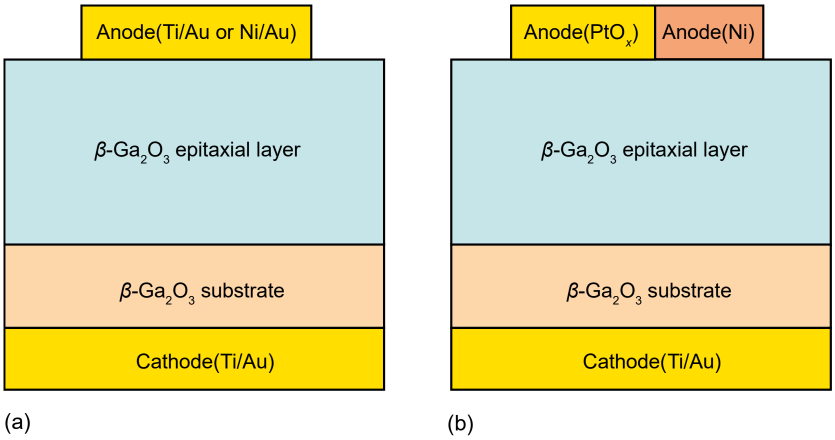


Figure 2. (**a**) Device diagram of the β-Ga_2O_3 SBD with different anode metals. (**b**) Device diagram of the double-barrier β-Ga_2O_3.

As surface state is a major reason for the surface band bending, surface treatment could be beneficial to the barrier height modulation. It is reported that a CF_4 plasma treatment can reduce the leakage current of β-Ga_2O_3 SBDs [77]. Ti/Al/Au was deposited on the backside of the sample, and the β-Ga_2O_3 substrate was then sent into a reactive ion etch (RIE) system for a low-power CF_4-plasma treatment. Subsequently, Ni/Au metal was deposited on the sample to form the Schottky contact. A Schottky barrier height of 1.31 eV was obtained by adopting the F-plasma treatment, while the untreated SBD exhibited a φ_b of 1.18 eV. XPS measurement indicated that the insulating GaF_x was introduced and Si dopants near the surface region were removed after the F-plasma treatment. Consequently, the surface Fermi level shifted toward the valence band by ~0.14 eV, leading to the increase of φ_b and the four times order reduction in the reverse leakage current.

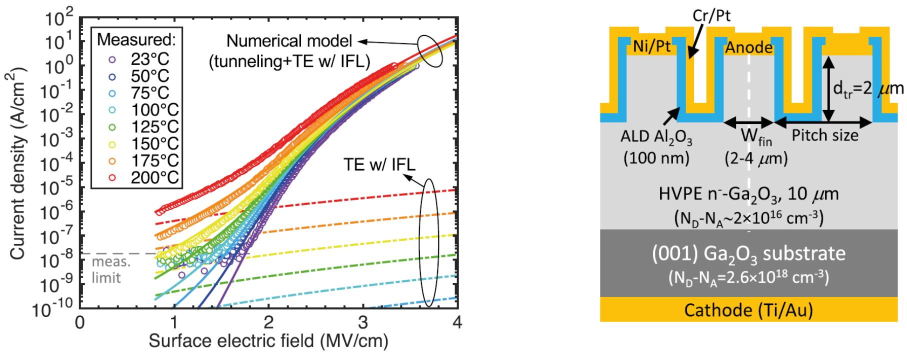
The interfacial layer can be also utilized to modulate the φ_b. He et al. introduced the aluminum oxide interfacial layer between the Schottky contact and the semiconductor surface [78]. Three types of devices were investigated, namely the Al-reacted interfacial layer case, ALD Al_2O_3 case, and abrupt metal–semiconductor–Schottky barrier case. The insertion of the oxide interfacial layer presented major impact on the Schottky barrier height. A lower subthreshold slope (SS) was achieved by using the Al-reacted interfacial layer. On the other hand, the ALD Al_2O_3 sample exhibited a much greater SS of ~200 mV/Dec due to the fixed charge resulting from the O-dangling bonds.

For power electronics, the forward voltage drop and the leakage current are often found to be contradictory. As for the β-Ga_2O_3 SBD, a lower φ_b would lead to a reduced forward voltage drop and a consequently decreased on-state power dissipation. However, the leakage current surges with a reduced φ_b, and thus the off-state power consumption increases. It is necessary to adjust the φ_b according to the application. Based on the above-mentioned techniques, the variation of the φ_b can be achieved and more precise regulations will soon be available.

2.2. Reduction of the Interface Electric Field

As β-Ga_2O_3 SBD is designed to withstand a higher reverse voltage than the Si as well as SiC counterparts, the electric field at the Schottky contact interface and the band bending throughout the β-Ga_2O_3 substrate would be significant. As a result, the image force lowering (IFL) as well as the barrier width reduction become prominent, and thus the leakage current surges [79]. A Ni-contact β-Ga_2O_3 SBD on (201) Sn-doped β-Ga_2O_3 substrates was fabricated to eliminate the edge leakage current and improve the Schottky interface quality [79]. The reverse J-V curve was well fitted by their numerical model considering the thermionic field emission (TFE), TE, IFL and doping effects, as shown in Figure 3a. It is evident that the tunneling, i.e., the TFE or the field emission (FE), is the main conduction process at a high electric field scenario. Hence, the leakage current increases rapidly with the rise of surface electric field.

Due to the significant FE and the TFE current in β-Ga_2O_3 SBD, it is thus necessary to reduce the electric field strength at the Schottky contact/β-Ga_2O_3 interface. To date, the most popular method is to introduce the trench structure into the β-Ga_2O_3 SBD [80–87]. The device structure of the trench SBD is plotted in Figure 3b [81]. As the reverse voltage increases, the leakage current rises rapidly and coincides with the TFE model. The trench SBD, however, exhibits a much lower leakage current and a higher breakdown voltage, which may be attributed to the introduction of an extra electric field peak at the trench corner and the reduction of surface electric field strength.



(a) (b)

Figure 3. (**a**) Comparison of physical models for the calibration of reverse leakage current. Reprinted from [79], with the permission of AIP Publishing. (**b**) Device diagram of the trench β-Ga_2O_3 SBD. Reprinted from [81], with the permission of AIP Publishing.

2.3. Suppression of the Edge Electric Field

It is also confirmed that a peak electric field exists at the Schottky contact edge and often causes the premature breakdown [88–90]. To suppress this unexpected electric field peak, various structural designs have been proposed [91–106]. Field plates are widely used in commercial power devices and have also been introduced into the β-Ga_2O_3 SBD [97]. The structure of the field plate SBD can be found in Figure 4. An on-state resistance of 5.1 mΩ/cm^2 and a breakdown voltage of 1076 V were measured. Simulation results showed that the breakdown electric field under the anode foot edge was 5.1 MV/cm and was greater than the theoretical E_{br} of SiC and GaN, confirming the potential of β-Ga_2O_3 in power electronics.

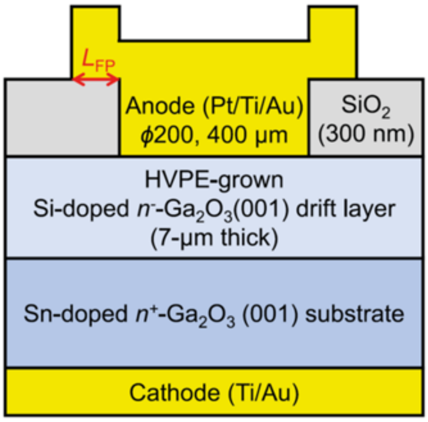


Figure 4. Device diagrams of SBD with field plates. Reprinted from [97], with the permission of AIP Publishing.

A bevel field-plated β-Ga_2O_3 SBD can further reduce the peak electric field at the contact edge and improve the breakdown performance, as shown in Figure 5 [100]. The beveled trench can be introduced by BCl_3 dry etching. The β-Ga_2O_3 SBD with the beveled field plate showed a breakdown voltage of 190 V, while that of planar SBD was measured to be 138 V. The 2D numerical results indicated that peak electric field at the contact foot edge was reduced by adopting the field plate and thus the breakdown performance was improved. It is worth noting that a small angle trench is more effective in GaN vertical diode for improving the electric field profile at the anode edge [107]. Similar conclusions may also apply to β-Ga_2O_3 SBDs. To verify this, the vertical β-Ga_2O_3 SBDs with small-angle beveled field plates was fabricated [102]. The beveled field plate structure shows an angle of ~45° and the small-angle plate features a ~1° beveled field plate. The small, titled angle was formed by PECVD-SiO_2/spin-on-glass (SOG) deposition and wet etch, and the following is the RIE dry etching. Compared with the beveled field plate, a small-angle beveled field plate can reduce the electric field peak by 50%. Consequently, the small-angle configuration exhibited the highest breakdown voltage of ~1100 V and that of the bevel field-plated SBD was measured to be ~650 V. However, the small-angle field plate would increase the cell area and further investigation on the tilt angle is expected.

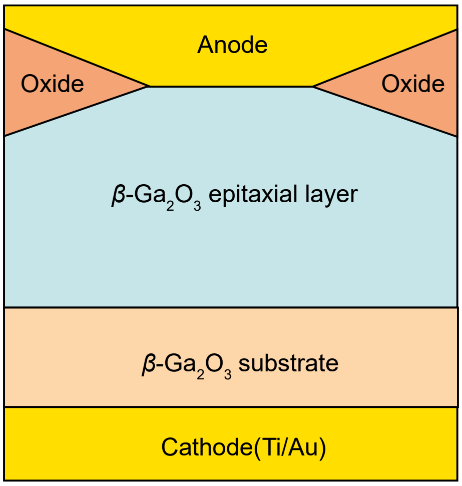


Figure 5. Device diagrams of SBD with beveled field plate.

More recently, a trench SBD with the dual field plate has been proposed [103]. The trench SBD has the greatest on-state resistance in comparison with the mesa SBD and conventional SBD due to the sidewall depletion. Meanwhile, leakage current is significantly depressed by utilizing the trench architecture. Consequently, the trench SBD with field plate showed a $R_{on,sp}$ of 8.8 $m\Omega\cdot cm^2$ and a breakdown voltage of 2.89 kV, featuring a corresponding power figure of merit (FOM) of 0.95 GW/cm^2.

Apart from the field plates, edge termination has also been proven to be effective in optimizing the electric field profile along the Schottky edge. The structure of β-Ga_2O_3 SBD with edge terminations is shown in Figure 6. Recently, a vertical β-Ga_2O_3 SBD with Mg-implanted edge termination was fabricated [91]. Triple Mg implantations were carried out with energy/concentration of 50 keV/1.4 $\times$ 10^{14} cm^{-2}, 125 keV/2 $\times$ 10^{14} cm^{-2}, and 250 keV/9.8 $\times$ 10^{14} cm^{-2}, respectively. The introduction of Mg-implanted edge termination resulted in the breakdown voltage increase from 500 V to 1550 V. The Schottky barrier height and ideality factor were extracted to be 1.02 eV and 1.05, respectively. It is also observed from the simulation results that Mg-implanted edge termination can effectively relieve the electric field crowding effect by reducing the peak value from 10.2 MV/cm to 6.8 MV/cm. Since the implantation mainly occurs at the contact periphery, the ion-implanted edge termination technique would result in minimal impacts on the forward performance and thus could present potential in high-power β-Ga_2O_3 rectifiers.

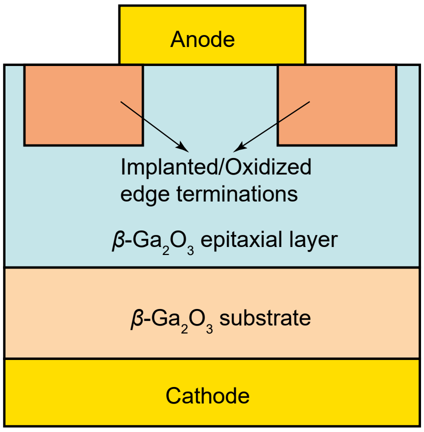


Figure 6. Device diagram of β-Ga_2O_3 SBD with edge terminations.

The Ar-implanted edge termination is also effective for edge field reduction [93]. The electric field strength at the anode periphery was reduced from 6.5 MV/cm to 4.5 MV/cm with a reverse voltage of 250 V; thus, a breakdown voltage increase of 134 V was obtained by using the Ar implantation. Zhang et al. further studied the impact of He- and Mg-implanted edge terminations [95]. It is shown that the introduction of He and Mg edge termination can enhance the breakdown voltage from 0.5 to 1.0 kV and 1.5 kV, respectively.

Additionally, thermally oxidized termination has been proved to be beneficial for enhancing the off-state performance of β-Ga_2O_3 SBDs. A thermal oxidation edge termination β-Ga_2O_3 rectifier has been demonstrated by annealing at high temperature in O_2 ambient for 30 min [94]. The C-V test showed that the electron concentration was reduced after the thermal oxidation, mostly because of the passivation of oxygen vacancies and the oxidation of donor impurities. The simulated profile indicated that the thermal oxidation can lower the peak electric field, resulting in a breakdown voltage of 940 V and a FOM of 295 MW/cm^2. Detail physical insights of thermal oxidization on the electron concentration can be further studied. In addition, Wei et al. proposed a compound termination β-Ga_2O_3 SBD. The edge termination consists of thermal oxidation [96], 20 nm SiO_2, 300 nm SiN_x, and air space. The air space is designed to reduce the SiO_2/β-Ga_2O_3 interface state. Breakdown voltage is improved from 145 V to 400 V by utilizing the compound termination.

Due to the absence of practical *p*-type doping in β-Ga_2O_3, floating guard rings and junction termination extension that have been applied in Si and SiC SBDs are challenging to realize in β-Ga_2O_3 SBDs. To avoid this issue, β-Ga_2O_3 SBDs with a guard ring formed by nitrogen ion implantation were fabricated in the work [105]. In addition, guard ring rectifiers incorporated with field plates were also demonstrated. Forward characteristics of studied structures were similar while the guard ring and field plate β-Ga_2O_3 SBD presented the greatest breakdown voltage. Note that the introduction of the guard ring resulted in a breakdown voltage increase of less than 100 V, indicating that further optimization is necessary, and *p*-type doping to enhance the floating guard ring performance is required.

Recently, the effect of *p*-type III-nitride guard ring on breakdown characteristics has been theoretically investigated [106]. It was found that guard ring with nonpolar graded *p*-AlGaN showed the optimal electric field profile and the greatest breakdown voltage, thus providing an optional approach in achieving the *p*-*n* junction. Although the *p*-type doping is not yet unavailable and not likely to be for a long time, the adoption of heterojunction may be a feasible approach and requires extensive research.

Similar results can be found in another work [80]. The effect of the fin/trench width on the electric field profile was detailed in this study. The surface electric field is suppressed, while the trench corner introduces an extra electric field peak. Meanwhile, the leakage current of the trench SBD reduced as the fin width decreased. This reveals that the fin width could affect the surface electric field profile as well as the tunneling process. In fact, the conventional SBD exhibited a triangle-shaped profile, and thus the maximum electric field is located at the Schottky interface. The trench SBD, however, showed more uniform distribution, and the interface electric field was reduced with a lower fin width. It is worth noting that the extra electric field peak at the trench corner indicates that a relatively great potential difference is applied on the dielectric layer, and thus the reliability of such structure needs further verification and optimization.

2.4. Thermal Consideration

The thermal issue is critical for β-Ga_2O_3 power devices because of the low thermal conductivity [108–113]. For β-Ga_2O_3 SBDs, an elevated temperature can increase the reverse current and thus deteriorates the off-state power consumption. However, the effect of temperature on the forward characteristics is currently under debate. Wang et al. investigated the performance of bevel-field-plated β-Ga_2O_3 SBDs at various temperatures [110]. It is found that the Schottky barrier height is increased with a greater operating temperature, which could be attributed to the inhomogeneity of barrier height. The turn-on voltage decreases as the temperature rises, which is in accordance with other reported results. As shown in Figure 7, the forward current, as well as the on-state differential resistance, were degraded with a higher operating temperature, mainly resulting from the degenerated mobility. On the contrary, Reddy et al. reported a positive temperature coefficient of forward current [111]. The reduced on-state resistance is believed to be introduced by the lowered Schottky barrier height at an elevated temperature. In addition, the enhanced donor ionization could be also beneficial to the on-state current by increasing the operating temperature. Nevertheless, the operation temperature should be reduced, and the reverse leakage current should be minimal since β-Ga_2O_3 SBD is expected to sustain a higher reverse voltage than SiC- and GaN-based SBDs.

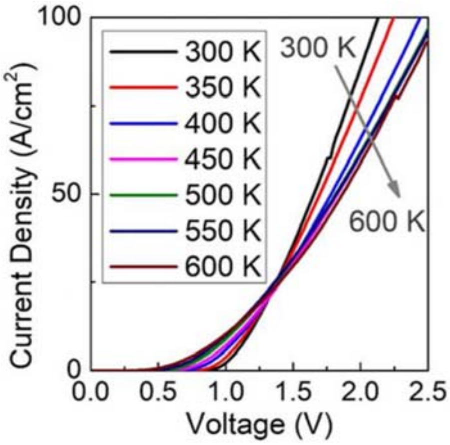


Figure 7. Impact of the temperature on the forward characteristics of β-Ga_2O_3 SBD. Reprinted from [110], with the permission of AIP Publishing.

To reveal the source of self-heating effect in β-Ga_2O_3 SBD, Chatterjee et al. investigated the heat generation process by utilizing various optical thermography approaches such as thermoreflectance thermal imaging, micro-Raman thermography, and infrared thermal microscopy [109]. It was shown that a significant part of heat was generated from the anode–substrate interface, and the Joule heating from the drift region is inevitable. Hence, it is recommended that a top-side cooling or flip-chip method can be effective for relieving the thermal issue of β-Ga_2O_3 SBDs. For this reason, high-performance packaging technology is critical for β-Ga_2O_3 SBDs [113]. Despite the low thermal conductivity of β-Ga_2O_3, the bottom-side cooling SBD showed a similar surge current capability to the commercial SiC SBD. Furthermore, the double-side cooling architecture showed an even superior performance in comparison with SiC SBDs. Based on the results, we believe that thermal concerns can be neglected in β-Ga_2O_3 SBDs by using advanced packaging and possible foreign substrate integration.

3. Field-Effect Transistors

β-Ga_2O_3 field-effect transistors (FETs), including bulk/epitaxy FETs [114–135] and nanomembrane FETs [136–161], are fundamental in the next generation β-Ga_2O_3-based power converters and systems. β-Ga_2O_3 FETs evaluate the on-state resistance R_{on} as well as the breakdown voltage V_b. Since the first practical β-Ga_2O_3 FET was fabricated, various techniques and structural engineering have been reported to improve the electrical performances of β-Ga_2O_3 power FETs. At the initial stage, β-Ga_2O_3 power FETs were grown on the Sn-doped Ga_2O_3 epitaxy layer with uniform *n*-type doping throughout the active region [114], as shown in Figure 8a. The measured V_b was 257 V with a gate-to-drain distance of 8 µm. As a result, the average longitudinal electric field was only 0.3 MV/cm in the drift region, which is far lower than the predicted value of 8 MV/cm by first principles calculations. In addition, the on-state current I_{on} was ~13 mA/mm with a gate overdrive voltage V_{on} of 10 V, giving a maximum transconductance g_m of 2.8 mS/mm. The specific on-state resistance $R_{on,sp}$ was 0.3 $\Omega \cdot cm^2$, which is two orders of magnitude higher than the ideal value. Clearly, to improve the performance of β-Ga_2O_3 power FETs, more effort is required.

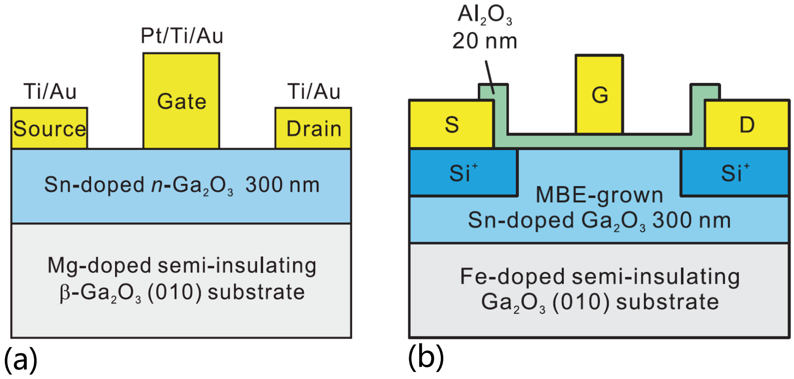


Figure 8. Device diagram of (**a**) β-Ga_2O_3 FET and (**b**) β-Ga_2O_3 MOSFET with Al_2O_3 gate dielectric. Reprinted from [114,115], with the permission of AIP Publishing.

In the past few years, numerous innovations have been implemented to reduce the R_{on} and improve the V_b of β-Ga_2O_3 power FETs. As the early devices were basically lateral FETs with depletion mode, and the enhancement-mode (E-mode) operation and the vertical architecture were subsequently released. This section will be organized according to the above content.

3.1. R_{on} Reduction

In terms of the reduction of R_{on}, high-quality ohmic contact of the source/drain (S/D) region as well as the carrier transport with high mobility are necessary. In addition, high electron mobility transistors (HEMTs) and the suppression of the self-heating effect (SHE) are also feasible approaches.

3.1.1. Ohmic Contact

High doping concentration is a common method to achieve ohmic contacts. To introduce the ohmic contact, Higashiwaki et al. proposed β-Ga_2O_3 power metal oxide semiconductor field-effect transistors (MOSFET) with Al_2O_3 as the gate dielectric [115], as shown in Figure 8b. A heavily doped S/D region is formed by the Si ion implantation, followed by the S/D contact anneal in N_2 to further reduce the contact resistance. As a result, the measured contact resistance was reduced to 8.1×10^{-6} $\Omega \cdot cm^2$. The fabricated MOSFET showed a breakdown voltage of 370 V and a reduced on-state resistance of 75 $m\Omega \cdot cm^2$. The spin-on-glass (SOG) doping was also utilized to realize low-resistance ohmic contacts. The cost of the SOG doping is significantly lower than the ion implantation since an ion implanter is not required [123]. The extracted specific contact resistivity was measured to be 2.1 ± 1.4 × 10^{-5} Ω·cm^2, and the peak g_m of the fabricated β-Ga_2O_3 power MOSFET was 1.23 mS/mm.

3.1.2. Channel Doping

In the early stage, the doping of the channel region was formed by molecular beam epitaxy (MBE) homoepitaxial Ga_2O_3 growth with Sn as its dopants [114,115]. However, the in situ Sn doping was considered to be inefficient because of the Sn segregation during the MBE growth [162]. To address this issue, the Si implantation was developed to form the *n*-type doping channel region. Nevertheless, the simple replacement of the Sn dopants to Si would lead to the Fe out diffusion into the channel region, resulting in the decreased channel doping. A Si-doped channel with a resistive buffer layer was proposed to reduce the parasitic conduction [119]. The channel region was defined by Si ion implantation with a doping concentration of 3 × 10^{17} cm^3. The channel thickness was 0.3 µm, and thus the UID layer under the channel would protect the substrate from implantation damage as well as the Fe out diffusion. Note that the UID layer could introduce a parasitic conduction path at the substrate/UID interface providing that a post-processing is absent. While the UID layer was deposited on the substrate, ozone/oxygen and the residual Si would form the thermally unstable silicon monoxide (SiO). It was found that the SiO can be desorbed after annealing, and the leakage current was thus reduced from >10 mA/mm to <1 nA/mm. The maximum measured field mobility was 105 cm^2 V^{-1} s^{-1}, and an anisotropy mobility was found, which is consistent with the theoretical calculations.

In addition to Sn and Si dopants, Ge dopant was considered to be an alternative because of its comparable atomic radius to Sn and a better match than Si. A Ge-doped β-Ga_2O_3 MOSFET on a (010) Fe-doped semi-insulating substrate was fabricated and studied [121]. The device showed a reasonable performance with $I_{on}/I_{off} > 10^8$, $I_{on} > 75$ mA/mm, and a maximum mobility of 111 cm^2 V^{-1} s^{-1}.

3.1.3. β-$(Al_xGa_{1-x})_2O_3/\beta$-$Ga_2O_3$ Heterostructures

Numerous works have reported that the carrier mobility in bulk β-Ga_2O_3 channel is in the range of 100–150 cm^2 V^{-1} s^{-1}, which is significantly lower than that of the GaN (1250 cm^2 V^{-1} s^{-1}) and 4H-SiC (1000 cm^2 V^{-1} s^{-1}) [48]. However, theoretical calculations have demonstrated up to 1000 cm^2 V^{-1} s^{-1} 2D electron gas (2DEG) mobility in β-Ga_2O_3 heterostructures due to the screening of impurity scattering [163]. As β-$(Al_xGa_{1-x})_2O_3/\beta$-$Ga_2O_3$ heterostructures have been successfully fabricated, the β-Ga_2O_3 HEMT incorporated with the modulation doping or delta doping is expected to greatly improve the electron mobility as well as its current driving capability [164–171].

Krishnamoorthy et al. reported on a β-$(Al_xGa_{1-x})_2O_3/\beta$-$Ga_2O_3$ FET with delta Si doping in the β-$(Al_xGa_{1-x})_2O_3$ layer [165]. The epitaxial structure is shown in Figure 9a. The heteroepitaxial structure was conducted by the oxygen plasma-assisted MBE and the delta doping was achieved through the pulsed doping approach. 2DEG with a sheet charge of 5 × 10^{12} cm^{-2} was obtained. The measured on-state current was 5.5 mA/mm, and the extracted maximum transconductance was 1.75 mS/mm. The mobility reported in this work was 74 cm^2 V^{-1} s^{-1} and thus needs further improvement in comparison with the predicted value. In addition, the I_{on}/I_{off} ratio of the device was 10^5, which could be attributed to the parasitic conduction at the buffer/substrate interface.

Researchers have also adopted Ge as the *n*-type dopant to fabricate the β-$(Al_xGa_{1-x})_2O_3/\beta$-$Ga_2O_3$ HEMT [164]. The heterostructure was grown by using the plasma-assisted MBE as well, but the Ga polishing was introduced before the epitaxial growth. The details of the Ga polishing can be found in [172]. As a result, the rms surface roughness of the substrate was significantly reduced from >5 nm to 0.37 nm. More importantly, the Ga-polishing process could effectively decrease the unintentionally doped Si and Ge at the substrate surface by five times. Measured I-V characteristics showed that the I_{on}/I_{off} was up to 10^9 and a maximum transconductance of 4 mS/mm was obtained.

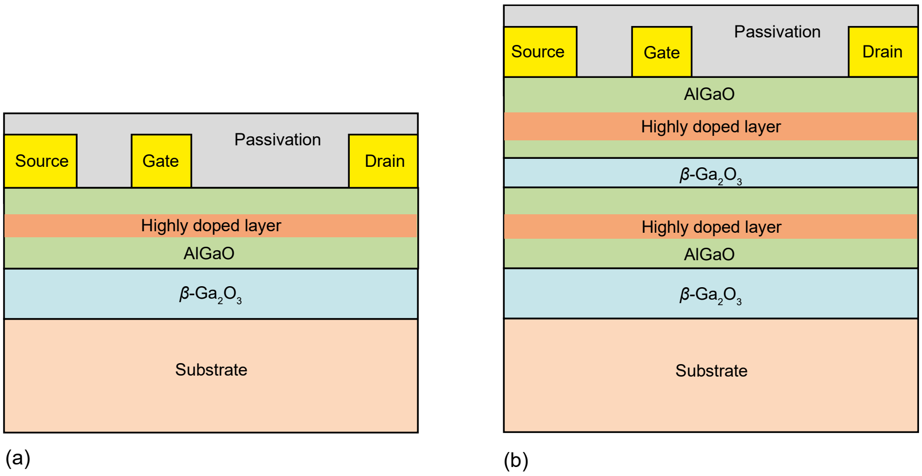


Figure 9. (**a**) Device diagram of β-(Al$_x$Ga$_{1-x}$)$_2$O$_3$/β-Ga$_2$O$_3$ FET with delta Si doping in the β-(Al$_x$Ga$_{1-x}$)$_2$O$_3$ layer. (**b**) β-(Al$_x$Ga$_{1-x}$)$_2$O$_3$/β-Ga$_2$O$_3$ FET with double channel.

To further reduce the on-state resistance, a β-(Al$_x$Ga$_{1-x}$)$_2$O$_3$/β-Ga$_2$O$_3$ HEMT with double heterostructures was proposed [166], as shown in Figure 9b. The dual-heterojunction can be clearly observed with a 3 nm β-Ga$_2$O$_3$ layer between the β-(Al$_x$Ga$_{1-x}$)$_2$O$_3$ barriers. Two channels are introduced and located at the β-Ga$_2$O$_3$ quantum well and the β-(Al$_x$Ga$_{1-x}$)$_2$O$_3$/UID Ga$_2$O$_3$ interface, respectively. By varying the doping levels in the top β-(Al$_x$Ga$_{1-x}$)$_2$O$_3$ barriers, a parasitic channel was introduced, and the charge density of the major channel was improved. However, this could also lead to a reduced 2DEG mobility in the β-Ga$_2$O$_3$ quantum well due to the impurity scattering. Nevertheless, the fabricated device shows superior performances with a peak transconductance of 39 mS/mm and a maximum I_{on} of 257 mA/mm. The measured hall mobility was 123 cm^2 V^{-1} s^{-1}, and the average breakdown electric field was 3.2 MV/cm. Just recently, Kalarickal et al. demonstrated a double heterojunction β-(Al$_x$Ga$_{1-x}$)$_2$O$_3$/β-Ga$_2$O$_3$ HEMT with a composite gate dielectric stack consisting of a low-*k* layer (Al$_2$O$_3$) and a high-*k* dielectric layer (BaTiO$_3$) [171]. The device exhibited a mobility of 85 cm^2 V^{-1} s^{-1} and an average breakdown electric field of 5.7 MV/cm, showing its potential for high-power and high-frequency device applications. In addition, a normally off AlN/β-Ga$_2$O$_3$ FET was demonstrated, where the 2DEG was introduced by the polarization effects at the AlN/β-Ga$_2$O$_3$ interface [169]. The device was examined through a TCAD simulation and showed promising performance. Further experimental verifications are needed to study the polarization effects.

3.1.4. Thermal Management

Power devices with high voltage and high current would introduce significant Joule heating, and thus the thermal conductivity of the constituent material is vital. Typically, the raised channel temperature would lead to a decreased mobility and an increased on-state resistance, which in turn amplifies the lattice temperature. Since β-Ga$_2$O$_3$ shows only <30 W/mK thermal conductivity, the SHE would be devastating to the β-Ga$_2$O$_3$ power FETs [173–193]. The channel temperature in β-Ga$_2$O$_3$ MOSFET has been evaluated by electrical measurements [173]. Results indicated that the SHE is the main reason for the premature saturation of drain current, and a 50% decrease in the maximum on-state current was observed. Therefore, aggressive thermal management should be implemented to improve the current driving capacity as well as the reliability of the β-Ga$_2$O$_3$ power MOSFET.

Heterogeneous integration of the high thermal conductivity substrate and the β-Ga$_2$O$_3$ epitaxial layer could be an effective approach to reduce the impacts of the SHE. The device diagram of β-Ga$_2$O$_3$ FET fabricated on a heterogeneous substrate is shown in Figure 10. Russell et al. studied the integration of β-Ga$_2$O$_3$ on the 4H-SiC substrate [174]. The simulation results predicted a lattice temperature reduction of 68 degrees and a 19% on-state current improvement. However, the heteroepitaxy growth remains a major challenge [194–196].

Furthermore, a wafer scale heterogeneous integration of β-Ga_2O_3 power MOSFET on SiC and Si substrates was proposed [184]. The heterointegration was realized by the wafer bonding with ion cutting. As the ambient temperature was increased from 300 K to 500 K, the on-state resistance of the β-Ga_2O_3 power MOSFET on the SiC or Si substrate showed only a 14% increment, while the β-Ga_2O_3 device without thermal management exhibited 117% R_{on} degradation. Therefore, heterointegration would be a promising way to overcome the shortage of the low thermal conductivity of β-Ga_2O_3.

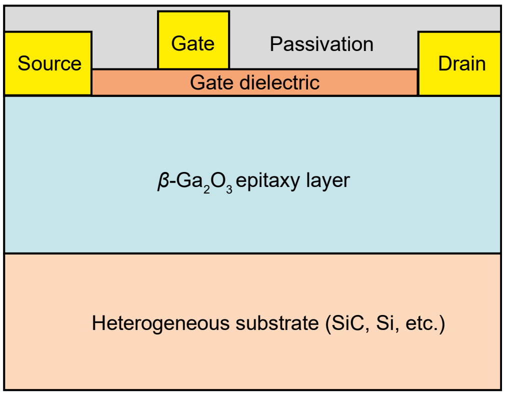


Figure 10. Device diagram of β-Ga_2O_3 FET fabricated on a heterogeneous substrate.

More aggressive heat dissipation engineering is required for β-$(Al_xGa_{1-x})_2O_3$/β-Ga_2O_3 HEMT since β-$(Al_xGa_{1-x})_2O_3$ exhibits even lower thermal conductivity than β-Ga_2O_3. Chatterjee et al. have theoretically investigated a feasible approach to reduce the SHE in β-$(Al_xGa_{1-x})_2O_3$/β-Ga_2O_3 HEMT [186]. The flip-chip or the double-sided method can be achieved by using the native or non-native substrate. The double-sided and the flip-chip schemes are more effective than the hetero substrates, indicating that the main thermal pathway is from the electrodes rather than the substrate. Besides, the simulation results also verified the thermal performance of double-sided cooling with nanocrystalline diamond covering the top and bottom sides of HEMTs. A maximum power-handling capability of 10 W/mm can be achieved by this method, highlighting the potential of thermal management in β-Ga_2O_3 power devices. In the near future, advanced thermal solutions such as mini channel heat sinks and integration of heat spreaders with high thermal conductivity could eliminate the robustness concerns of β-Ga_2O_3 devices.

3.2. Improvement for the Breakdown Voltage

In terms of the improvement in breakdown voltage, various techniques have been developed and significant enhancements have been achieved. Numerous researchers have shown that, for lateral power devices, the peak electric field is mainly located at the drain side of the gate edge, indicating that this location could be the most vulnerable area under a high drain voltage [147,151,159,197–199]. In order to improve the breakdown performance, i.e., increase the breakdown voltage, the peak electric field needs to be reduced. The optimization of the device structure could change the charge distribution, and thus the electric field profile can be varied. Currently, field plates have been widely used in β-Ga_2O_3 FETs, and more cutting edge techniques, such as variation of lateral doping (VLD) and charge balancing, are in development.

The basic diagram of the β-Ga_2O_3 FET with field plates is illustrated in Figure 11a. The gate-connected field plate β-Ga_2O_3 MOSFET was demonstrated by Wong et al. [197] The device was fabricated on a Fe-doped semi-insulating β-Ga_2O_3 (010) substrate and a UID epitaxial layer. The channel and the S/D region concentration were regulated by ion implantation. The field plate was introduced after the formation of the deposition for the SiO_2 passivation and the gate electrode. Measurement results showed a breakdown voltage of 755 V with a gate–drain separation of 15 μm, presenting a >80% improvement in breakdown voltage compared to their previous work [115]. Meanwhile, the peak transconductance was 3.4 mS/mm and the I_{on}/I_{off} reached 10^9.

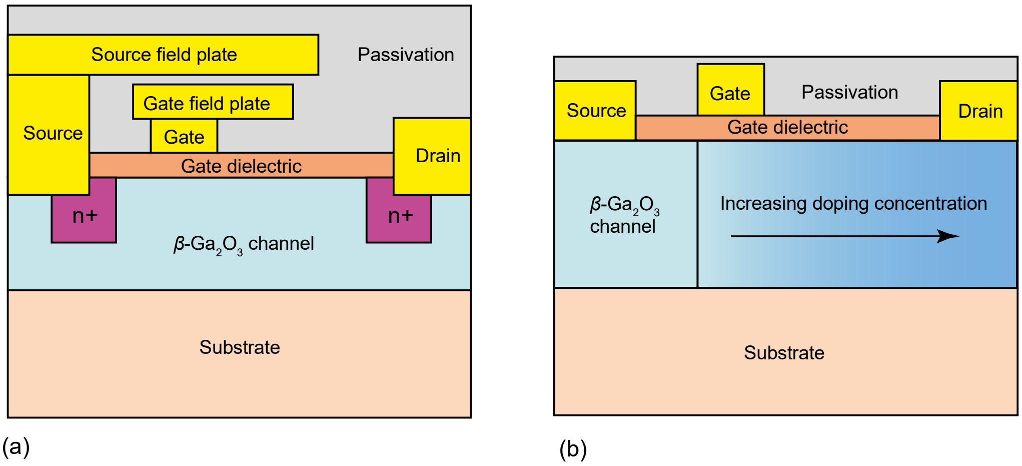


Figure 11. Device structure of the β-Ga_2O_3 FET with (**a**) gate/source field plate and (**b**) VLD technique.

Due to the nature of the high breakdown electric field for the β-Ga_2O_3, the breakdown could occur in the passivation layer before the channel breakdown. The breakdown within the passivation layer is irreversible and is unexpected, especially for field plate FETs with a shorter gate-to-drain distance. To avoid this issue, passivation engineering for the β-Ga_2O_3 FET was extensively investigated. The $\varepsilon_p \times E_{bp}$ is used to evaluate the breakdown characteristics of the passivation material, where ε_p and E_{bp} are the dielectric constant and the critical electric field, respectively. Al_2O_3, SiO_2, SiN_x, and polymers were utilized to improve the breakdown performance of β-Ga_2O_3 FET [167]. Al_2O_3 exhibits a satisfying figure of merit of 69.4 MV/cm and is suitable for the passivation of the β-Ga_2O_3 FET. In the early stage, Al_2O_3 was deposited by atomic layer deposition to form the gate dielectric as well as the channel passivation [115]. However, the deposition speed is difficult to meet the requirements of thick passivation films. SiO_2 deposited by PECVD shows high film quality and high deposition speed [197]. In addition, a figure of merit of 39 MV/cm suggests that it is suitable for the passivation layer. Further, SiN_x passivation with a figure of merit of 75 MV/cm was introduced to improve the breakdown characteristics of β-Ga_2O_3 FET. A breakdown voltage of 1.37 kV for a gate-to-drain distance of 16 µm was obtained [167]. Recently, the in situ epitaxial passivation has been introduced by using the UID β-Ga_2O_3 [200]. The in situ passivation is expected to perform greater electric characteristics than the ex situ due to the improved interfacial properties, which are verified by its enhanced breakdown voltage. In addition, a SU-8 passivation layer was introduced to avoid air arcing and to maximize the breakdown voltage [201]. The SU-8 passivation was formed by coating and baking process after the gate-connected field plate β-Ga_2O_3 MOSFET was fabricated. The device without SU-8 passivation showed a breakdown voltage of 2.7 kV, while the use of the SU-8 passivation improved the breakdown voltage up to 6.7 kV. Therefore, for extremely high-voltage applications, the passivation engineering needs further research.

In addition to the gate field plates, source-connected field plates would also be an effective approach to suppress the peak electric field [199,202,203]. Lv et al. proposed a source field-plated β-Ga_2O_3 MOSFET [202]. The fabrication of the source field plate is similar to that of the gate field plate, where the pattern of the field plate was realigned to the source contact rather than the gate contact. The breakdown voltage was increased from 260 V to 480 V with a source-to-drain distance of 11 µm after introducing the source field plate. Simulation results showed that the electric field peak at the gate edge was reduced by nearly 30% due to the secondary electric field peak introduced by the source field plate. Most importantly, the proposed device realized a BFOM of 50.4 MW/cm^2, highlighting the potential of the field plate techniques. Furthermore, by incorporating the source-connected and the T-shape gate-connected field plates, a lateral β-Ga_2O_3 with a BFOM of 277 MW/cm^2 was achieved [204]. The V_b and the R_{on} of the proposed device with a gate-to-drain distance of 4.8 µm were measured to be 1.4 kV and 46.2 mΩ·cm^2, respectively. Simulation results also indicated that the peak electric field in the SiN passivation layer was two times higher than the channel layer, indicating that the breakdown happens in the SiN layer and optimization could be conducted in the future.

Recently, the performance of the double source-connected field plates β-Ga_2O_3 MOSFET has been investigated [205]. The double source field plate would reduce the electric field peak at the drain side of the field plate edge, thus minimizing the impact of an unoptimized field plate on the breakdown performance. The breakdown voltage of the double field plate MOSFET was measured to be 2440 V, while the single field plate MOSFET only exhibited a breakdown voltage of 1230 V.

VLD is also a promising approach to optimize the electric field profile since the potential distribution governed by Poisson equation can be altered through the varying of the channel concentration distribution [206–208]. Zhou et al. investigated the performance improvement of VLD β-Ga_2O_3 MOSFET by numerical methods [209]. The device diagram can be found in Figure 11b. The doping concentration has a minimum value of 1×10^{16} cm^{-3} under the gate, and gradually increases towards the drain side. Numerical results show that the peak electric field in the channel was reduced from nearly 9 MV/cm to 7.03 MV/cm by applying a drain voltage of 1500 V, resulting in a 58% improvement in breakdown voltage.

p-type doping can assist to deplete the drift layer, and thus improve the V_b~R_{on} relationship. Considering the difficulty in achieving *p*-type doping, a *p*-NiO_x/*n*-Ga_2O_3 heterojunction gate FET was demonstrated, as shown in Figure 12 [135]. The gate dielectric was replaced by *p*-type NiO_x with a thickness of 215 nm and acceptor concentration of 2×10^{18} cm^{-3}. The results show that the *p*-type NiO_x is beneficial to the surface lateral depletion, indicating that a higher channel concentration can be realized. As a result, the V_b was measured to be 1115 V and the R_{on} was 3.19 mΩ·cm^2, giving a BFOM value of 390 MW/cm^2.

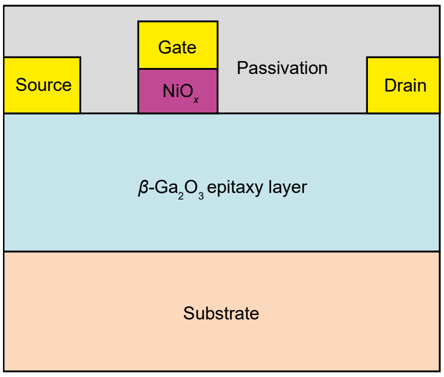


Figure 12. Device structure of the β-Ga_2O_3 FET with *p*-NiOx gate dielectric.

For a given MOSFET structure, the relationship between the breakdown voltage and the on-state resistance is strongly dependent on the channel doping concentration. For β-Ga_2O_3 power MOSFETs, unintentional doping plays an important role and impacts the V_b~R_{on} relationship in a dramatic way. Unintentional doping determines the carrier concentration in the channel and thus sets the upper limit on breakdown voltage. Therefore, to further improve the limit of breakdown voltage, unintentional doping needs to be reduced. Recently, the incomplete ionization, i.e., the 110 meV unintentional donor in power β-Ga_2O_3 devices, has been investigated [210]. In the on state, the 110 meV energy is significant enough and would cause the incomplete ionization. As a result, the on-state resistance remains unchanged. However, in the reverse state, the electron can gain enough energy to be activated as a carrier, reducing the depletion width and the breakdown voltage. The 110 meV donor concentration should be less than 5×10^{14} cm^{-3} in order to minimize its impacts on $V_b \sim R_{on}$ characteristics. The fabrication of a high-quality epitaxy layer is critical for power applications and more research is needed.

3.3. E-mode Operation

Due to the difficulty in realizing the *p*-type doping, most β-Ga_2O_3 power devices are fabricated by a junctionless epitaxy layer and present a depletion-mode operation. However, power applications prefer enhancement-mode (E-mode) for the convenience of circuits design. Theoretically, the E-mode can be achieved by decreasing the channel thickness or the channel doping concentration beneath the gate electrode. Recently, various β-Ga_2O_3 MOSFET structures have been proposed and fabricated to illustrate the feasibility of E-mode operation [122,125,211–215]. An enhancement-mode β-Ga_2O_3 wrap-gate fin field-effect transistor (FinFET) fabricated on a native (100) substrate was proposed [211]. The fin array with fin width of 300 nm and fin pitch of 900 nm was formed by electron beam lithography. Since the gate was wrapped on the fin, the gate control ability could be improved, and the E-mode should be realized. The measured threshold voltage was +0.8 V at a drain voltage of 10 V. In addition, the breakdown voltage was greater than 600 V for a gate to drain distance of 21 µm. However, only a 0.18 mA/mm on-state current was observed, which limits its application in high power density scenarios.

Another approach to reducing the channel thickness is the recessed-gate structure, as shown in Figure 13 [212]. A threshold voltage of +2 V was measured, and an on-state current of 40 mA/mm was achieved. Besides, the breakdown voltage exceeded 505 V at a source drain spacing of 8 µm. Recently, a β-Ga_2O_3 trench gate MOSFET was fabricated and the enhancement mode was realized [216]. The channel thickness under the gate was reduced to realize a full depletion. A threshold voltage of +4.2 V was extracted with a drain voltage of 10 V. Meanwhile, the peak transconductance was measured to be 2.7 mS/mm, and the maximum drain current was 11 mA/mm. The switching performance was also evaluated in the work. A turn-on time of 28.6 ns and a turn-off time of 94.0 ns were observed, indicating that the trench gate β-Ga_2O_3 MOSFET is suitable for high-speed switching applications.

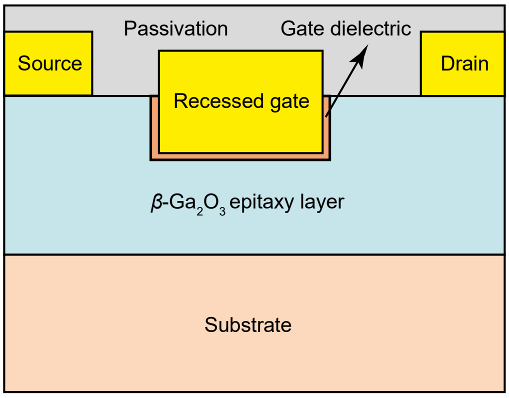


Figure 13. Device structure of the β-Ga_2O_3 FET with a recessed-gate structure.

In terms of the channel concentration reduction, Wong et al. demonstrated an enhancement-mode β-Ga_2O_3 MOSFET with Si ion-implanted source and drain [122]. The doping concentration under the gate is nearly identical to the UID layer, and thus the normally off operation could be achieved. A positive threshold voltage was observed, but the drain current was measured to be only 1.4 mA/mm. The low current driving capability is mainly due to the high-resistance UID channel. In addition, the absence of gate-drain underlap would also undermine the breakdown performance.

Recently, the unintentional N and Si doping in β-Ga_2O_3 layer fabricated by the plasma-assisted molecular beam epitaxy (PAMBE) method with high-purity O_2 gas (>99.99995%) as source gas was studied [125]. Note that unintentional N and Si incorporation was observed during the MBE with ozone gas as an O source. Therefore, it is likely that the impurity in the O_2 gas accounts for the source of N atoms. Since N is expected to behave as a deep acceptor in β-Ga_2O_3, the *n*-type unintentionally doped Si could be neutralized and the normally off operation would be achieved. It is found that the N and Si concentration varies with different O_2 flows. By optimizing the growth condition, N and Si doping concentrations of 1×10^{18} cm^{-3} and 2×10^{17} cm^{-3} were obtained, respectively. The threshold voltage was greater than +8 V and the E-mode was successfully achieved.

3.4. Vertical FETs

The aforementioned devices are lateral β-Ga_2O_3 FETs. Recently, vertical β-Ga_2O_3 power MOSFETs have received much attention due to their higher current density per chip, which is more suitable for discrete power devices [214,215,217–226]. A depletion-mode vertical β-Ga_2O_3 trench MOSFET with a fin-shaped channel was developed [217], as shown in Figure 14a. The Si-doped contact and the *n*-drift layers were grown on a Sn-doped (001) substrate by halide vapor phase epitaxy. The trench structure, i.e., the fin-shaped channel, was formed by the ion etch, followed by the deposition of the gate oxide, gate electrode, SiO_2, and source contact, respectively. The current density was measured to be 250 A/cm^2 with a gate overdrive voltage of 20 V and a drain voltage of 1.4 V. The on-state resistance was 3.7 mΩ/cm^2, indicating a promising power density the vertical β-Ga_2O_3 MOSFET could handle.

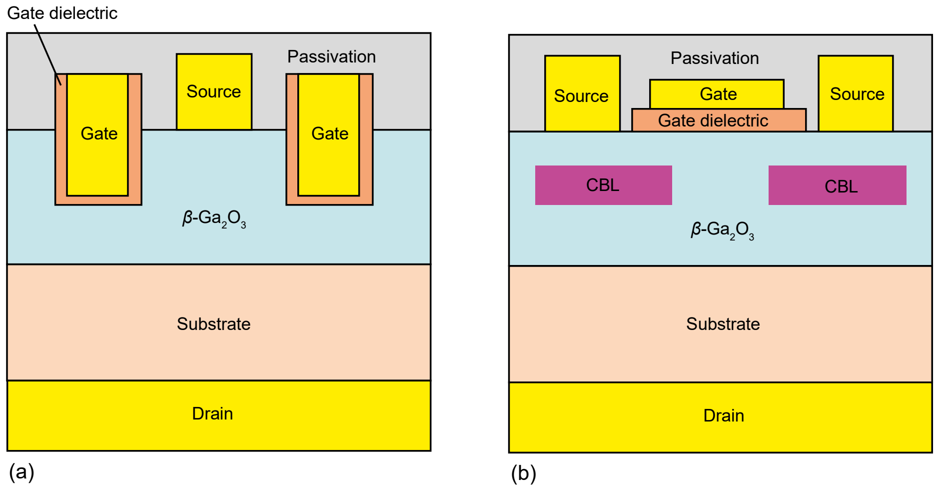


Figure 14. (**a**) Depletion-mode vertical β-Ga_2O_3 trench MOSFET. (**b**) Planar-gate current aperture vertical β-Ga_2O_3 MOSFET.

Another benefit from vertical MOSFETs with the fin-shaped channel is that the E-mode can be easily achieved by simply reducing the channel width between the gate electrodes. Hu et al. proposed an enhancement-mode β-Ga_2O_3 vertical transistor with a channel width of 330 nm and a channel length of 795 nm [215]. Due to the enhanced gate control capability, the proposed device exhibited a subthreshold slope of 85 mV/Dec and an on-state current up to 500 A/cm^2. The threshold voltage varies from 1.2 to 2.2 V, and thus the device is easy to drive. Moreover, the breakdown voltage of the E-mode vertical MOSFET has reached 1000 V, indicating the great potential of vertical devices in high power density applications.

Switching performances of the vertical β-Ga_2O_3 MOSFET with various dielectric designs were also evaluated [226]. A thicker dielectric in the inter-fin area could reduce the electric field at the corner of the fin-shaped channel, thus improving the breakdown voltage. Meanwhile, the placement of source electrodes impacts the switching performance significantly. It was observed that inter-fin areas with fully filled dielectric could lower the gate-to-source capacitance and, therefore, speed up the switching time. The damage introduced by the dry etching would lower the carrier mobility. The reduced mobility undermines the switching time as well as the switching loss, and thereby additional treatment should be introduced.

The vertical architecture can be also implemented without a trench gate. However, one should address the leakage current in such a case because of the inefficient gate control. The all ion-implanted planar-gate current aperture vertical β-Ga_2O_3 MOSFET has been demonstrated [219], which is plotted in Figure 14b. The current blocking layer was introduced by Mg implantation under the source electrodes, and the current aperture was thus formed. Transfer characteristics showed a peak transconductance of 1.25 mS/mm and a ~1.1 kA/cm^2 current density. However, the off-state current remained high due to the residual donor in the current blocking layer, which needs further improvement. Later on, a current aperture vertical MOSFET with nitrogen current-blocking layers was proposed [223]. The doping concentration of the channel area under the gate was 1.5×10^{18} cm^{-3}. The current density was 420 A/cm^2 and the on-state resistance was 31.5 $m\Omega/cm^2$. The leakage current can be as low as 10^{-6} A/cm^2 but it requires a gate voltage of −55 V. More recently, Wong et al. achieved an E-mode current aperture vertical β-Ga_2O_3 MOSFET by reducing the channel doping concentration to 5×10^{17} cm^{-3} [214]. A positive threshold voltage was observed, and an on-state current of 26 A/cm^2 was obtained. The breakdown voltage was 263 V and the $R_{on,sp}$ was 135 $m\Omega \cdot cm^2$ with a gate-to-drain distance of 9 μm.

4. Conclusions

We reviewed the progress of the β-Ga_2O_3 power devices including SBD and FET, in the view of device operations, structures, corresponding discussions, and some key matters (the comparison of their electrical performances can be found in Tables 2 and 3). Owing to the excellent natural physical properties, β-Ga_2O_3 is placed great expectations as the supplements in medium- and low-voltage devices (such as in Si-, SiC-, and GaN-based electronics, etc.), and also represent a particular advantage in high-voltage and high-frequency devices, benefit by its high John's figure of merit and Baliga's figure of merit.

Table 2. Comparison of electric performances for β-Ga_2O_3 SBDs.

Structures	V_{on} (V)	$R_{on,sp}$ ($m\Omega$ cm^2)	V_b (V)	n	I_{on}/I_{off}	SBH (eV)	FOM (MW/cm^2)	Refs.
Pt/Ti/Au with UID substrate	1.23	7.85	150	1.04–1.06	10^{10}	1.52	3.1	[67]
Ni/Au SBD	/	25	1600	1.07	10^7	1.22	102.4	[69]
Double-barrier SBD	1.13	4.1	630	/	10^{10}	1.26–1.62	96.8	[75]
SBD on ($\bar{2}01$) and (010) substrates	1.0, 1.3	0.56	/	1.34	10^9	1.27	/	[70]
SBD with F-plasma treatment	0.95	4.6	470	/	10^6	1.31	48	[77]
SBD with Al-reacted interfacial layer	0.79	/	/	1.19	10^9	1.39	/	[78]
Trench SBD	/	2.9	240	1.1	10^9	1.07	19.9	[87]
Trench SBD	1.25	9.8	2960	/	10^{10}	1.4	450	[80]
SBD with field plate	1.32	5.1	1067	1.03 ± 0.02	10^{14}	1.46	223.2	[97]
SBD with beveled field plate	/	3.6	190	1.03 ± 0.02	10^{10}	1.5	10	[100]
SBD with small-angle beveled field plate	/	2	1100	1.2	10^9	1.2	605	[102]
Trench SBD with dual field plate	/	8.8	2890	1.3	10^{10}	1.38	950	[103]
SBD with Mg-implanted edge termination	/	5.1	1550	1.05	10^9	1.01	470	[91]
SBD with He-implanted edge termination	0.73	4.8	1000	1.19	10^{11}	1.04	208.3	[95]
SBD with Mg-implanted edge termination	0.82	5.4	1500	1.11	10^{11}	1.17	416.6	[95]
SBD with Ar-implanted edge termination	1	4	391	1.02	10^{13}	/	38.2	[93]
SBD with compound termination	0.7	4	400	1.09	10^6	1.04	40	[96]
SBD with nitrogen-implanted guard ring	1.6	4.7	1430	1.04	10^{13}	/	435.1	[105]

Table 3. Comparison of electric performances for β-Ga_2O_3 FETs.

Structures	D-/E-Mode	I_{on}/I_{off}	V_b (V)	E_b (MV/cm)	g_m (mS/mm)	I_{on} (mA/mm or A/cm^2)	FOM (MW/cm^2)	$R_{on,sp}$ (mΩcm^2)	Refs.
Sn-doped MESFET	D	10^4	257	0.3	2.8	13	0.2	300	[114]
Sn-doped MOSFET	D	10^{10}	370	0.46	~3	39	1.8	75	[115]
Spin-on-glass doping	D	10^8	382	0.38	1.23	40	/	/	[123]
Si-doped MOSFET	D	10^9	/	/	3.2	80	/	/	[119]
Ge-doped MOSFET	D	10^8	479	0.87	/	75	/	/	[121]
Si-doped $(Al_{0.2}Ga_{0.8})_2O_3/Ga_2O_3$	D	10^5	/	/	1.75	5.6	/	/	[165]
Ge-doped $(Al_{0.2}Ga_{0.8})_2O_3/Ga_2O_3$	D	10^9	/	/	4	20	/	/	[164]
Dual-Si-doped $(Al_{0.2}Ga_{0.8})_2O_3/Ga_2O_3$	D	10^8	3.2	2.76	39	257	/	/	[166]
$Al_2O_3/BaTiO_3$ gate dielectric stack	D	10^7	840	5.5	/	200	408	1.72	[171]
Ga_2O_3 on SiC	E	10^7	800	0.22	/	55	13	49	[184]
Gate field plate	D	10^9	755	0.5	3.4	78	/	/	[197]
Gate field plate with SU-8 polymer passivation	D	10^7	8030	1.69	/	3	0.008	/	[201]
Source field plate	D	10^6	480	0.44	10.5	267	50.4	4.57	[202]
Source field plate and T-shaped gate field plate	D	10^9	1400	2.9	8.5	230	277	7.08	[204]
Dual source field plate	E	10^8	2440	3.1	/	/	94.35	63.1	[205]
p-NiO heterojunction gate	D	10^{10}	1115	2.6	/	455	390	3.19	[135]
Ga_2O_3 FinFET	E	10^5	567	0.35	/	0.18	/	/	[211]
Recess gate MOSFET	E	10^9	505	1.44	/	40	14.8	17.2	[212]
Trench gate MOSFET	E	10^7	/	/	2.7	11	/	27.3	[216]
UID channel MOSFET	E	10^6	/	/	0.38	1.4	/	/	[122]
Nitrogen-doped channel	E	10^5	/	/	/	0.0012	/	/	[125]
Trench gate vertical FET	D	10^3	/	/	/	250	/	3.7	[217]
Trench gate vertical FET	E	10^8	1057	1.1	/	350	62.1	18	[215]
Vertical FET with Mg-implanted CBL	D	10^0	/	/	5	410	/	/	[219]
Vertical FET with N-implanted CBL	E	10^8	<30	/	14.5	420	/	31.5	[214]

Comparisons of the V_b~$R_{on,sp}$ relationship between the reviewed work and β-Ga_2O_3 limit are shown in Figure 15. Current β-Ga_2O_3 power devices have broken through the limits of the Si-based counterparts, and the SiC limit will soon be surpassed. As the room for material and structure optimization to reach the β-Ga_2O_3 theoretical performance is still significant, efforts should continue to improve the competitiveness of this new but promising semiconductor power device. In general, β-Ga_2O_3 SBDs have received a higher level of development than that of β-Ga_2O_3 FETs. Commercial demonstrations of β-Ga_2O_3 SBDs will soon be available, and yet their performance can be further improved.

Various edge terminations have been proposed in recent years to relieve the edge electric field and the premature breakdown of β-Ga_2O_3 SBDs. Due to the lack of *p*-type doping, the realization of the advanced engineering such as the *p*-doped guard ring is facing challenges. It is well known that the flatness of the valence band for the β-Ga_2O_3 limits its practical *p*-doping. We believe that the introduction of hetero *p*-type semiconductors may be a feasible solution in the near future. In the long term, energy band engineering is expected to overcome this issue.

As for the optimization of the electric field profile, most works are aimed at the interface of the Schottky contact. However, the improvement of the bulk profile is also important because it amends the V_b~$R_{on,sp}$ relationship. Numerous approaches could achieve this such as gradient doping or charge balancing. For vertical FETs, this conclusion also applies. Although the Schottky barrier height can be tuned, its optimal value or range is unknown since the application strategy of β-Ga_2O_3 SBD is still undetermined. In addition, precise control of the Schottky barrier height requires further development.

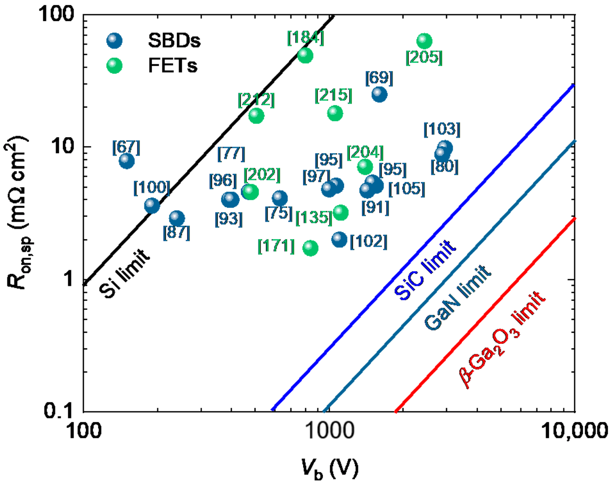


Figure 15. Benchmark of the V_b~$R_{on,sp}$ relationship for the aforementioned work.

Currently, the vertical β-Ga$_2$O$_3$ SBD is the mainstream and is more suitable for discrete devices. As the importance of the integration for power electronics increases, it is suggested that the planar SBD should receive more attention. Few studies in the literature focus on the β-Ga$_2$O$_3$ planar SBD since it suffers low current driving capabilities due to the crowding effects, and thus more efforts should be conducted.

For β-Ga$_2$O$_3$ FET, the on-state resistance has been significantly reduced over the last few years, and ohmic/Schottky contacts with high-quality interfaces and epitaxy layers with less defects have been developed. The surface quality of the epitaxy layer, with etch-induced and implant-induced damage, could be further optimized to improve the carrier mobility. To date, carrier mobility in a fabricated HEMT remains low compared to the first principles calculation results. Therefore, device physics involving carrier transport should be further investigated.

Heterointegration is an effective method but requires complex fabrication processes. Direct growth of the β-Ga$_2$O$_3$ epitaxial layer on a non-native substrate would be more efficient. In addition, engineering that has been developed in Si, GaN, and SiC power devices could also be applicable to the β-Ga$_2$O$_3$ devices. Charge coupling, heterojunction, and high-*k* techniques would be demonstrated soon.

Due to the unintentional doping of the β-Ga$_2$O$_3$ epitaxial layer and the lack of *p*-doping, depletion-mode FET is easier to obtain. The enhancement-mode operation is preferred for power circuits and systems; thus, the normally off β-Ga$_2$O$_3$ power FET should receive more attention. There appears to be a contradiction between the E-mode operation and the high current driving capability. Structural engineering is expected to address this issue. Besides, the combination of the E-mode and electric field management should be also put on the agenda.

In conclusion, β-Ga$_2$O$_3$ single crystal substrate and epitaxial layers have been basically solved, and high-performance prototype devices have been realized. It is expected that the explosion period of β-Ga$_2$O$_3$ ultra-wide bandgap semiconductor industry will come in the next few years.

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