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Ferroelectric Memory Based on Topological Domain Structures: A Phase Field Simulation

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Abstract: The low storage density of ferroelectric thin film memory currently limits the further application of ferroelectric memory. Topologies based on controllable ferroelectric domain structures offer opportunities to develop microelectronic devices such as high-density memories. This study uses ferroelectric topology domains in a ferroelectric field-effect transistor (FeFET) structure for memory. The electrical behavior of FeFET and its flip properties under strain and electric fields are investigated using a phase-field model combined with the device equations of field-effect transistors. When the dimensionless electric field changes from −0.10 to 0.10, the memory window drops from 2.49 V to 0.6 V and the on-state current drops from 2.511 mA to 1.951 mA; the off-state current grows from 1.532 mA to 1.877 mA. External tensile stress increases the memory window and off-state current, while compressive stress decreases it. This study shows that a ferroelectric topology can be used as memory and could significantly increase the storage density of ferroelectric memory.

Keywords: topological domain; polar topologies; domain switching; phase-field simulations

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1. Introduction

Ferroelectric memory, which features non-volatile memory, is used in defense and civilian products, such as security systems, aerospace and automotive electronics, and smart cards [1,2]. However, the low storage density of ferroelectric memory based on ferroelectric thin film limits its further application. Numerous methods have been proposed to improve the storage density of ferroelectric memory. The most frequently mentioned is the increasing of the storage density in ferroelectric memory by reducing the area of a single memory cell. Chiu demonstrated the switchable diode characteristics in highly strained $BiFeO_3$(BFO) thin films, significantly reducing the memory dimension with the same storage capacity [3]. The size reduction would result in a noticeable degradation of ferroelectric performance, which would impact data storage and reading [4–9]. It has been reported that novel polarized topological domain structures are formed when ferroelectric materials are scaled down to the nanoscale [10–14]. Li demonstrated that central topological domains could spontaneously form in BFO nano-islands [15]. Under the application of electric fields, a reversible switch can be found between two morphologies of central convergence and central divergence. Tang observed the atomic morphology of the flux-closure quadrant, as well as a periodic array of flux closures in ferroelectric $PbTiO_3$ films, which were mediated by tensile strain on a $GdScO_3$ substrate using aberration-corrected scanning transmission electron microscopy [16]. It has been noted that the different states of ferroelectric topology can be used to record the "1" and "0" of binary information [17]. Using the ferroelectric topological domain structure as the basic information storage unit efficiently achieves high-density storage. Biswas achieved the reversible switching of

partial topological domains by applying an electric field to two pairs of electrodes on $Pb(Mg_{1/3}Nb_{2/3})O_3$-$PbTiO_3$ substrates [17]. Ping realized that skyrmions could be created locally via an electric field in the magnetoelectric helimagnet Cu_2OSeO_3 [18]. Significant domain wall conduction was found in diamond-shaped BFO nano-islands embedded in a tetragonal phase matrix, leading to current readout in different types of center states and promising the development of non-volatile memories with current readout [19]. Other topological states have been found in isolated nanostructures. For instance, Schilling [20] et al., McGilly [21] et al., and McQuaid [22] et al., reported closed quadrant states in the single crystal nanoplates of $BaTiO_3$. The application of polarized topological domains in ferroelectrics has potential application prospects in ferroelectric memory. These studies primarily investigated the flip-flop of ferroelectric topology under external field conditions. They did not investigate storage properties such as memory windows. These studies also identified critical issues, which must be addressed before ferroelectric topology domain structures can be realized for storage. To the best of our knowledge, there are still relatively few systematic studies on the electric properties of the output characteristics of topology-based domain memory. Additionally, the experimental tuning of topological domain structures is already complicated; it is even more challenging to implement when used as a basic storage unit for memory.

In this study, to model the generation of ferroelectric topological domain structures and realize storage, a phase-field approach was applied to obtain the topological domain structure of ferroelectrics. Topological domain structure-based ferroelectric memory is controlled using electric and force fields based on field-effect transistor device equations. The simulation results establish a theoretical foundation for topological domain storage.

2. The Simulation Methodology

$PbTiO_3$ (PTO) has a high Curie temperature (490 °C) and a substantial spontaneous polarization, allowing it to be used in various ferroelectric devices. The research objective in this work was PTO. The topological domain structure of ferroelectrics was obtained by using the phase field method. F is the total free energy of the ferroelectrics, which is described as [23]:

$$\begin{aligned} F = \alpha_i P_i^2 \quad & +\alpha_{ij} P_i^2 P_j^2 + \alpha_{ijk} P_i^2 P_j^2 P_k^2 + \tfrac{1}{2} c_{ijkl} \varepsilon_{ij} \varepsilon_{kl} - q_{ijkl} \varepsilon_{ij} P_k P_l \\ & + \tfrac{1}{2} g_{ijkl} P_{i,j} P_{k_l l} - \tfrac{1}{2} \varepsilon_0 \varepsilon_r E_i E_i - E_i P_{i,} \end{aligned} \tag{1}$$

where P_i, ε_{ij}, and E_i are the polarization, strain, and electric field components, respectively. The electric field E_i = (E_1, E_2, E_3) in Equation (1) is extended to include the uncurled electric field E^{Unc} generated by the inhomogeneous polarization, the depolarization field, and a prescribed curled electric field. S is the coiled field's vorticity vector and u is the displacement vector [24,25]. In Equation (1), $\alpha_{i,}$ α_{ij}, and α_{ijk} are the higher-order dielectric stiffness coefficients, c_{ijkl} is the elastic constant, q_{ijkl} is the electrostrictive coefficient, g_{ijkl} is the gradient energy coefficient, ε_0 is the gradient energy coefficient, and ε_r is the relative dielectric constant. The topological domain of the ferroelectrics was then obtained by solving the time-dependent Ginzburg–Landau (TDGL) equation [26,27]:

$$\frac{\partial P_i(r,t)}{\partial t} = -L \frac{\delta F}{\delta P_i(r,t)} (i = 1, 2, 3) \tag{2}$$

where r and t are the spatial vector and time, respectively. L is the kinetic coefficient; i = 1, 2, 3 corresponds to the x, y, and z directions, respectively. To facilitate the calculation, the parameters were dimensionless in the simulation. The dimensionless process of the cyclic vorticity S and the toroidal moment G is where the characteristic moment is defined as $\boldsymbol{G}_0 = u_0 P_0$ =1 nm × 0.757 C/m^2 = 0.47 e/Å, in which u_0 and P_0 are the duple characteristic length and characteristic polarization, respectively [28]. The selection and details of other dimensionless parameters are described in our previous work [26]. Transistors based on ferroelectric nanodots with topology domain structures were studied in the simulation.

The cross-section of the transistors is shown in Figure 1a. The different chirality of the ferroelectric layer vortex indicates the stored "0" and "1". The top metal electrode is metal Pt with an extremely high work function (5.6 eV) and a thickness of 80 nm, and the ferroelectric layer is a PTO under the metal electrode. The semiconductor layer is Si with a thickness of 600 nm, the most widely used semiconductor material, and the insulating layer is a SiO_2 layer with a thickness of 140 nm, which can easily be grown on a silicon substrate. In addition to the two-dimensional case, which reflects most of the critical properties of the ferroelectric topological domain structure, topological domains were found to exist in the plane in our previous study; therefore, we used a two-dimensional phase field model in this study [29]. The ferroelectric topology domain structure in PTO is modeled on a discretely sized grid and the grid spacing is set as $\Delta x^* = \Delta z^* = 0.3$, corresponding to the actual size of 7.2 nm; the time step is set as $\Delta t^* = 10{,}000$.

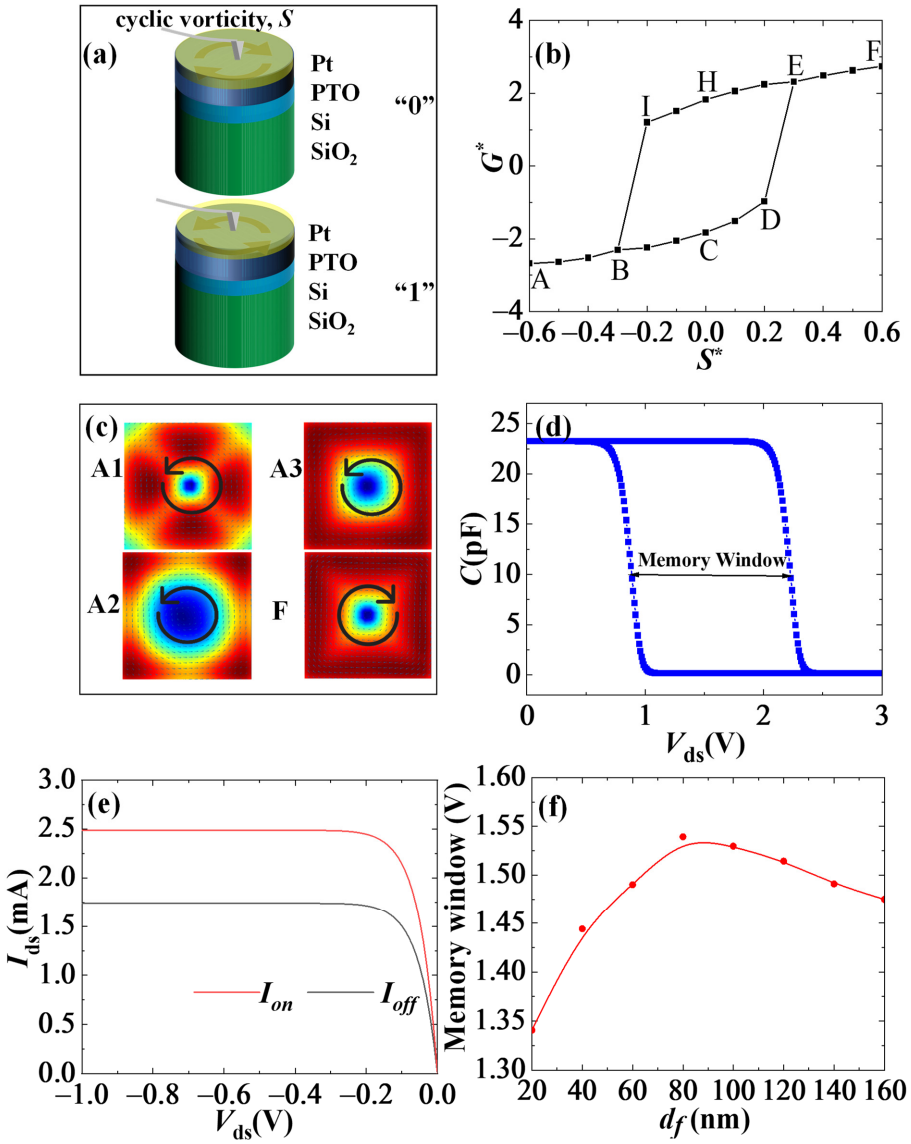

Figure 1. (**a**) Schematic diagram of the ferroelectric topology domain transistor structure. (**b**) Hysteresis loop between the toroidal moment G^* and vorticity S^* at room temperature (A-I is the loading point corresponding to S^*). (**c**) A1, A2, and A3 are 500 steps, 5000 steps, and 10,000 steps at point A, respectively, and F shows the ultimate domain structure at point F. (**d**) C-V_{ds}. (**e**) I_{ds}-V_{ds}. (**f**) Memory window for different PTO thicknesses. The superscript * indicates the corresponding dimensionless posterior parameter.

The device equations of field-effect transistors were then developed to study the electric properties of the ferroelectric memory. Gate voltage is expressed as [28]:

$$V_g = V_f + V_i + \psi_s \tag{3}$$

where $V_f = d_f E_f$ denotes the corresponding voltage drop on the ferroelectric layer and $V_i = d_i E_i$ denotes the corresponding voltage drop on the insulator layer; d_f and d_i are the corresponding thicknesses of the ferroelectric layer and the insulator layer, respectively. E_f and E_i represent the electric field applied on the ferroelectric and insulator layers and ψ_s denotes the corresponding surface potential of the silicon substrate. The electric displacement is written as [30]:

$$D = \varepsilon_0 \varepsilon_f E_f + P(E_f) = \varepsilon_0 \varepsilon_i E_i = \varepsilon_0 \varepsilon_{si} E_{si} = -Q_s \tag{4}$$

where ε_f, ε_i, and ε_{si} are the relative dielectric constant of the ferroelectric layer, the relative dielectric constant of the insulator layer, and the relative dielectric constant of the silicon substrate, respectively. $P(E_f)$ denotes the polarization of the switching dipoles and Q_s denotes the space charge density on a silicon substrate, which can be written as [29]:

$$Q_s(\psi_s) = -sign(\psi_s)\frac{\sqrt{2}\varepsilon_0\varepsilon_i}{\beta L_D}\left(\frac{n_i^2}{N_D{}^2}(e^{-\beta\psi_s} + \beta\psi_s - 1) + (e^{\beta\psi_s} - \beta\psi_s - 1)\right)^{1/2} \tag{5}$$

According to Gauss's theorem, the capacitance of a ferroelectric capacitor can be described as [31]:

$$C_{Si}(\psi_s) = \frac{A_i\varepsilon_i\varepsilon_0}{\sqrt{2}L_D} \cdot \frac{\left(\frac{n_i^2}{N_D{}^2}(-e^{-\beta\psi_s} + 1) + (e^{\beta\psi_s} - 1)\right)}{\left(\frac{n_i^2}{N_D{}^2}(e^{-\beta\psi_s} + \beta\psi_s - 1) + (e^{\beta\psi_s} - \beta\psi_s - 1)\right)^{1/2}} \tag{6}$$

where $L_D = \sqrt{\varepsilon_0\varepsilon_S\phi_t/qN_D}$ represents the bulk Debye length. The capacitance of ferroelectrics and insulation is written as $C_f = A_f\varepsilon_0\varepsilon_f/d_f$, $C_i = A_i\varepsilon_0\varepsilon_i/d_i$ and the total capacitance as $C_{total} = (C_f{}^{-1} + C_i{}^{-1} + C_{Si}{}^{-1})^{-1}$. The leakage current ($I_{ds}$) is [32]:

$$I_{ds} = q\mu\frac{W}{L}\int_0^{V_{ds}}\int_{\psi_b}^{\psi_s}\frac{(n_i{}^2/N_D)e^{\beta}(\psi - V)}{\xi(\psi, V)}d\psi dV \tag{7}$$

where q is the electron charge and W and L are the effective conductive channel width and effective conductive channel length on the surface of the substrate, respectively. ψ is the difference between the Fermi level and the intrinsic Fermi level of the substrate.$\psi_b = -\phi\ln(\frac{N_D}{n_i})$, $\phi = kT/q$ is the thermodynamic potential of the system, whereby k denotes the Boltzmann constant and thermodynamic temperature. The C-V_{ds} relation and the output characteristic (I_{ds}-V_{ds}) curve can be obtained.

3. Results and Discussion

Figure 1a depicts the structure of the ferroelectric topology domain transistor. At room temperature, Figure 1b shows annular moment G^* and its response to cyclic vorticity S^*(d_f = 20 nm). The superscript * indicates the corresponding dimensionless posterior parameter. The counterclockwise start domain structure, denoted as A, is shown in Figure 1c in illustration A3, and the toroidal moment is −2.6775. After that, cyclic vorticity S^* is increased from −0.6 to 0.6 with a magnitude of −0.6. The inset A1 and A2 depict the evolution of the topological domain structure with time at point A, with time increments of 500 steps and 5000 steps, respectively. When the vorticity increases to 0.3, the polarized vortex switches and the topological domain structure becomes anti-counterclockwise. When S^* grows to 0.6 with a toroidal moment of 2.3166, the topological domain structure at

this point is shown in Figure 1c in illustration F. When cyclic vorticity S^* decreases from 0.6 to −0.6, cyclic vorticity switches from the F-I-B point and the toroidal moment change decreases from 2.7431 to −2.3056. The response to cyclic vorticity shows an asymmetric rectangular hysteresis line, which indicates that polarized vortices in ferroelectric topological domains have potential applications in future high-density memories, such as the *P-E* loop of the ferroelectric thin film. Cyclic vorticity from the F-I-B point and the vorticity moment change drops from 2.7431 to −2.3056 when cyclic vorticity S^* declines from 0.6 to −0.6. An asymmetric rectangular hysteresis line appears in response to the cyclic vorticity, indicating that polarized vortices in ferroelectric topological domains could be used in future high-density memory.

The C-V_{ds} and I_{ds}-V_{ds} characteristic curves were then investigated under the influence of cyclic vorticity. When the memory window is 1.3407 V, the open-state current is 2.487 mA and the closed-state current is 1.7388 mA (Figure 1e) (d_f = 20 nm). The C-V_{ds} curve is shown in Figure 1d (d_f = 20 nm), which is larger than the memory window of 1.08V in the literature [33]. The results indicate that the ferroelectric topology domain structure is feasible for storage and that transistors are based on a topological domain structure with a large memory window. Information storage cells based on this polar architecture are theoretically capable of achieving ultra-high density memory with an area density of more than 12 Tbit/in^2.

A change in the thickness of the ferroelectric layer leads to a change in the voltage shared on the ferroelectric layer, which in turn affects the magnitude of the ferroelectric layer capacitance and thus the size of the storage window of the device [34]. Therefore, it is important to study the effect of a ferroelectric layer's thickness on its memory window. Figure 1f shows the effect of different ferroelectric layer thicknesses on the storage window of FeFETs. It is evident that as the thickness increases, the storage window tends to increase and then decrease, reaching a maximum thickness of 80 nm. This is because the voltage on the ferroelectric layer increases as the thickness increases, and the increase in voltage makes the ferroelectric film polarization of the ferroelectric layer more adequate, thus making the storage window larger. However, as the thickness continues to increase, the voltage of the ferroelectric layer is no longer sufficient to simultaneously produce better polarization characteristics of the ferroelectric topology domains; this also leads to poor saturation performance, so the thickness of the ferroelectric layer continues to increase instead of reducing the storage window. However, the increase in the thickness of the ferroelectric layer will also lead to an increase in the size of the device, which is not in line with the development requirements of today's information technology. For this consideration, in the following simulations, we choose a PTO thickness of 20 nm. The development of ferroelectric topological domains is mainly due to the rivalry of distinct energies. To realize topological domain storage, the influence of the applied electric field on topological domains was thoroughly examined. Figure 2a shows the C-V_{ds} curves for various external electric fields (E_1^*), with the C-V_{ds} curves becoming narrower as E_1^* increases. The memory window shrinks from 2.49 to 0.6 V when E_1^* grows from −0.1 to 0.1 (Figure 2b). This can be explained as an increase in polarization due to the total system energy of the system's increase caused by the external electric field. Figure 2c shows I_{ds}-V_{ds} of ferroelectric memory as a function of E_1^*, with magnitudes of −0.10, −0.05, 0.05, and 0.10. When E_1^* increases from −0.10 to 0.10, the open-leakage current decreases from 2.516 mA to 1.951 mA and the closed-leakage current increases from 1.532 mA to 1.887 mA (Figure 2d). The rise in E_1^* makes the G^*-S^* curve thinner (Figure 2e) and the positive residual toroidal moment of the PTO decreases (Figure 2f). In addition, the positive charge generated in semiconductor Si decreases accordingly, which leads to resistance of the channel increases and open-state current increases [35]. Furthermore, as E_1^* climbs, the negative residual toroidal moment of the ferroelectric film diminishes, resulting in a decrease in the negative charge created in the semiconductor channel. More charge accumulates in the semiconductor channel with a large E_1^* and causes the transistor's closed-leakage current to decrease.

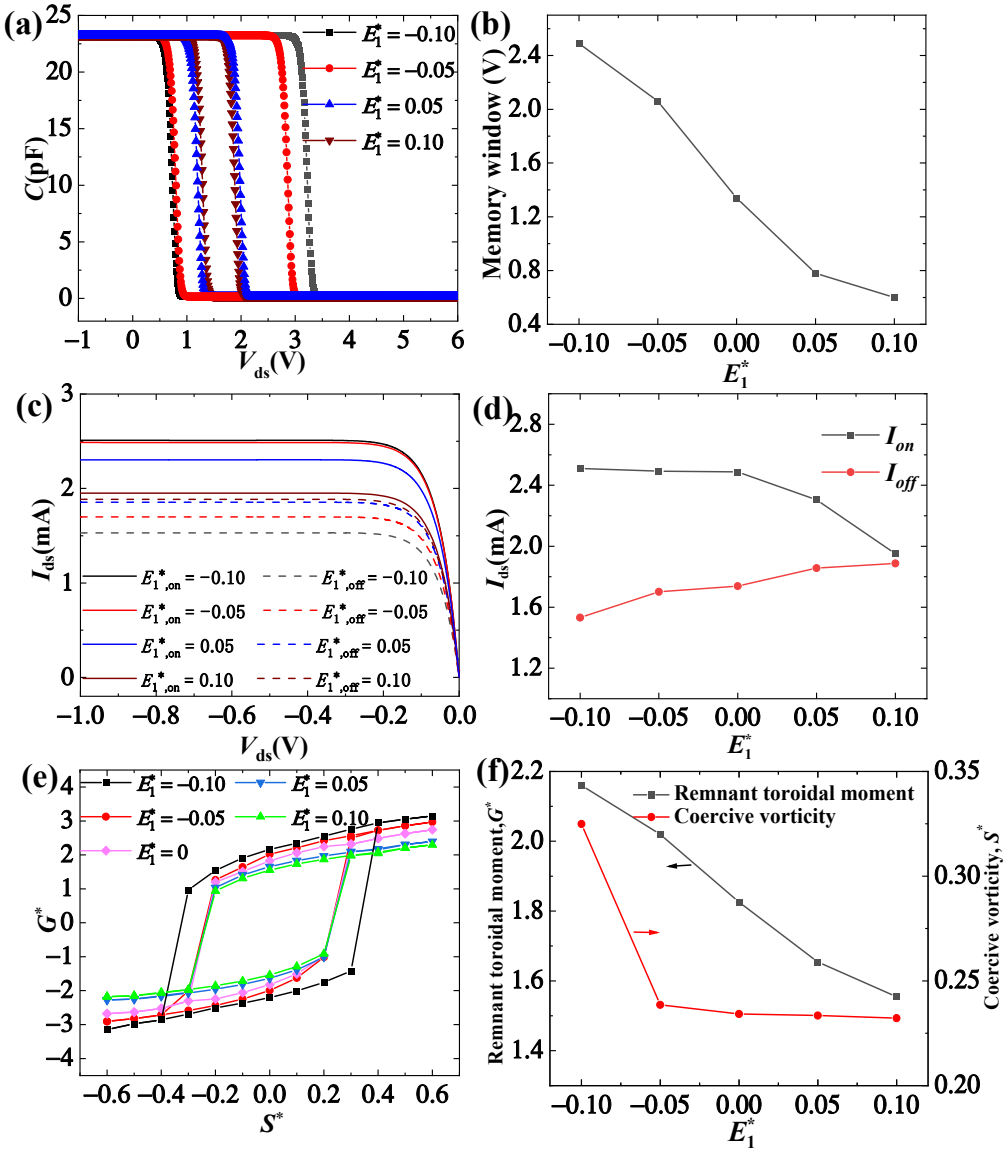

Figure 2. Effect of E_1^* on the ferroelectric topology domain transistors of (**a**) C-V_{ds} characteristics of Pt/PTO (20 nm)/Si/SiO_2 structures. (**b**) Memory window. (**c**) I_{ds}-V_{ds} characteristics of Pt/PTO (20 nm)/Si/SiO_2 structures. (**d**) Open-state current and closed-state current. (**e**) G^*-S^*. (**f**) Coercive vorticity and remnant toroidal moment. The superscript * indicates the corresponding dimensionless posterior parameter.

The force has a significant impact on the ferroelectric topology domain structure, which in turn has an impact on transistor performance. Here, we investigated the effect of stress on the behavior of topological domain structure transistors. Figure 3a represents the C-V_{ds} curves of the ferroelectric memory when $\sigma_{11} = -2 \times 10^8$ Pa and $\sigma_{11} = 2 \times 10^8$ Pa. When σ_{11} increases from -2×10^8 Pa to 2×10^8 Pa, the memory window decreases from 2.498 to 0.367 V (Figure 3b). When compressive stress becomes tensile stress, the elastic energy in the system progressively climbs and the elastic energy in the system grows as the polarization value increases. The voltage drop in the ferroelectric layer is raised. With a constant gate voltage, the pressure drop at both ends of the PTO rises, but the pressure drop at both ends of the insulating layer SiO_2 remains unchanged; therefore, the surface potential of the semiconductor Si layer decreases, resulting in a smaller memory window. At $\sigma_{11} = -2 \times 10^8$ Pa, the closed-leakage current is 1.701 mA and the open-state current is 2.911 mA. The open-state current is 1.887 mA at $\sigma_{11} = 2 \times 10^8$ Pa, while the closed-leakage current

is 2.304 mA (Figure 3c). The open-state current drops as it intensifies, but the closed-state current flows (Figure 3d). The positive residual toroidal moment decreases as the stress increases from -2×10^8 Pa to 2×10^8 Pa (Figure 3e,f), causing the charge induced in the Si channel to drop and the Si surface to progressively transition from an electron-accumulated to an electron-depleted state. As a result, channel resistance rises while the open leakage current falls. Furthermore, when the topological domain transistor channel is closed, the Si substrate surface is inverted. The value of the negative residual toroidal moment decreases during this process, resulting in a smaller degree of Si substrate inversion and, eventually, an increase in the closed-state leakage current.

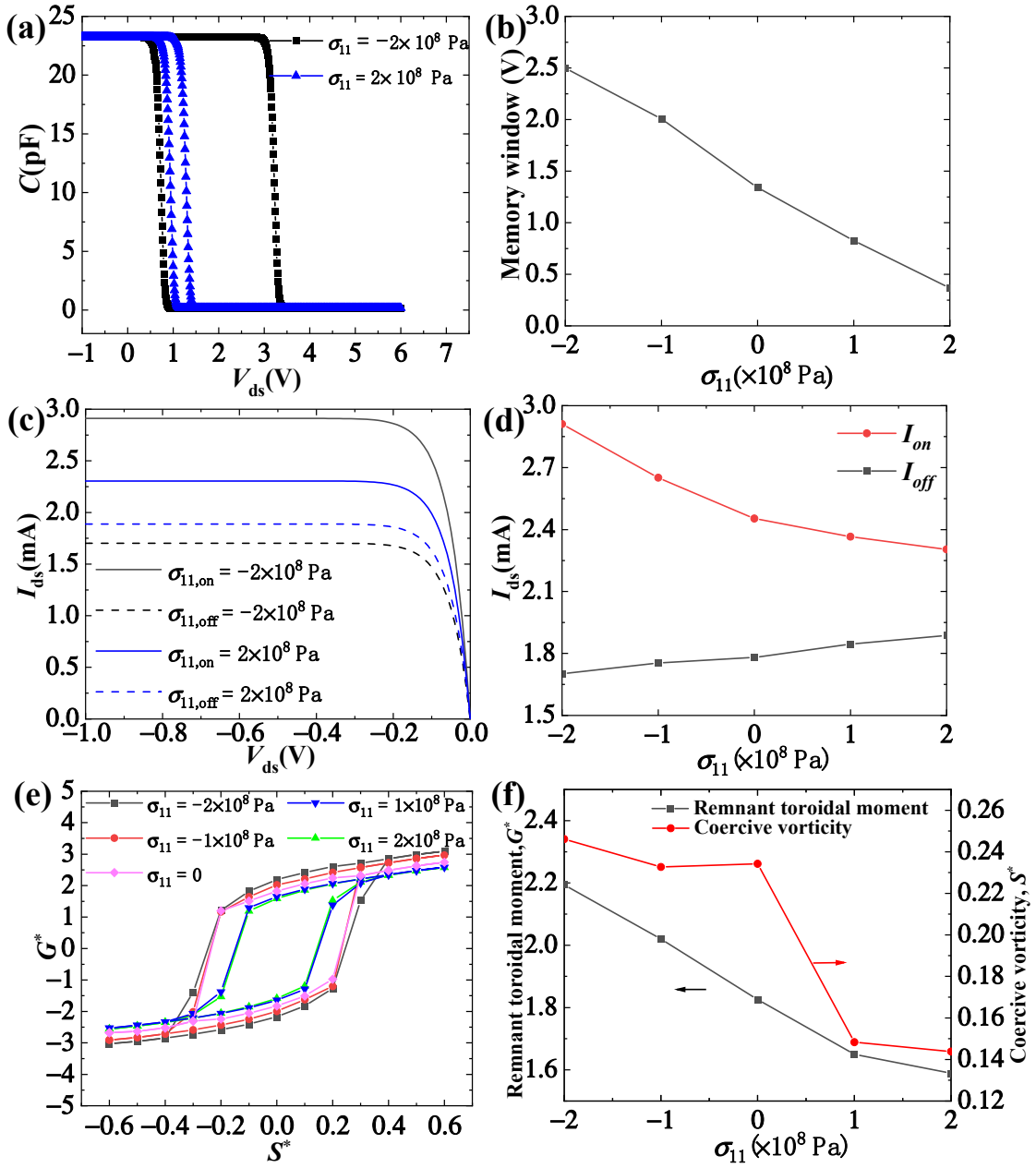

Figure 3. Effect of stress on ferroelectric topology domain transistors of (**a**) C-V_{ds} characteristics of Pt/PTO (20 nm)/Si/SiO_2 structures. (**b**) Memory window. (**c**) I_{ds}-V_{ds} characteristics of Pt/PTO (20 nm)/Si/SiO_2 structures. (**d**) Open-state current and closed-state current. (**e**) G*-S*. (**f**) Coercive vorticity and remnant toroidal moment. The superscript * indicates the corresponding dimensionless posterior parameter.

4. Conclusions

In conclusion, we used circulating eddy currents to successfully flip ferroelectric eddy currents. The response of toroidal moment $\boldsymbol{G}^*$ to cyclic vorticity S^* was obtained at room temperature. It was confirmed that the topological domain structure can be used for storage and this substantially increases the storage density of ferroelectric memory. Furthermore, topology is modulated by electric field and stress, and the C-V_{ds} relationship curve and output characteristic I_{ds}-V_{ds} relationship curve are obtained under various conditions using the semiconductor device equation. When the dimensionless electric field changes from -0.10 to 0.10, the memory window drops from 2.49 V to 0.6 V and the on-state current drops from 2.511 mA to 1.951 mA; the off-state current grows from 1.532 mA to 1.877 mA. When σ_{11} increases from -2×10^8 Pa to 2×10^8 Pa, the memory window decreases from 2.498 to 0.367 V. At $\sigma_{11} = -2 \times 10^8$ Pa, the closed-leakage current is 1.701 mA and the open-state current is 2.911 mA. The open-state current is 1.887 mA at $\sigma_{11} = 2 \times 10^8$ Pa, while the closed-leakage current is 2.304 mA. This points us in the right direction for the development of new non-volatile random access memory with an ultra-high density.

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Conflicts of Interest: The authors declare no conflict of interest.

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